2002/12/4

Winbond
Advanced ACPI Controller
W83303D

W83303D
Data Sheet Revision History

	Pages	Dates	Version	Version on Web	Main Contents
1		Nov./01	0.12	N/A	Draft Version
2					
3					
4					
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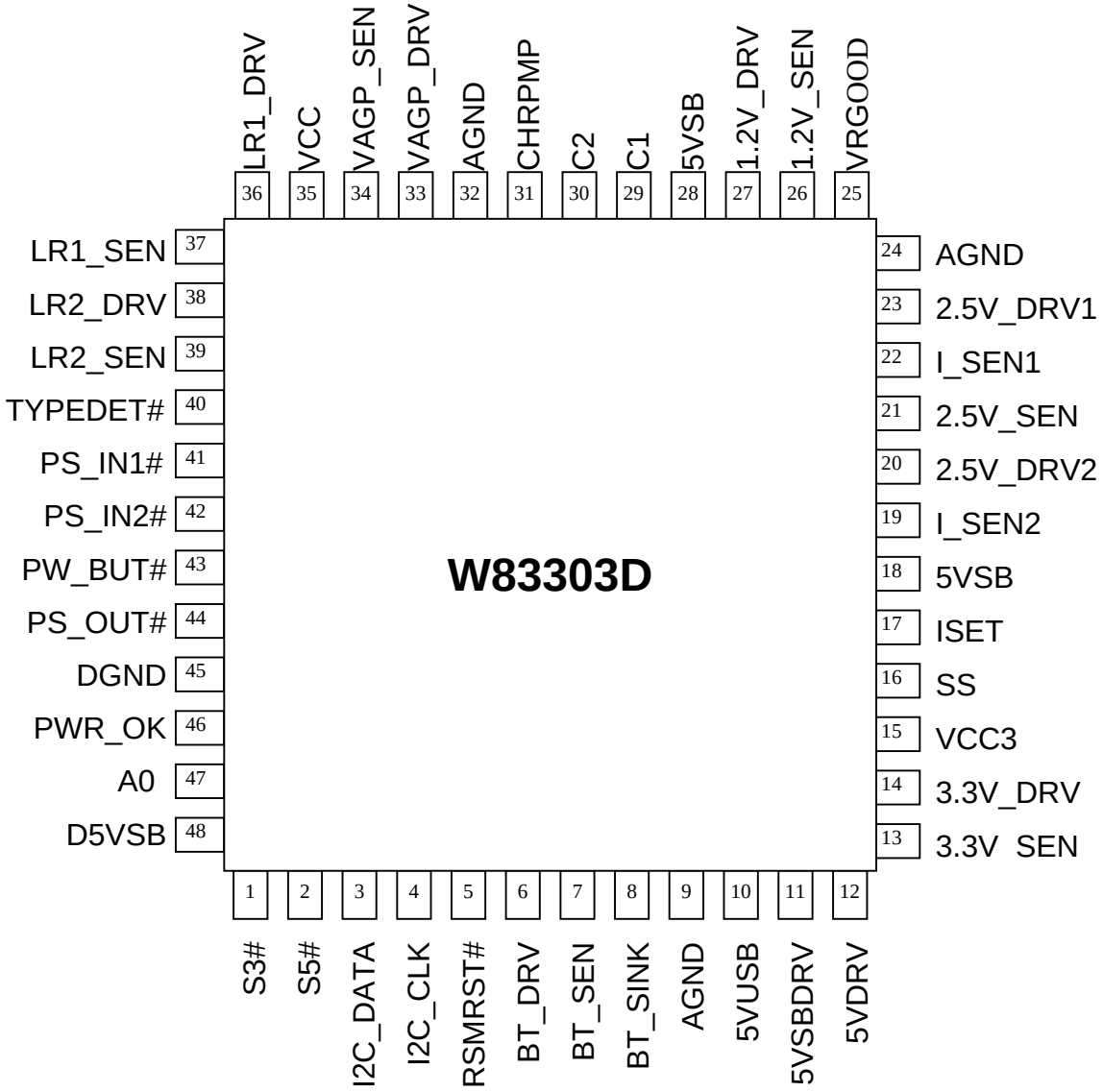
General Function Description

- Provides
  - 5V Active/Sleep ($5V_{DL}$)
  - Programmable $5V_{DL}$/$5V_{STR}$/$5V_{CC}$ for USB Devices
  - 3.3V Active/Sleep ($3.3V_{DL}$)
  - Programmable Two Channel 2.5V Active/Sleep ($2.5V_{STR}$) for DDR
  - Programmable 3.3V/1.5V for AGP 2X/4X/8X Voltage
  - Two Programmable1.25V~5V Linear Regulators for Over-Clocking Application.
  - Programmable 1.25V DDR Bus Termination Regulated Voltage which with Driving and Sinking.
  - 1.2V VCCVID for Intel Northwood CPU
- Supports VRGood signal for Intel Northwood Power Good Control
- Supports RSMRST# Signal Control
- Provides Signals for ATX Power Supply PS_ON# Control
- I2C Interface
- Selectable I2C Address
- Internal Charge Pump Support Up to 9.5VSB
- Drive All N-Channel MOSFET
- Soft Start
- Under-Voltage Monitoring for VAGP, VRAM Channels

W83303D Pinout



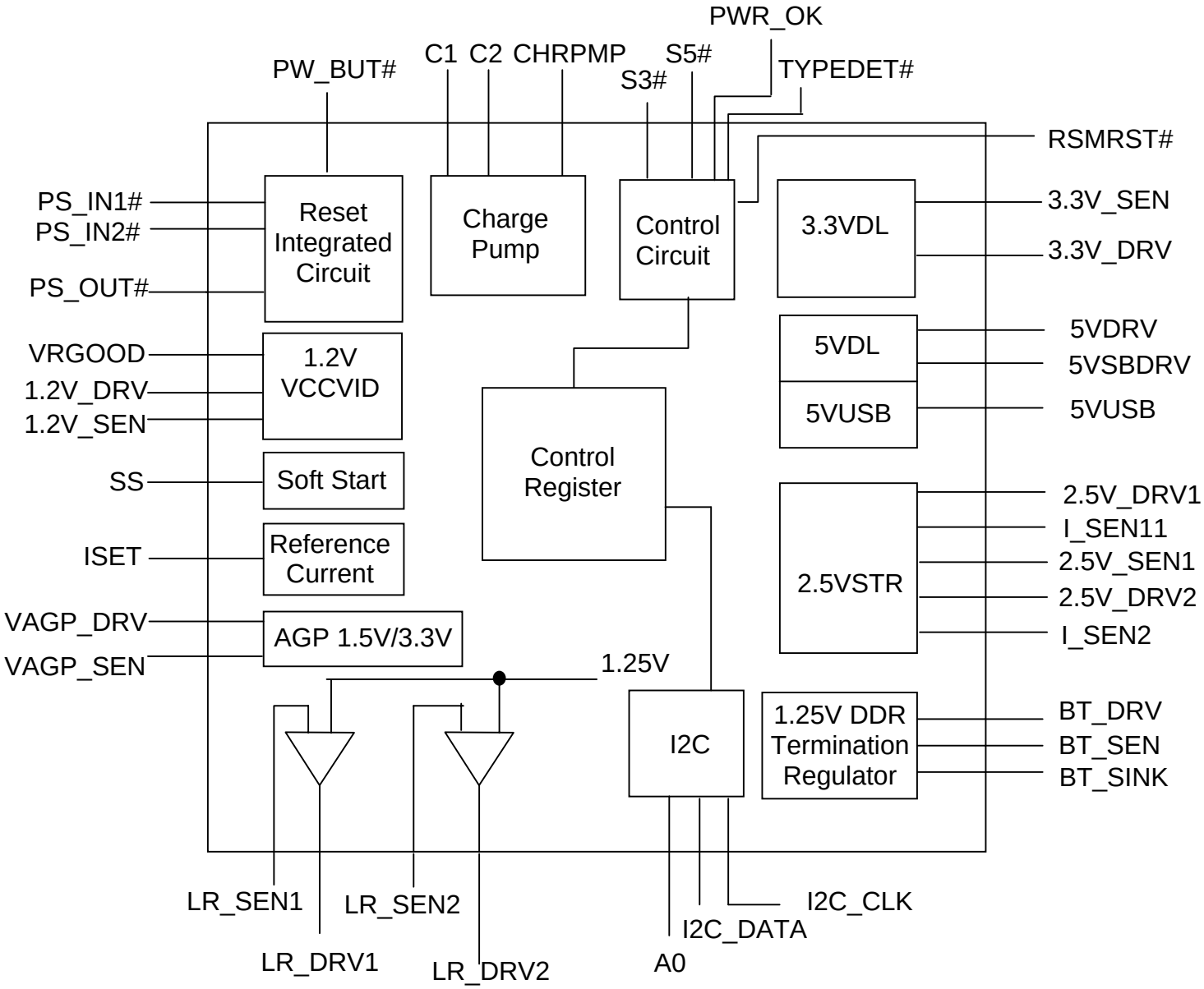
Pin Descriptions

NO	Name	I/O	Function Description
1	S3#	I	ACPI Control Signal
2	S5#	I	
3	I2C_DATA	I/O	I2C Interface, and the ID are defined as 5CH (0101 110X) as well as 5EH (0101 111X), and X is used to control read/write.
4	I2C_CLK	I	
5	RSMRST#	OD	A signal to indicate 5VSB power status. The signal will be issued after 80ms delay when the level of 5VSB higher than 4.3V
6	BT_DRV	O	Regulate a 1.25V for DDR bus termination; two modes is set by CR04
7	BT_SEN	I	
8	BT_SINK	O	
9	AGND	P	Power ground
10	$5V_{USB}$	O	Provide Selectable Voltages-5VDL and 5VUSB; in which the $5V_{USB}$ can programmed by register CR00
11	$5VSB_{DRV}$	O	
12	$5V_{DRV}$	O	
13	3.3V_SEN	I	Generate a 3.3VDL Voltage
14	3.3V_DRV	O	
15	VCC3	P	Power 3.3Vcc
16	SS	I	Soft-Start pin. Attach a capacitor (0.1u) to this pin to determine the soft-start rate; and the slew-rate of SS is set by adjust the capacity of the external capacitor.
17	I_{SET}	I	Attached a specific external resistor to determine the internal reference current.
18	5VSB	P	Power Pin
19	I_SEN2	I	2 channels of $2.5V_{STR}$ output for DDR with internal current sharing design to balance the current on the channels. In which I_SEN1 & I_SEN2 pins should be connected together to 5VSB if only one channel used.
20	2.5V_DRV2	O	
21	2.5V_SEN	I	
22	I_SEN1	I	
23	2.5V_DRV1	O	
24	AGND	P	Power ground
25	VRGOOD	OD	The signal only for the Intel Northwood CPU using to declare the CPU VID status.
26	1.2V_SEN	I	For Intel P4 CPU application; to regulate a 1.2Vcc Voltage for Intel P4 CPU Using.
27	1.2V_DRV	O	
28	5VSB	P	Power Pin
29	C1	I	Charge Pump Pins. It Supports 10mA Driving Current and insures output voltage 9V or above.
30	C2	I	
31	CHRPMP	P	
32	AGND	P	Power Pin
33	VAGP_DRV	O	To regulate a specific voltage 1.5V/3.3V for AGP 2X/4X/8X by TYPEDECT# Pin.
34	VAGP_SEN	I	
35	VCC	P	Power pin

36	LR1_DRV	O	Linear Regulators which range form 1.25V to 5V and adjusted by external resistors
37	LR1_SEN	I	
38	LR2_DRV	O	
39	LR2_SEN	I	
40	TYPEDET#	I	A signal to indicate the type of VGA card inserted in the slot, low means 1.5V for AGP 4X/8X and high means 3.3V for AGP 1X/2X
41	PS_IN1#	I	Provide 2 fault events to shut the ATX power supply down directly by control the PS_ON# signal directly
42	PS_IN2#	I	
43	PW_BUT#	I	
44	PS_OUT#	O	Connect this pin to ATX power supply PS_ON# pin to control power on/off directly
45	DGND	P	Power ground
46	PWR_OK	I	Power good signal of ATX power supply
47	A0	I	A pin to set I2C address
48	D5VSB	P	Power pin

*VRGOOD & TYPEDET# can endure 0-12V level voltage.

Internal Block Diagram



Register Description

CR00 (5VUSB Setting Register, Default 0x00h, Read/Write)
Bit1 and 0 are used to set the output type for corresponding USB devices:

Bit1	**Bit0**	**Condition**	**Power Type**
0	0	S0, S3 state support	S0, S3 state NMOS Q7 turn on
0	1	S0, S3, S5 state support	S0, S3, S5 state NMOS Q7 turn on
1	0	S0 state support	S0 state NMOS Q7 turn on

CR01 (V_{AGP} Over-clocking Configuration Register, Default 0x00h, Read/Write)
Bit7 is TYPEDET# Setting (Bit 1 and 2 are not valid when Bit7 is high)
Bit6~2 are reserved
Bit1 and 0 are used to set output voltage of AGP 4X/8X for over-clocking application:

Bit1	**Bit0**	**V_{AGP} Output (V)**
0	0	1.5
0	1	1.6
1	0	1.7
1	1	1.8

CR02 (V_{RAM} Over-clocking Configuration Register, Default 0x00h, Read/Write)
Bit2, 1 and 0 are used to set output voltage of V_{RAM} for over-clocking application:

Bit2	**Bit1**	**Bit0**	**V_{RAM} Output (V)**
0	0	0	2.5
0	0	1	2.6
0	1	0	2.7
0	1	1	2.8
1	0	0	2.9
1	0	1	3.0

CR03 (V_{LR} Over-clocking Configuration Register, Default 0x00h, Read/Write)
Bit2, 1 and 0 are used to set output voltage of V_{LR1} (Linear Regulator 1) for over-clocking application:

Bit2	**Bit1**	**Bit0**	**Increase percentage (%)**
0	0	0	0
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	12
1	0	1	16

CR04 (V_{BT} Mode Configuration Register, Default 0x00h, Read/Write)

Bit0 is used to set the track mode of bus termination regulator

Bit0	V_{BT}
0	V_{BT} Tracking with VRAM_2.5
1	Fix in 1.25V

CR05 (Linear Under Voltage setting)

Bit0, 1 and 2 are used to enable/disable LUV protection.

Bit0	**1/0**	Enable/disable VAGP LUV, default value=1
Bit1	**1/0**	Enable/disable VRAM2.5 LUV, default value=1
Bit2	**1/0**	Enable/disable Dual3.3V LUV, default value=0

Electrical Specification

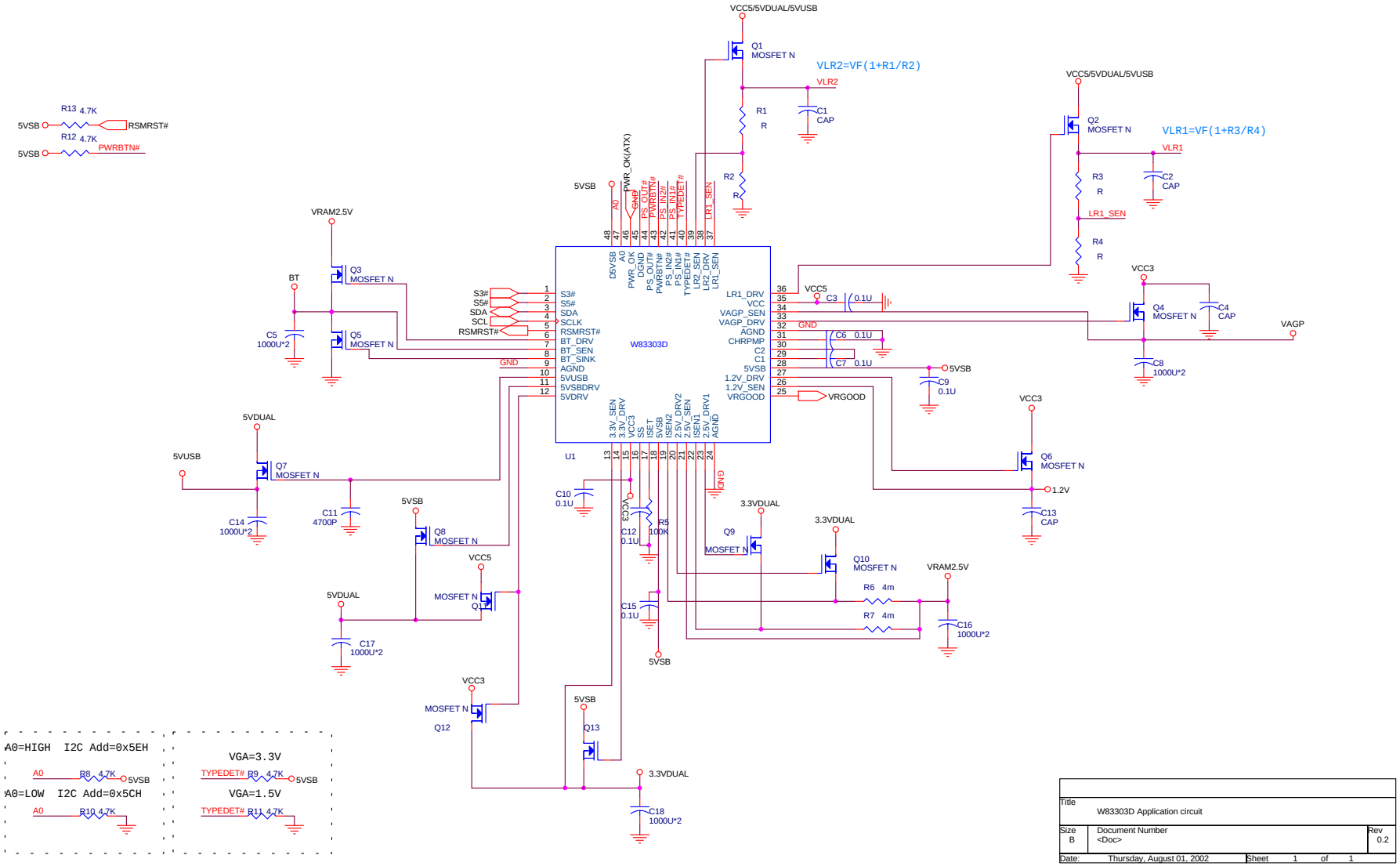
AC CHARACTERISTICS

Vcc=5V ± 5 %, T_A = 0°C to +70°C						
Parameter	**symbol**	**Min**	**Typ**	**Max**	**Units**	**Test Conditions**
VAGP Linear Regulator / Switch						
Nominal Output Voltage			1.5		V	CR01(bit1,bit0)=00
Nominal Output Voltage			1.6		V	CR01(bit1,bit0)=01
Nominal Output Voltage			1.7		V	CR01(bit1,bit0)=10
Nominal Output Voltage			1.8		V	CR01(bit1,bit0)=11
Regulation				5	%	
Under-Voltage Falling Threshold			66.67		%	
VAGP_DRV Output Voltage		8			V	CR0F=80h I(VAGP_DRV) < 0.1mA
Vref Voltage Reference						
Nominal Output Voltage		1.21	1.25	1.29		I_{load} < 1mA
1.2V Linear Regulator						
Nominal Output Voltage		1.14	1.2	1.26	V	
VRGood delay			2		mS	After 1.2V_SEN>1.1V
VRAM2.5 Regulator						
Nominal Output Voltage			2.5		V	CR02(bit2,bit1,bit0)=000
Nominal Output Voltage			2.6		V	CR02(bit2,bit1,bit0)=001
Nominal Output Voltage			2.7		V	CR02(bit2,bit1,bit0)=010
Nominal Output Voltage			2.8		V	CR02(bit2,bit1,bit0)=011
Nominal Output Voltage			2.9		V	CR02(bit2,bit1,bit0)=100
Nominal Output Voltage			3.0		V	CR02(bit2,bit1,bit0)=101
Regulation				5	%	
Under-Voltage Falling Threshold			72		%	
MAX VRAM_2.5_DRV Output Voltage		9			V	I(VRAM_2.5_DRV) < 0.1mA
Increase percentage of Linear Regulator _1 output voltage (%)						
Nominal Output Voltage			0		%	CR03(bit2,bit1,bit0)=100
Nominal Output Voltage			2		%	CR03(bit2,bit1,bit0)=101
Nominal Output Voltage			4		%	CR03(bit2,bit1,bit0)=100
Nominal Output Voltage			8		%	CR03(bit2,bit1,bit0)=101
Nominal Output Voltage			12		%	CR03(bit2,bit1,bit0)=100
Nominal Output Voltage			16		%	CR03(bit2,bit1,bit0)=101

AC CHARACTERISTICS(Cont's)

Bus Termination Regulator						
Nominal Output Voltage / V(VRAM2.5_SEN)			50		%	CR04(bit0)=0 VBT Tracking with VRAM_2.5
Nominal Output Voltage			1.25		V	CR04(bit0)=1
5VDUAL Switch Controller						
5VDRV Output High Voltage		9				Cap Loading
5VSBDRV Output High Voltage		9				Cap Loading
5VUSB Output High Voltage		9				Cap Loading
5VUSB SS Sourcing Current			2.5		uA	@ Soft-start
3.3 Dual						
Under-Voltage Falling Threshold			66.67		%	
MAX VRAMDRV2 Output Voltage		9			V	CR10=C0h, S0 state, I(VRAMDRV2) < 0.1mA
Charge Pump						
Charge Pump Frequency			200		KHz	
Charge Pump Voltage		9.5				

Application Circuit



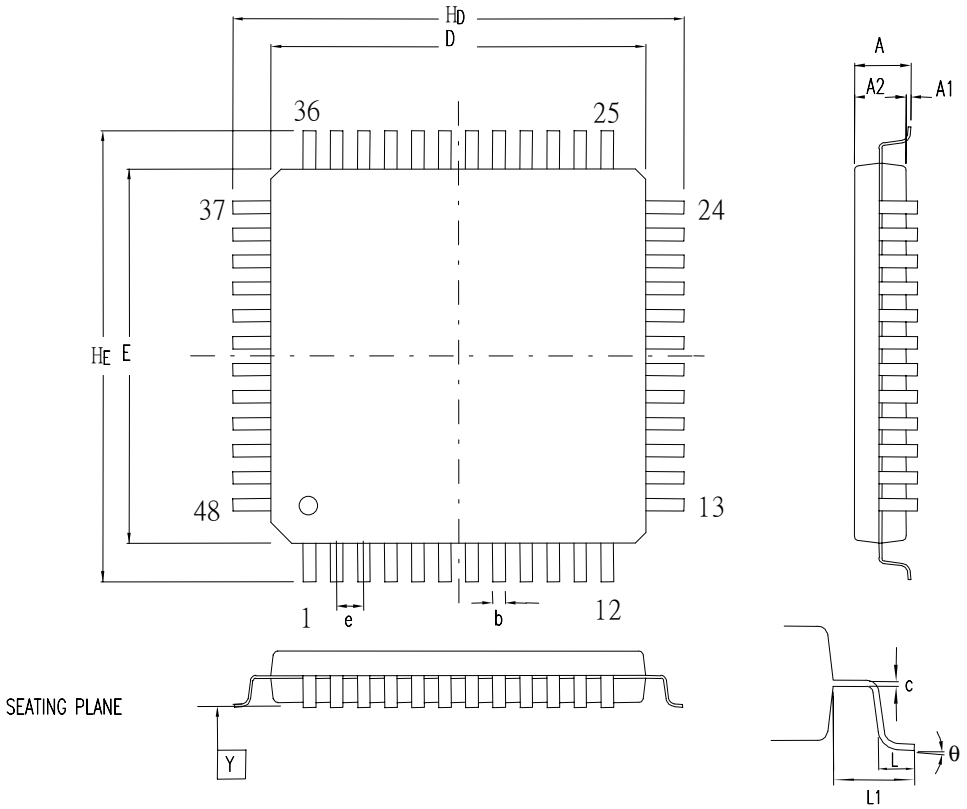
Ordering Instruction

PART NO.	PACKAGE	REMARKS
W83303D	48-pin LQFP	

How to Read the Top Marking

1st Line: Winbond Logo
2nd Line: Part_No W83303D
3rd Line: Date Code (XXX) + Assembly House Code (X) + Chip Version (XXX)

Package Dimension



Controlling dimension : Millimeters

Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	—	—	—	—
A_1	0.002	0.004	0.006	0.05	0.10	0.15
A_2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.006	0.008	0.010	0.15	0.20	0.25
c	0.004	0.006	0.008	0.10	0.15	0.20
D	0.272	0.276	0.280	6.90	7.00	7.10
E	0.272	0.276	0.280	6.90	7.00	7.10
e	0.014	0.020	0.026	0.35	0.50	0.65
H_D	0.350	0.354	0.358	8.90	9.00	9.10
H_E	0.350	0.354	0.358	8.90	9.00	9.10
L	0.018	0.024	0.030	0.45	0.60	0.75
L_1	—	0.039	—	—	1.00	—
Y	—	—	0.004	—	—	0.10
θ	0°	—	7°	0°	—	7°

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