Winbond Advanced ACPI Controller W83303D Application Note V1.62

1 For bus termination regulator application, two beforehand capacitors (C1 and C2 in Fig.1) for both sinking and driving gates are advised to prevent somehow noise interference in bus termination regulator.

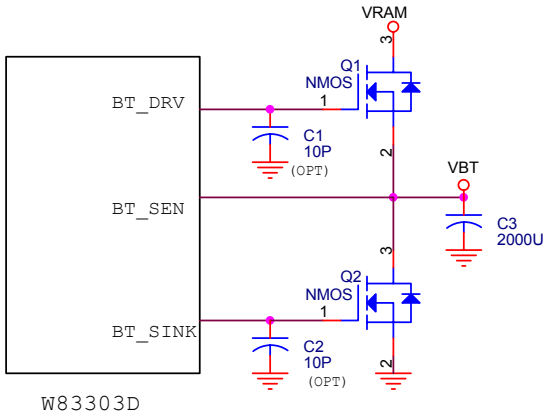
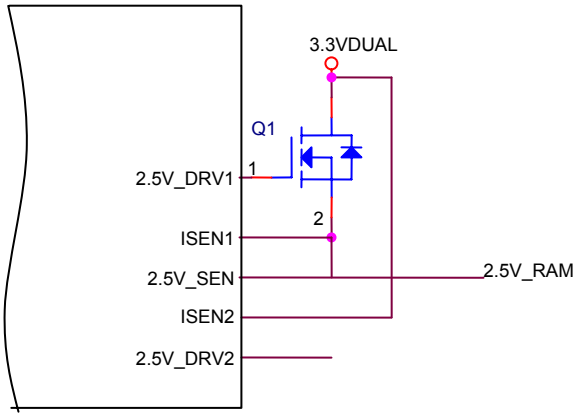


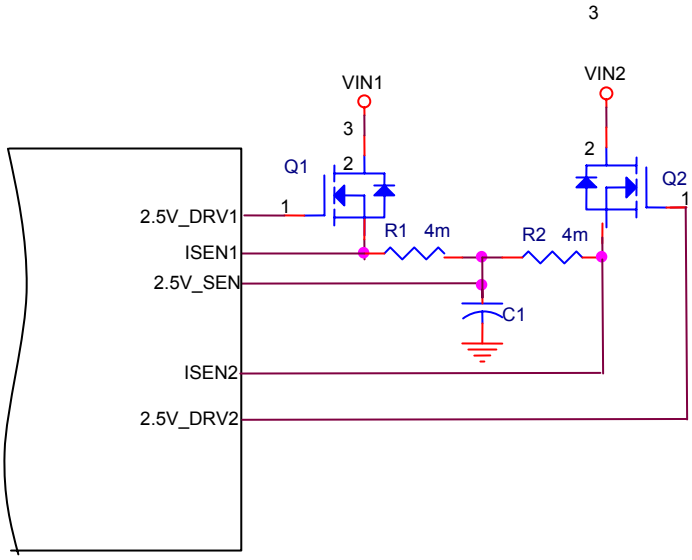
Figure.1

2 The W83303D provides a specific dual-channels 2.5V_{RAM} voltage for DDR application, and the V_{RAM} voltage is with a current balancing technology and can support over 10Amp continuous current application. On the other hand, the 2.5V_{RAM} can apply with single channel with lower loading application (<5Amp). The specific circuits of applications are shown as following.

2.1 For lower loading application (<5Amp)



2.2 For higher loading application (>5Amp), the dual-channels with current balancing technology will be advised.



3 With dual channels application, the different power source can be applied such as V_{IN1}=5V and V_{IN2}=3.3V for some power consideration; but the thermal issue between the two MOSFETs should be considered and can be adjusted by the ratio of R1/R2. For equal power consumption on the both MOSFETs, the following equations are described about the power

$$P_{Q1}=I_1*(V_{IN1}-V_{RAM}) = I2*(V_{IN2}-V_{RAM}) = P_{Q2} \Rightarrow I_1/I_2=(V_{IN2}-V_{RAM})/(V_{IN1}-V_{RAM})=R2/R1$$

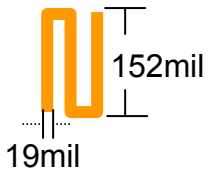
- The two 4mΩ (4~8mΩ) resistors for dual-channels V_{RAM} application can be implemented by simple PCB traces. The following information can apply for the trace design reference.
- Resistance calculation:
  - The typical resistance of 1Oz. PCB track is 0.34mΩ/square; and 2Oz. PCB track is 0.17mΩ/square.
- Trace width determination:

Loading		Continuous 5Amp		Continuous 7Amp	
Outer PCB Track		1 Oz.	2 Oz.	1 Oz.	2 Oz.
Temperature Rising	60°C	Width=37mil	19 mil	60 mil	30 mil
	70°C	34 mil	17 mil	54 mil	27 mil
	80°C	31 mil	16 mil	50 mil	25 mil

For example, if a 4mΩ/2Oz./Continuous Loading=5Amp/ Rising Temperature=60°C spec. is implemented; the size of PCB will be calculated by following equation and figure.

$$4m\Omega \div 0.17\,{}^{m\Omega}\!/_{square} = 24square$$

$$trace\_length = 24\times = 19mil \times 456mil$$

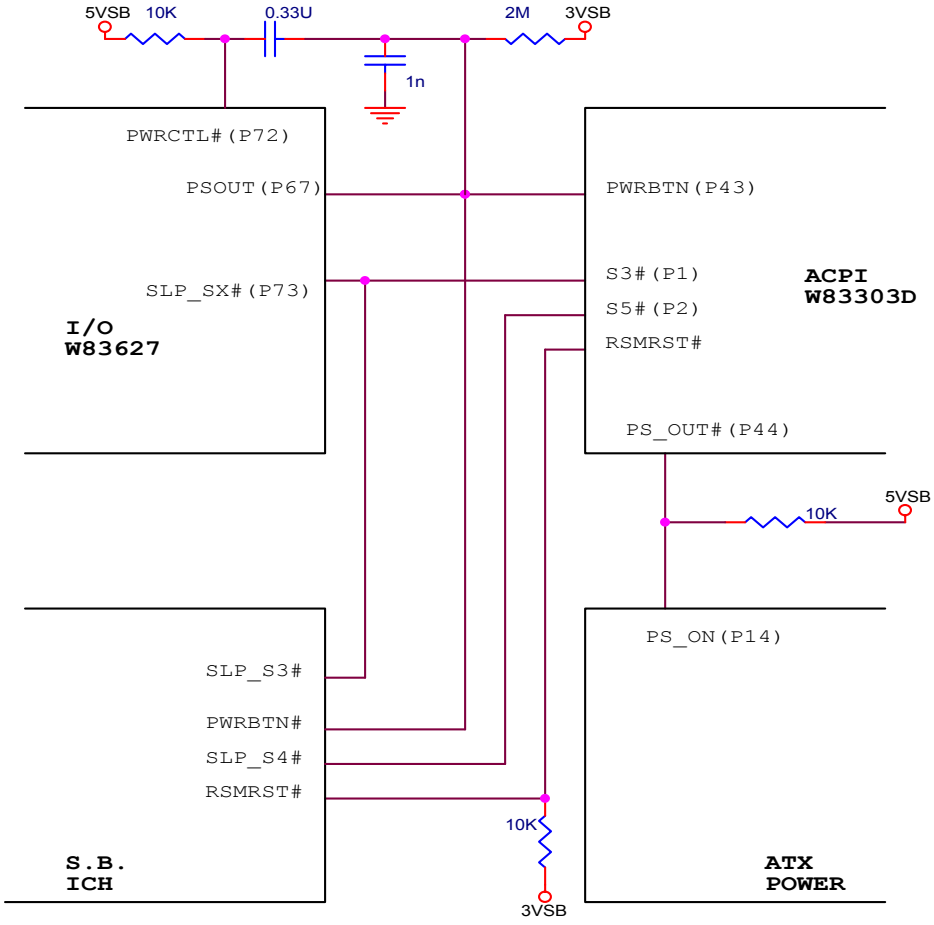


As our suggestion the 4mΩ resister can be implemented with

1 2Oz. PCB Track 30mil X 706mil
2 1Oz. PCB Track 60mil X 706mil
3 0.5OZ. PCB Track 120mil X 706mil

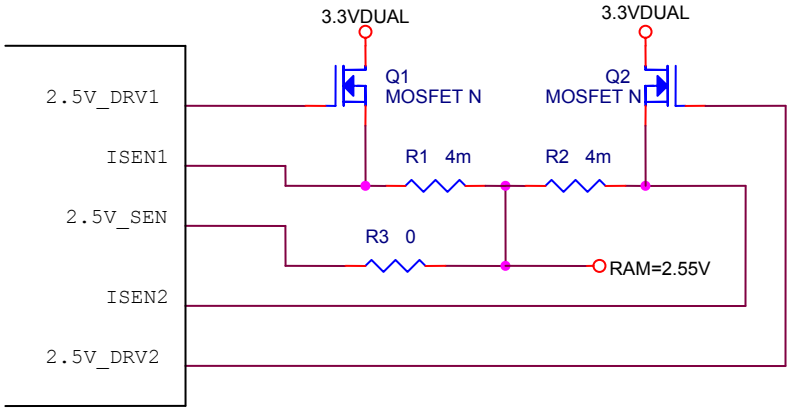
4 As the AGP voltage setting, to avoid mis-setting the AGP voltage to 3.3V when the graphic card is not properly inserted in slot, we suggest that connect one 100kΩ pull down resister to TYPEDETC# on mother board to force the AGP voltage to 1.5V when TYPEDECT# is opened.

5 With some W83303D functions, the signals of PS_ON#, S3#, and PWRBTN# are needed for power control between W83303D, Super IO, South Bridge and ATX power supply. The relationship of implementation is shown as following figure,



6 A 4.7KΩ resister which pulled high to $5V_{SB}$ should be attached on pins of PS_IN1#, and PS_IN2#.

7 The pin22 (2.5V_SEN) input current is about 0.486mA.



8 For Intel ICH4, and ICH5 platform, the pin S5# should be connected to South Bridge SLP_S4#.

9 W83303D spec. change from VER. C to VER. E.

9.1 The default output voltage of two linear regulators is updated from 1.25V to 1.20V. And can be ranged from 1.20V to 5.00V by external resisters adjustment.

9.2 The default status of 5VUSB is updated from $5V_{STR}$ to $5V_{DL}$, and the configuration table is also updated as following table.

Bit1	Bit0	5VUSB Condition
0	0	S0, S3, S5 state support
0	1	S0, S3 state support
1	1	S0 state support

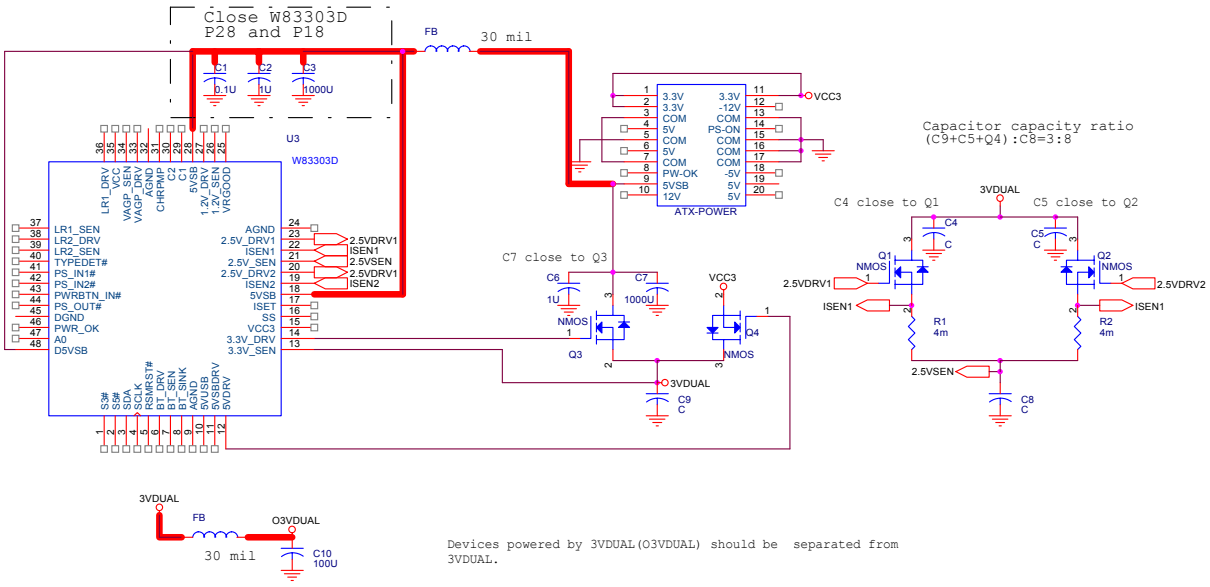
9.3 The default voltage of V_{AGP} is changed from 1.5V to 1.55V, and the voltage table of the output is updated as following table.

Bit1	Bit0	VAGP Voltage
0	0	1.55V
0	1	1.50V
1	0	1.60V
1	1	1.65V

9.4 The default voltage of V_{RAM} is updated from 2.5V to 2.55V, and the voltage table of the output is updated as following table.

Bit2	Bit1	Bit0	VRAM voltage
0	0	0	2.55V
0	0	1	2.50V
0	1	0	2.60V
0	1	1	2.65V
1	0	0	2.70V
1	0	1	2.80V

10 In the earlier stage of system power on, the V_{RAM} is regulated from $3.3V_{SB}$ power and following with soft-start of W83303D; meanwhile, the standby power is too weak to supply for the output device with too large capacitors. Therefore the capacitors' ratio of the standby power to output device should be took care for this issue, and 3:8 is recommended as experience. Another way to prevent from this phenomenon, a layout as shown as following should be took care to separate the interference on standby power.



11 How to read top marking

1st Line: Winbond Logo
2nd Line: Part No. W83303D
3rd Line: Production track code (XXXXXXXX)
4th Line: Date Code (XXX) + Assembly House Code (X) + Chip Version (XXX)

W83303D Application Notice Version History

	Date	Version	Remark
1	9/20/2002	1.00	■ Application Circuit Recommendation
2	11/27/2002	1.50	■ Adjust V_{RAM} 2.5V to 2.55V
3	01/23/2003	1.51	■ S5# signal connect to ICH4/5, slp_s4#. Please refer to item 5.
4	02/17/2003	1.60	■ Spec. change from VER. C to VER. D. See Item 7 and 9.
5	03/04/2003	1.61	■ Version change to E
6	03/13/2003	1.62	■ Layout guide for V_{RAM} with $3V_{DUAL}$.