

R33 INTEL UMA/DISCRETE SYSTEM DIAGRAM

01

+3V/+5V S5
PG.35

+1.05V_VTT
PG.38

CPU Core
PG.40~41

DDR3
PG.37

VCCSA
PG.36

Charge
PG.34

Dis-Charge
PG.39

+VGACORE
PG.42

+1.0V_VGA
PG.43

SODIMM1
Max. 4GB
PG.12

SODIMM2
Max. 4GB
PG.13

INTEL IVY
37.5mm X 37.5mm
989pin PGA
TDP 35W
PG.2-5

AMD Thames XT
29mm X 29mm
TDP 25W
PG.14-20

VRAM
128Mx16x8,128bit
PG.21-22

HDD
PG.32

ODD
PG.32

INTEL PCH Panther Point
PG.6-11

USB3.0 Ports X2
PG.28

Webcam
PG.23

PCI-E x 1

LANE2 LANE1

LAN
RTL8105EH
10/100
PG.29

WLAN BT COMBO
PG.33

USB 2.0
PORT10

PCI-E x 1

LANE3

Accelerometer
PG.33

Card Reader
RTS5229
PG.26

KBC
EnE KB3930QF A2
PG.30

SMBUS LPC

KB PG.31

TP PG.31

ROM PG.30

FAN PG.32

AUDIO CODEC
IDT 92HD87
ICT
PG.27

Speaker
PG.27

HP/MIC
PG.28

Analog MIC
PG.28

HDMI
PG.25

CRT
PG.24

LVDS
PG.23

Stackup

TOP

GND

IN1

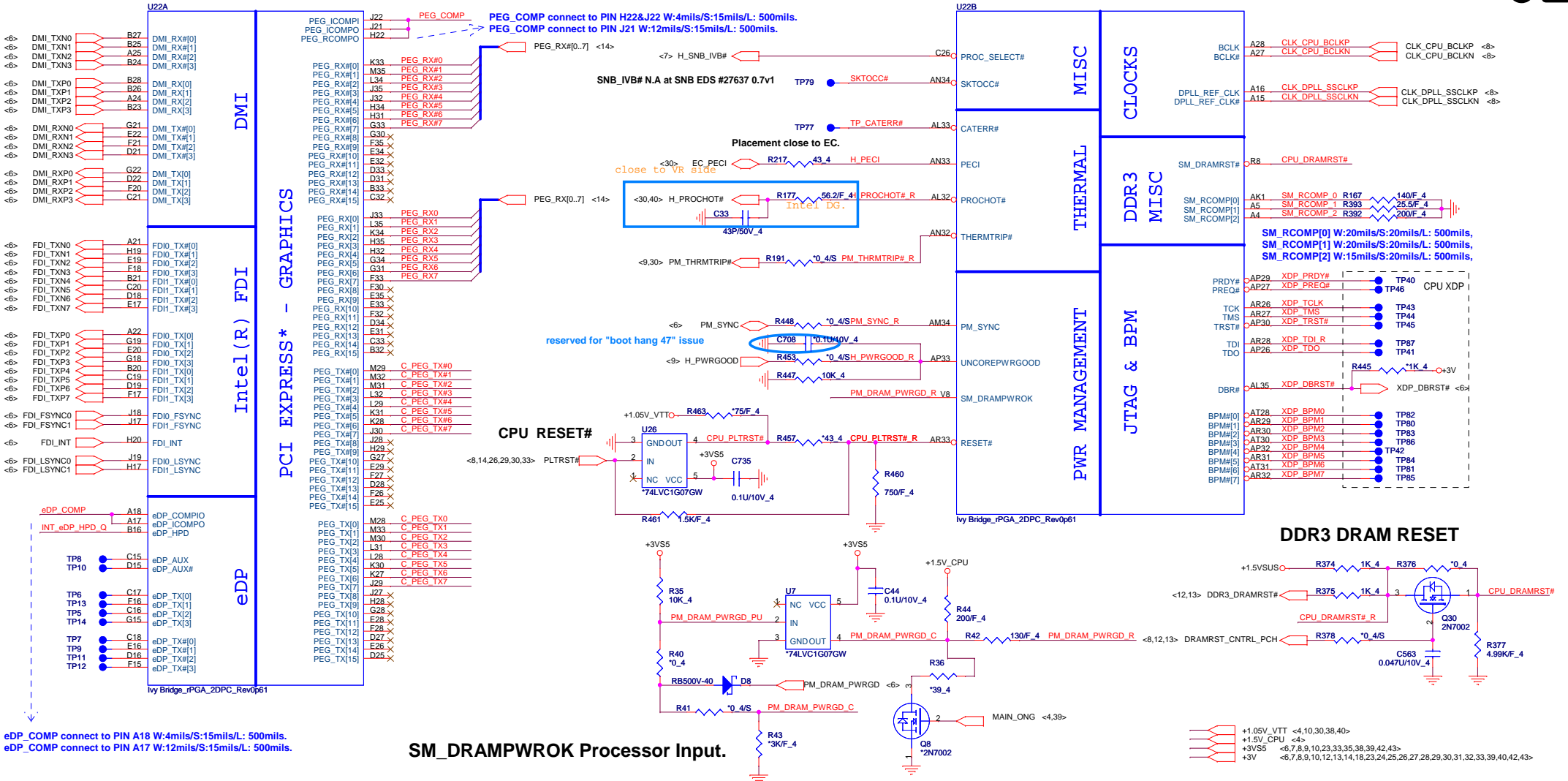
IN2

VCC

BOT



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FDI disable (DIS only stuff)

DEL

FDI_FSYNC can gang all these 4 signals together and tie them with only one 1K resistor to GND (DG V0.5 Ch2.2.9).

PEG x16 disable (UMA only remove)

C PEG TX0	C596	0.1u/10V	4	PEG TX0	C PEG TX#0	C599	0.1u/10V	4	PEG TX#0
C PEG TX1	C600	0.1u/10V	4	PEG TX1	C PEG TX#1	C602	0.1u/10V	4	PEG TX#1
C PEG TX2	C603	0.1u/10V	4	PEG TX2	C PEG TX#2	C605	0.1u/10V	4	PEG TX#2
C PEG TX3	C607	0.1u/10V	4	PEG TX3	C PEG TX#3	C614	0.1u/10V	4	PEG TX#3
C PEG TX4	C617	0.1u/10V	4	PEG TX4	C PEG TX#4	C618	0.1u/10V	4	PEG TX#4
C PEG TX5	C619	0.1u/10V	4	PEG TX5	C PEG TX#5	C622	0.1u/10V	4	PEG TX#5
C PEG TX6	C623	0.1u/10V	4	PEG TX6	C PEG TX#6	C627	0.1u/10V	4	PEG TX#6
C PEG TX7	C632	0.1u/10V	4	PEG TX7	C PEG TX#7	C640	0.1u/10V	4	PEG TX#7

0.22uF AC coupling Caps for PCIE GEN1/2/3

DP & PEG Compensation

check

+1.05V_VTTO R59 10K 4 INT_eDP_HPD_Q

+1.05V_VTTO R395 24.9F 4 eDP_COMP

eDP_ICOMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

+1.05V_VTTO R97 24.9F 4 PEG_COMP

PEG_ICOMPI and RCOMPO signals should be routed within 500 mils typical impedance = 43 mohms PEG_ICOMPO signals should be routed within 500 mils typical impedance = 14.5 mohms

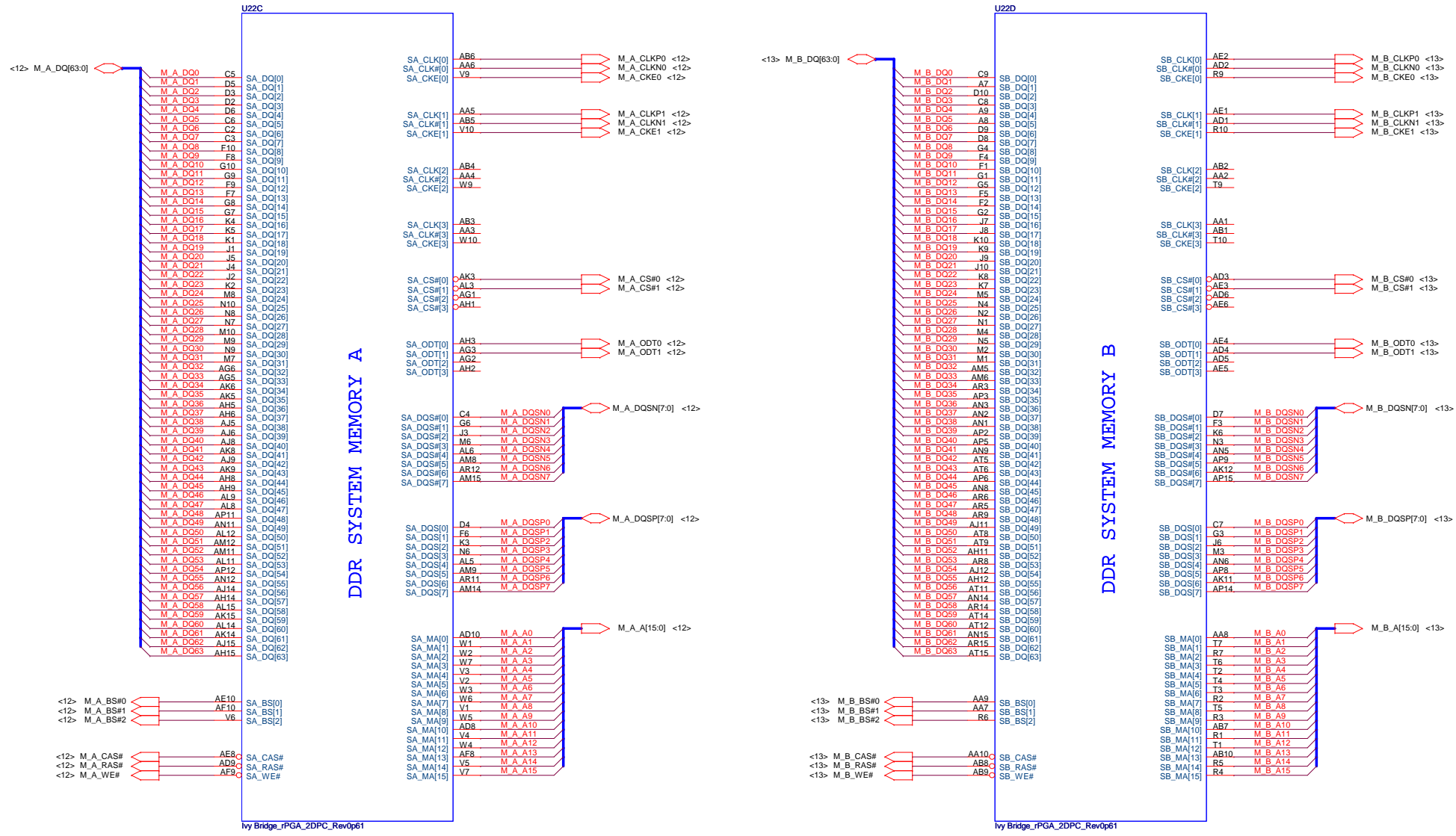
Processor pull-up (CPU)

H PROCHOT#	R176	62	4
XDP_TDO	R186	51	4
XDP_TMS	R189	51	4
XDP_TDI_R	R462	51	4
XDP_PREQ#	R188	51	4
XDP_TCLK	R187	51	4
XDP_TRST#	R190	51	4

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Size Custom	Document Number SNB 1/4 (PCIE&DMI&FDI)	Rev 1A
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Ivy Bridge Processor (DDR3)

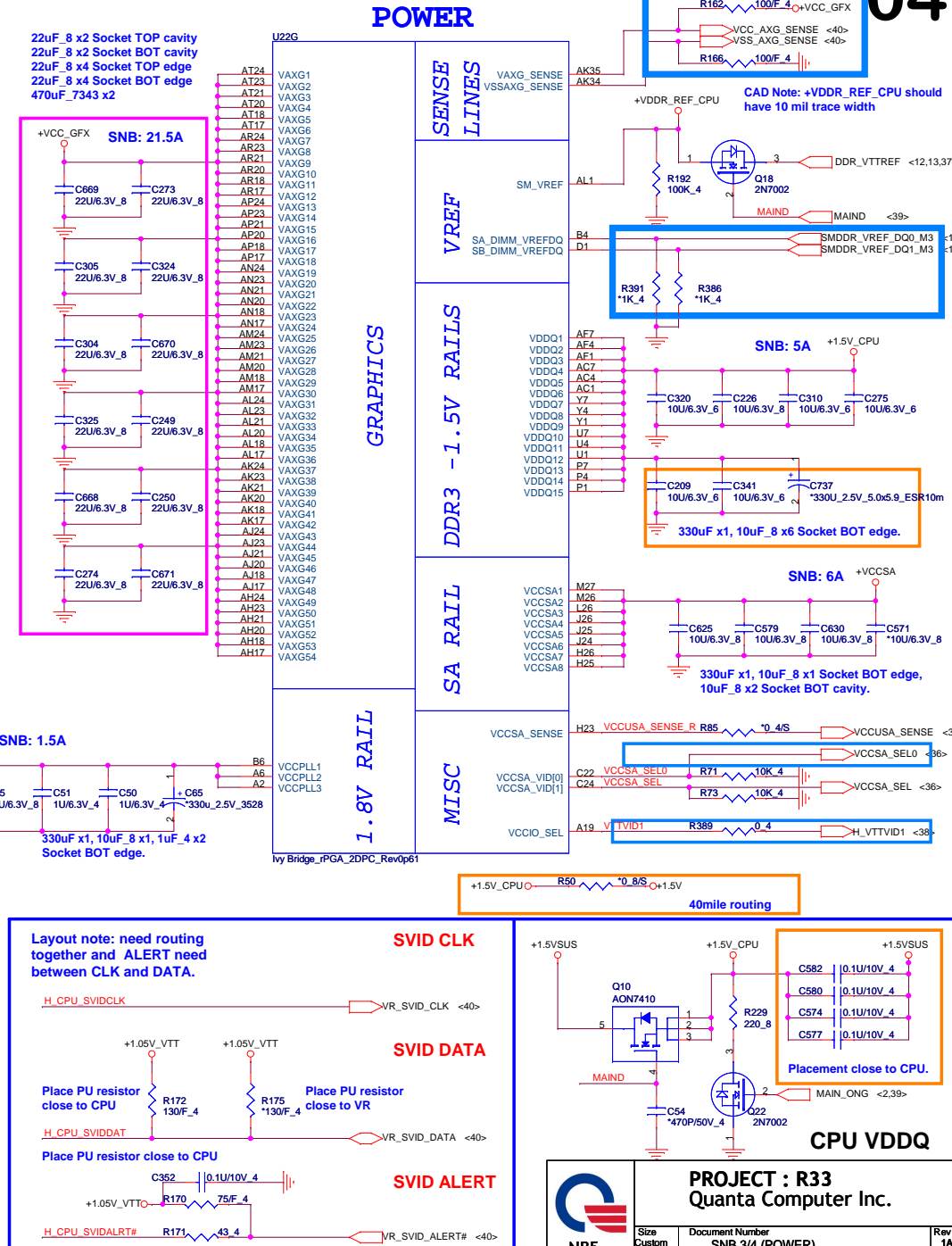
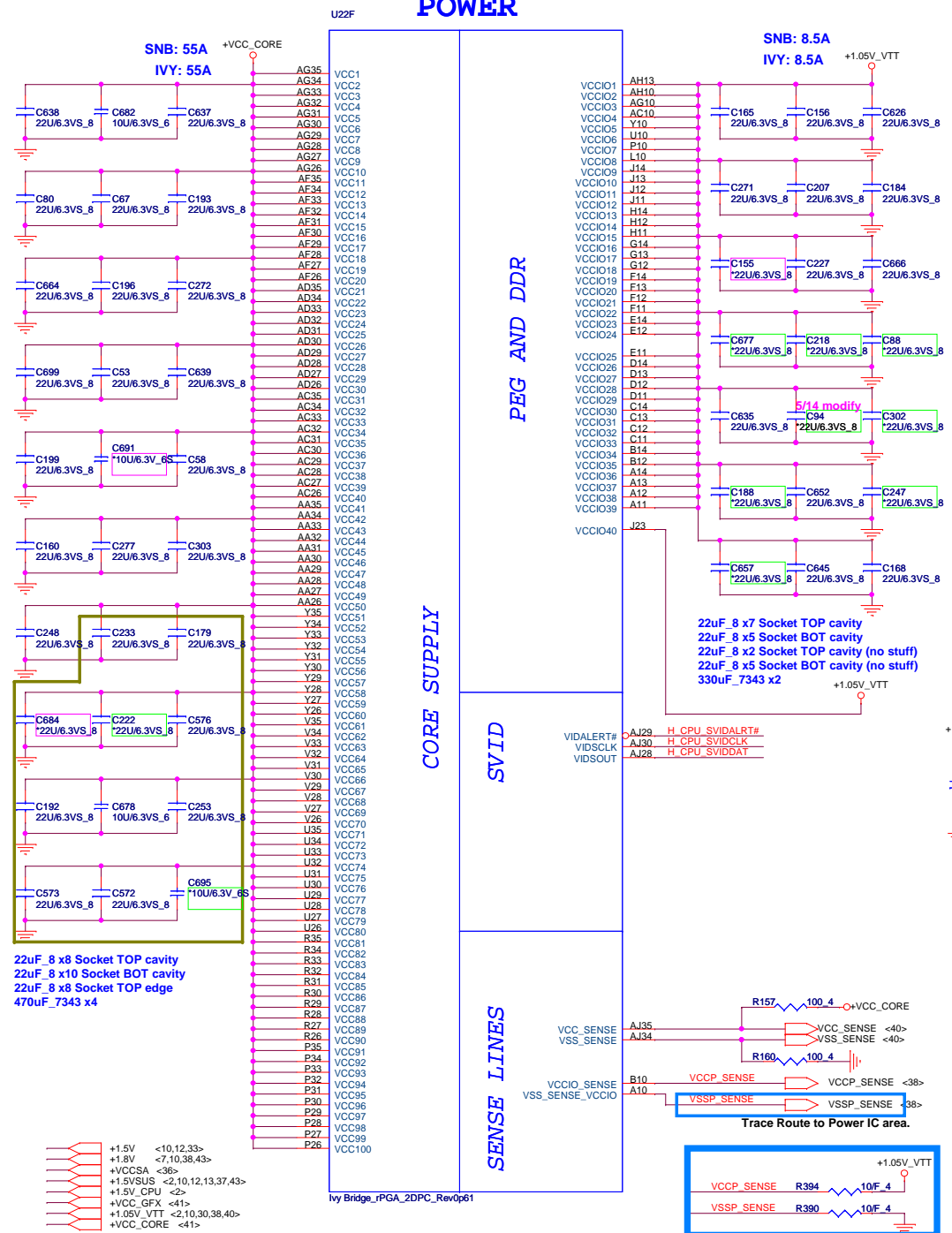


	PROJECT : R33		Rev 1A
	Quanta Computer Inc.		
	Size Custom	Document Number SNB 2/4 (DDR3 I/F)	
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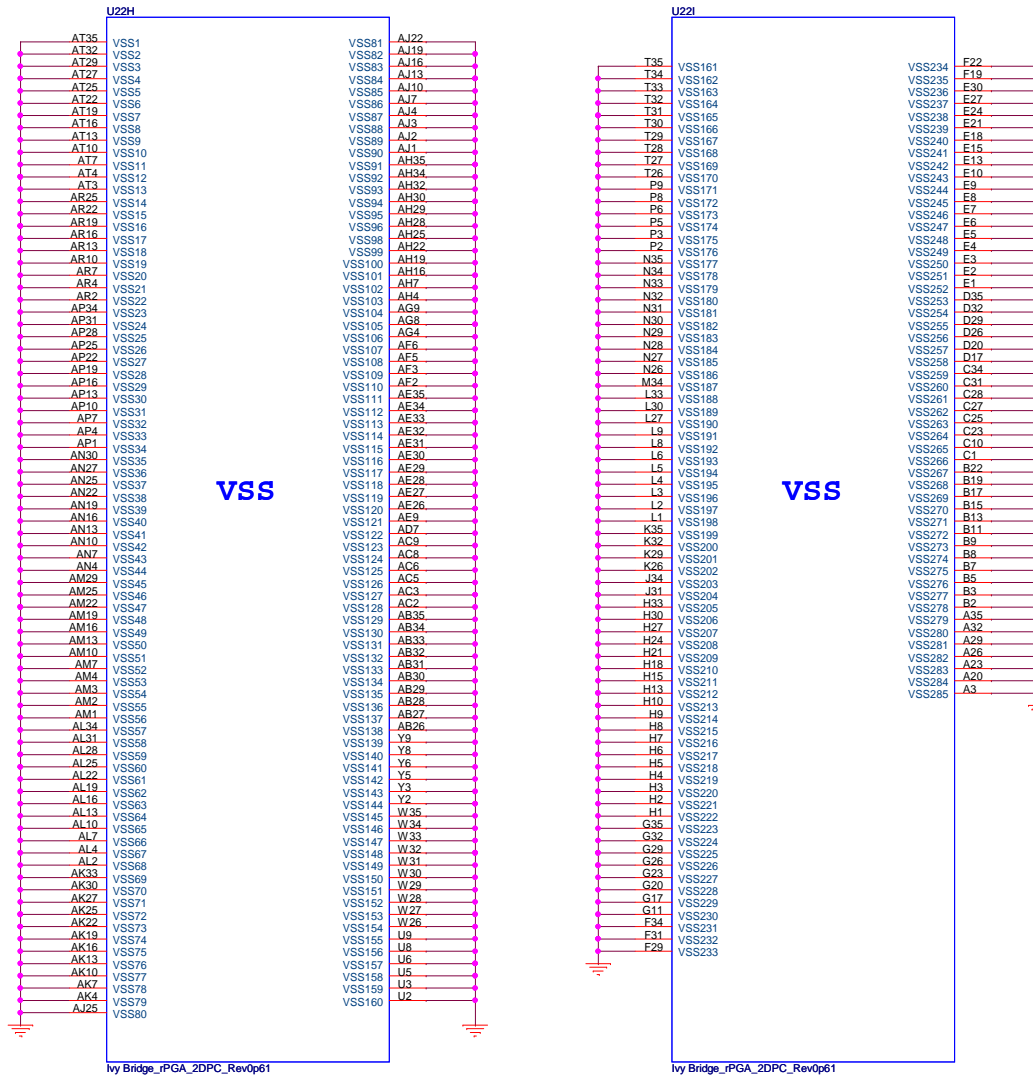
Ivy Bridge Processor (POWER)

POWER

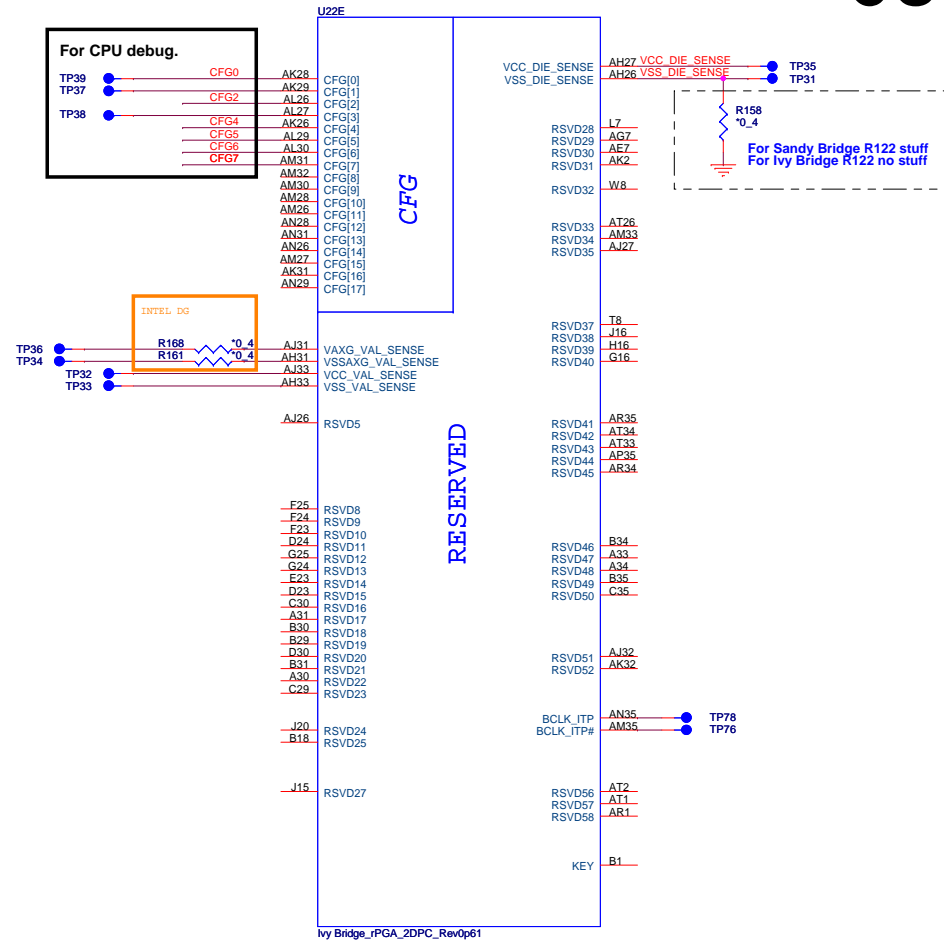
POWER



Ivy Bridge Processor (GND)



Ivy Bridge Processor (RESERVED, CFG)

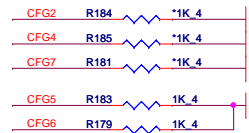


For rPGA socket, RSVD59 pin should be left NC.

Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training



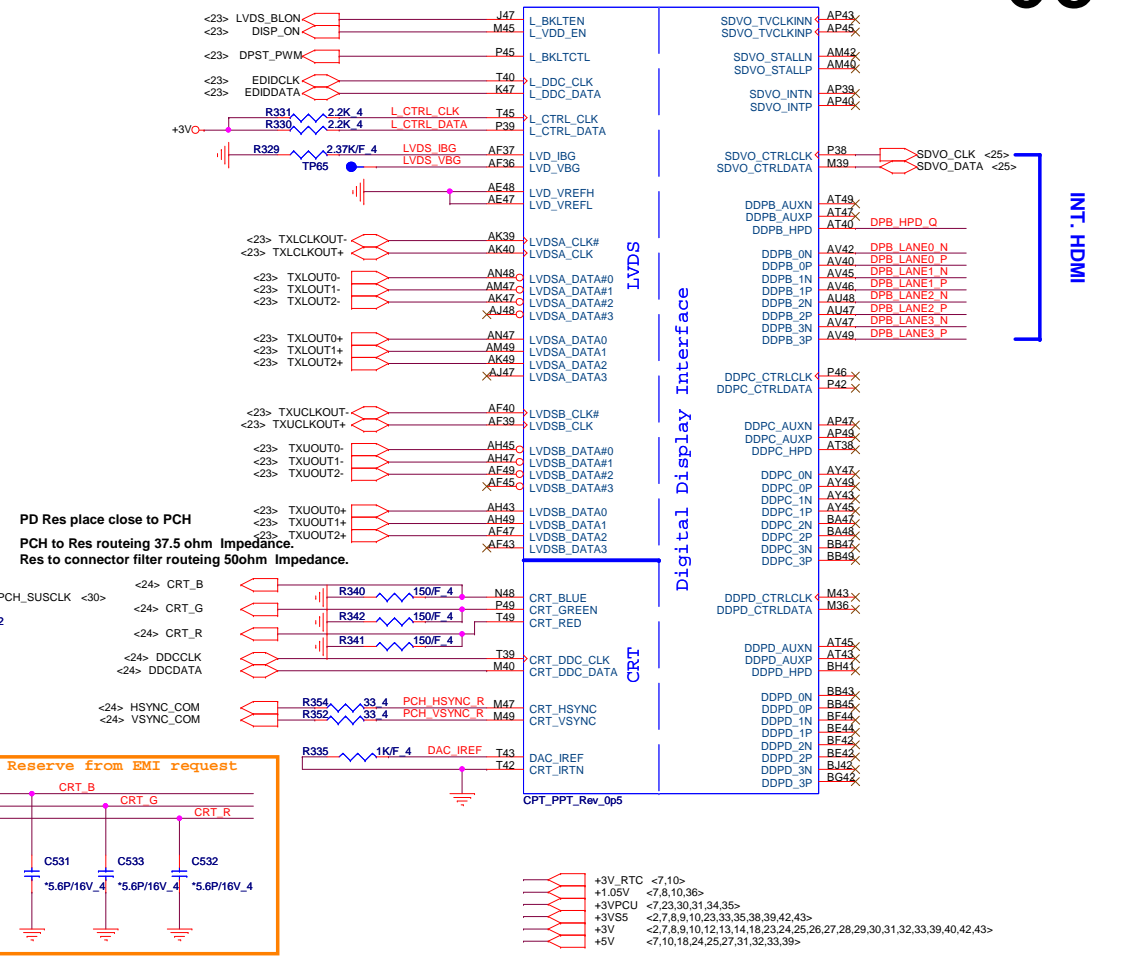
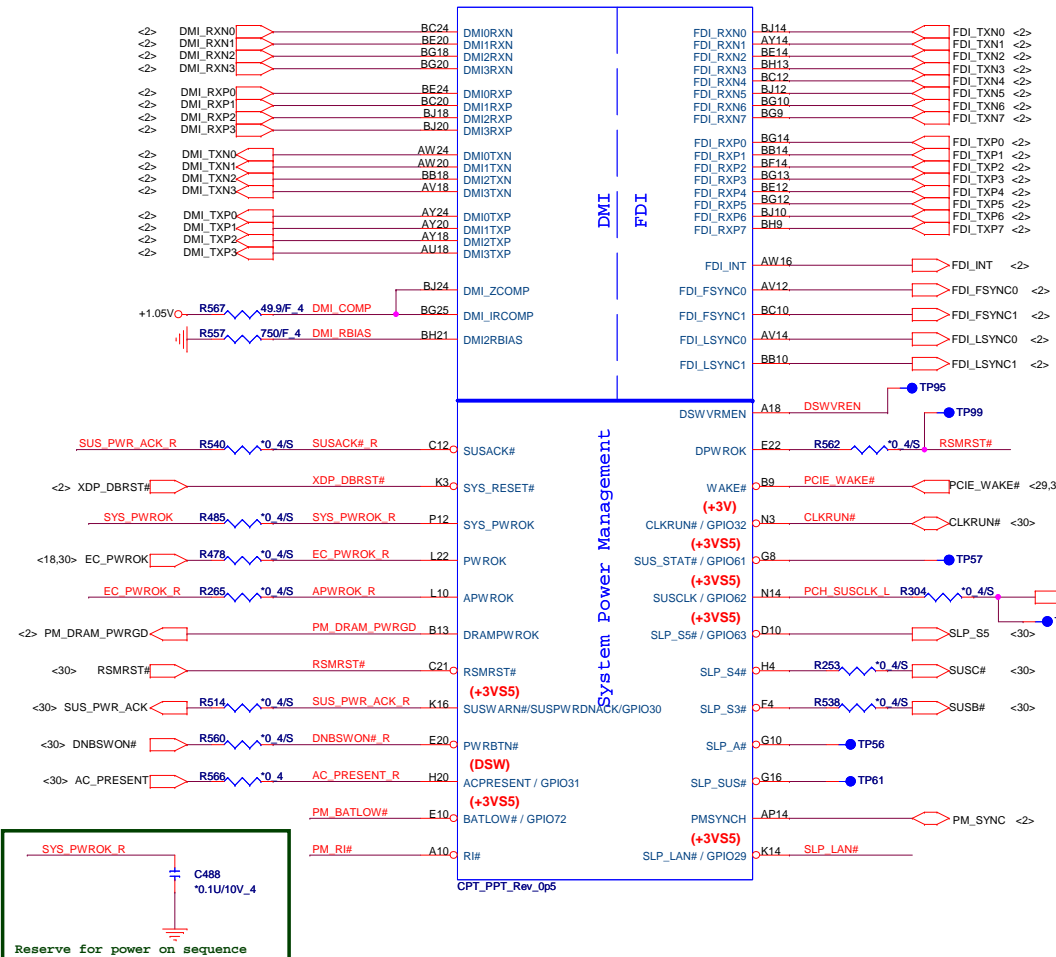
CFG[6:5] (PCIe Port Bifurcation Straps)
 11: (Default) x16 - Device 1 functions 1 and 2 disabled
 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
 00: x8, x4, x4 - Device 1 functions 1 and 2 enabled

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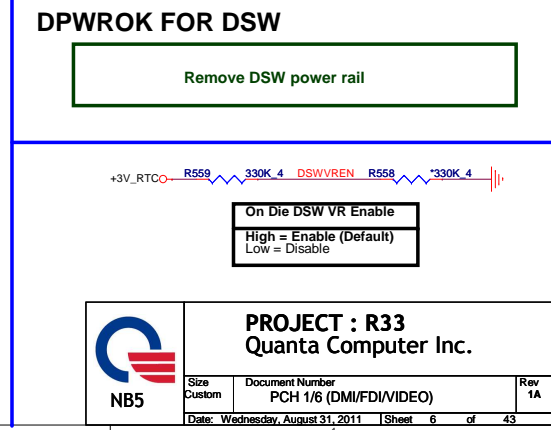
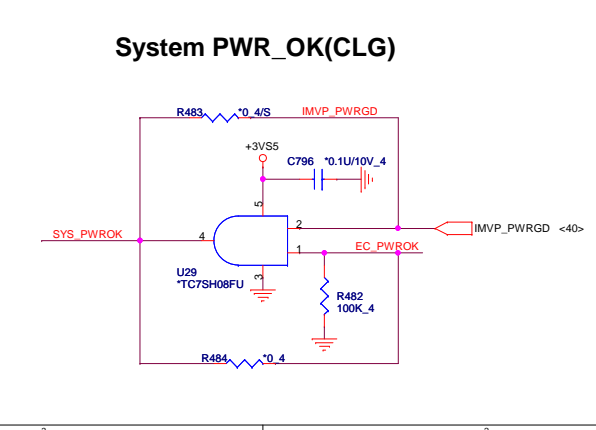
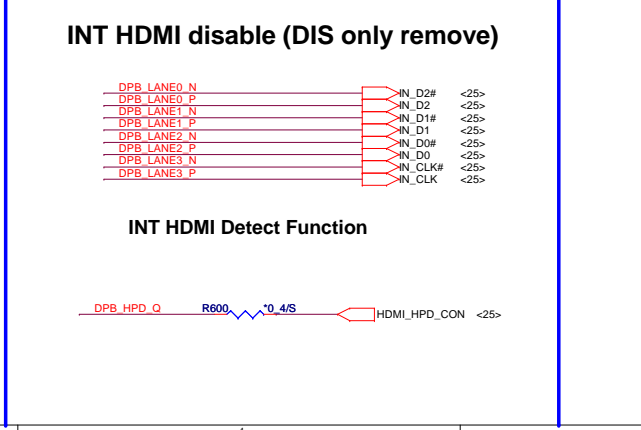
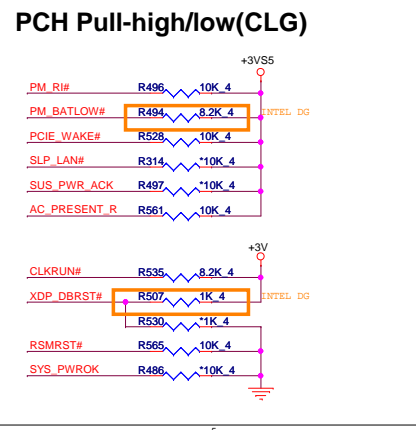
Size Custom	Document Number SNB 4/4 (GND)	Rev 1A
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U32C

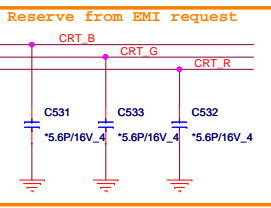
U32D



INT_HDMI



Reserve for power on sequence



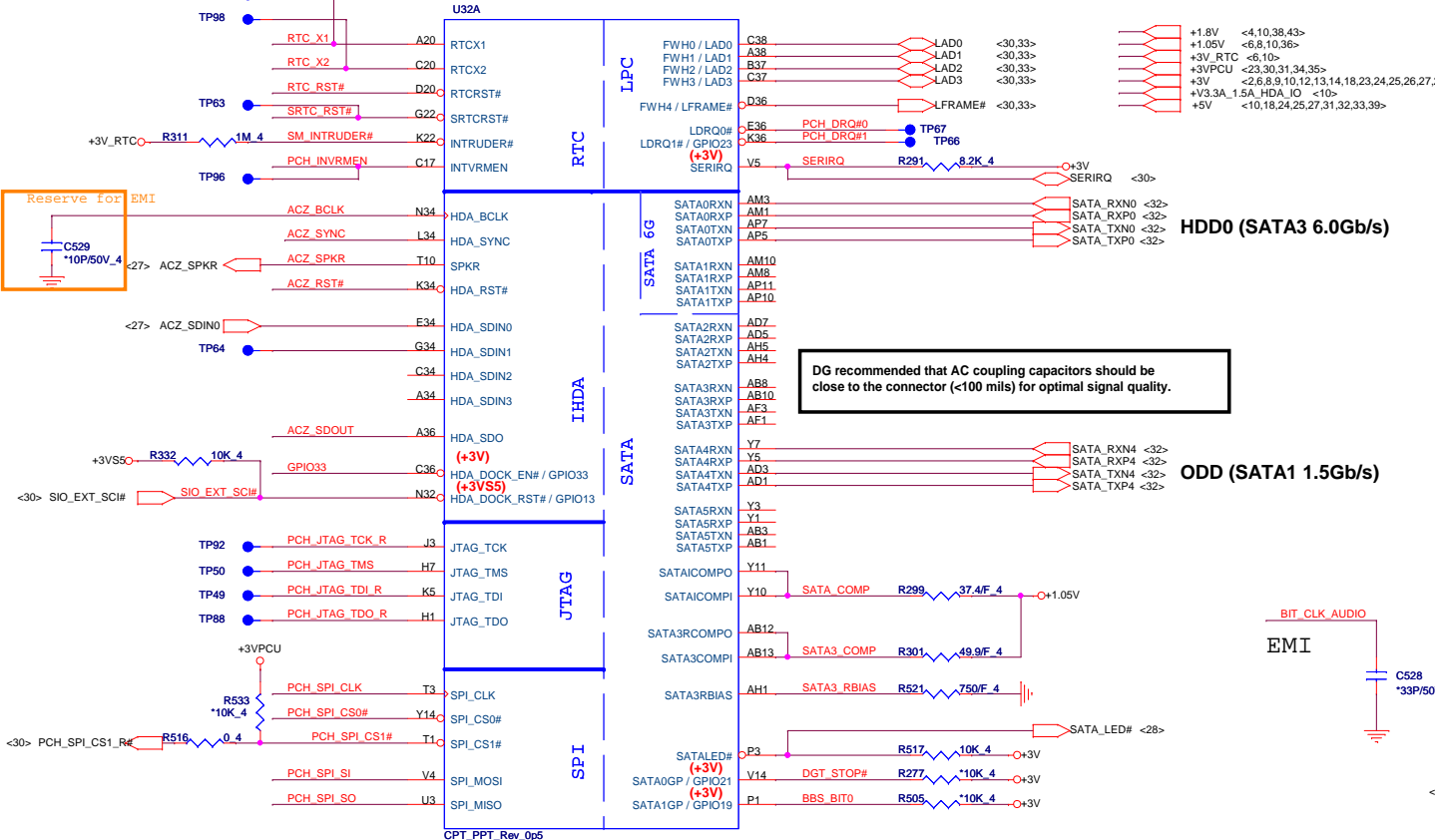
- +3V_RTC <-7,10>
- +1.05V <-7,8,10,36>
- +3VPCU <-7,23,30,31,34,35>
- +3VS5 <-2,7,8,9,10,23,33,35,38,39,42,43>
- +3V <-2,7,8,9,10,12,13,14,18,23,24,25,26,27,28,29,30,31,32,33,39,40,42,43>
- +5V <-7,10,18,24,25,27,31,32,33,39>

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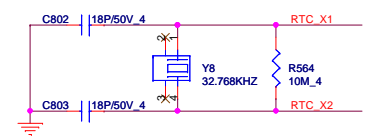
Size Custom Document Number PCH 1/6 (DMI/FDI/VIDEO) Rev 1A

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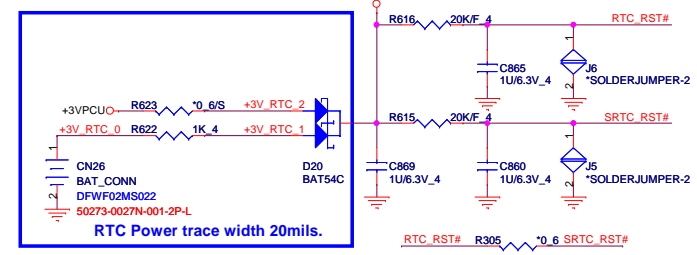
Cougar Point/Panther Point (HDA,JTAG,SATA)



RTC Clock 32.768KHz



RTC Circuitry(RTC)

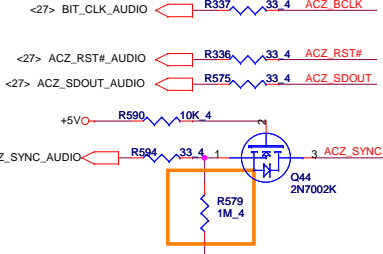


HDD0 (SATA3 6.0Gb/s)

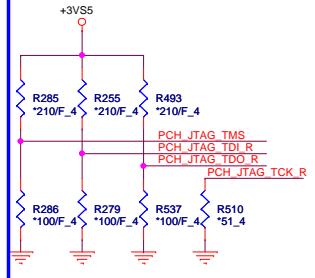
ODD (SATA1 1.5Gb/s)

DG recommended that AC coupling capacitors should be close to the connector (<100 mils) for optimal signal quality.

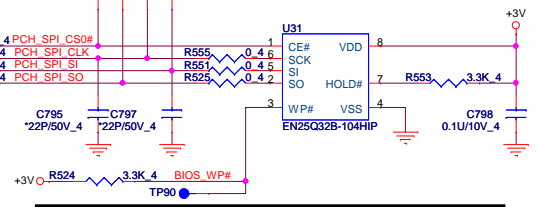
HDA Bus(CLG)



PCH JTAG Debug(CLG)



PCH SPI ROM(CLG)



PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	Circuit
SPKR	Different from Calpella No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	ACZ_SPKR R500 *1K 4 +3V
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R584 *1K 4 R595 *10K 4 +3V
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	PCH_INVRMEN R563 330K 4 +3V_RTC
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security Only for Interposer	PWROK	0 = Override 1 = Default (weak pull-up 20K)	R572 0 4 GPIO33 1 2 BIOS_WP#
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	[Need external pull-down for LPC BIOS] Default weak pull-up on GNT0/1#	R534 *1K 4 R595 *1K 4 BBS_BIT0
GPIO19	Different from Calpella Boot BIOS Selection 0 [bit-0]	PWROK		R534 *1K 4 R595 *1K 4 BBS_BIT1 <8>
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN
NV_ALE	Intel Anti-Theft HDD protection Only for Interposer	PWROK	0 = Disable (Internal pull-down 20kohm)	+1.8V R547 *1K 4 NV_ALE <8>
NV_CLE	DMI Termination voltage	PWROK	weak pull-down 20kohm	+1.8V R528 *2.2K 4 R546 *1K 4 NV_CLE <9> H_SNB_IVB# <2> gandy/ivy bridge
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+3VSS0 R334 *1K 4 ACZ_SYNC
HDA_SDO	Flash Descriptor Security	PWROK	0 = Default (weak pull-down 20K) 1 = Overriden	<30> GPIO33_E ACZ_SDOUT R573 *1K 4 +V3.3A_1.5A_HDA_IO
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)	
GPIO28	Different from Calpella On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	R492 *1K 4 PLL_ODVR_EN <9>
SPI_MOSI	ITPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable	PCH_SPL_SI R292 *1K 4 +3V

Vender	Size	P/N
EON	4MB	AKE39ZNOQ02 (EN25Q32B-104HIP)
Max	4MB	AKE39FP0Z02 (MX25L3206EM2I-12G)
Socket		DFHS08FS023

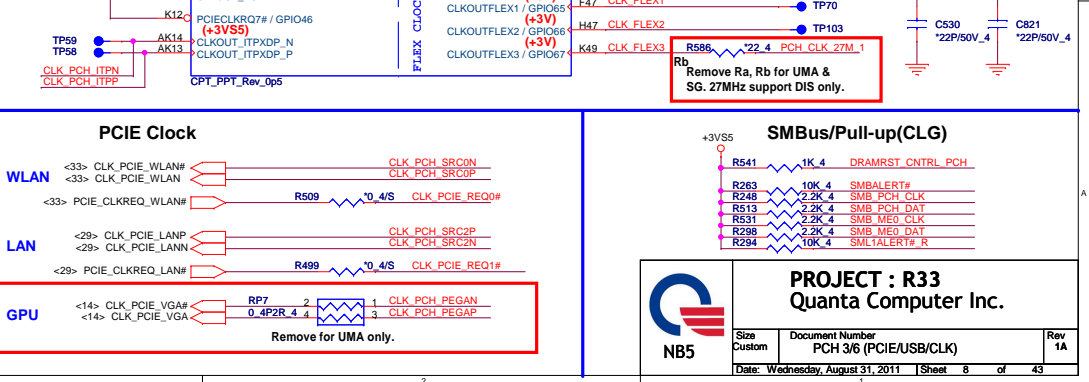
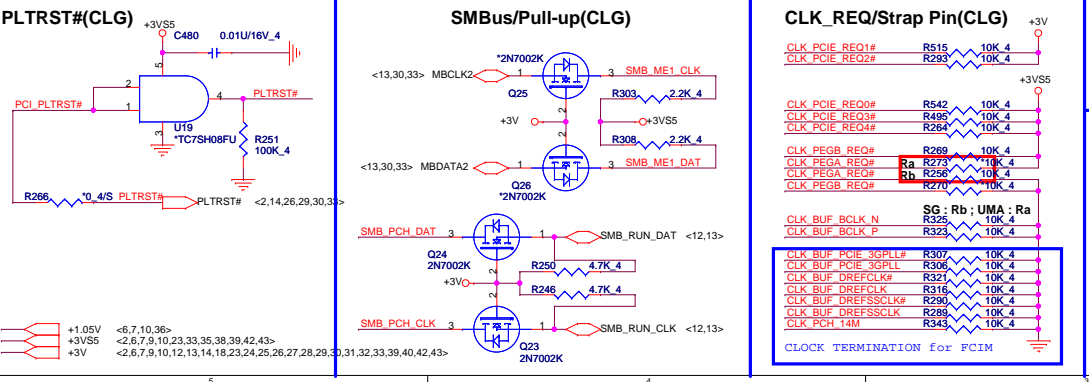
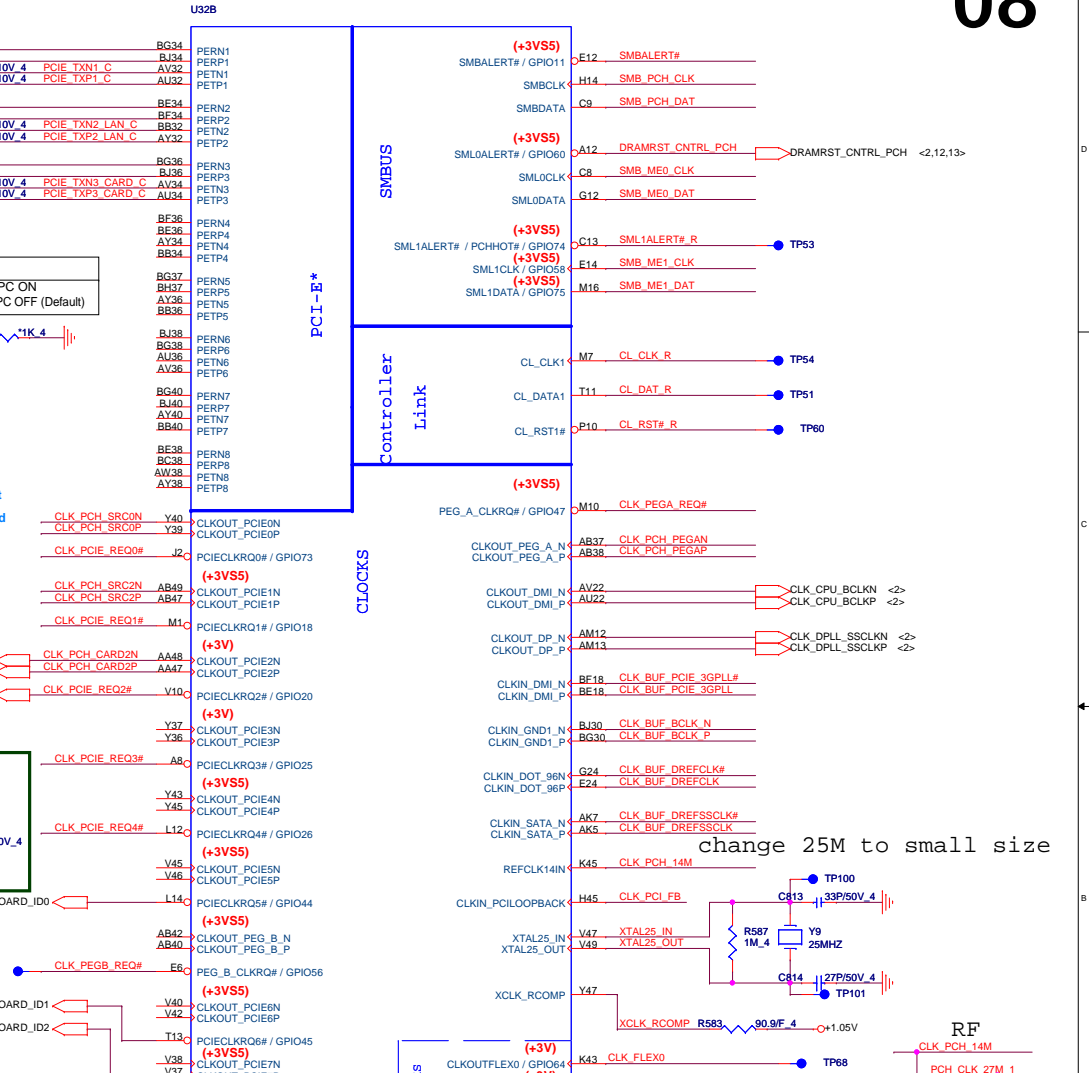
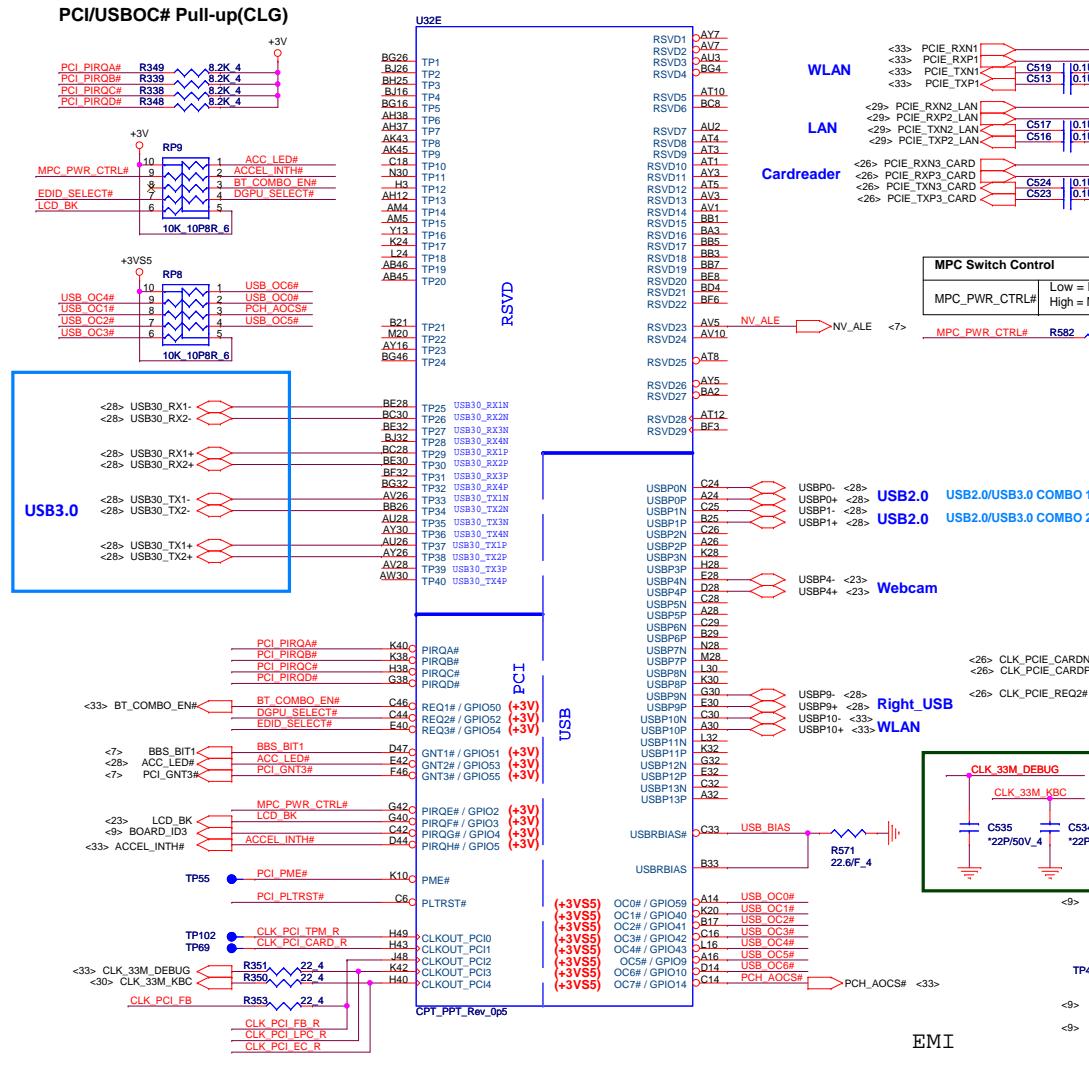


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Size Custom	Document Number PCH 2/6 (SATA/HDA/SPI)	Rev 1A
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Cougar Point/Panther Point (PCI,USB,NVRAM)

Cougar Point/Panther Point (PCI-E,SMBUS,CLK)



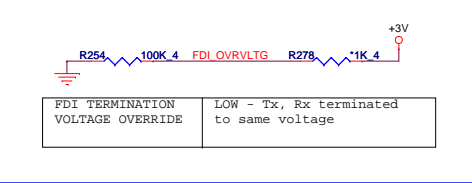
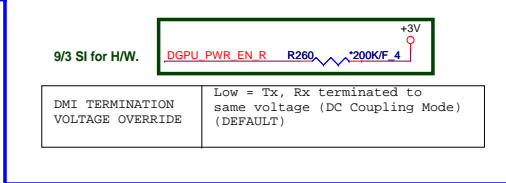
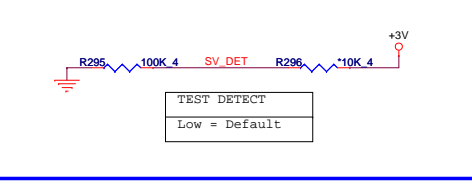
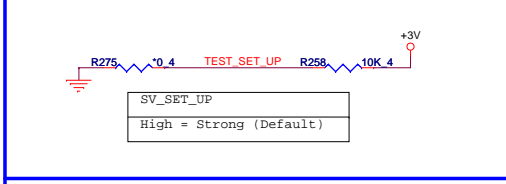
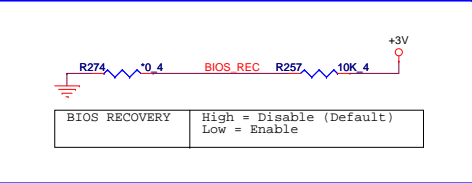
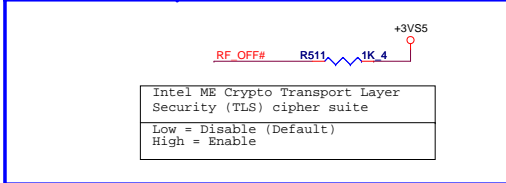
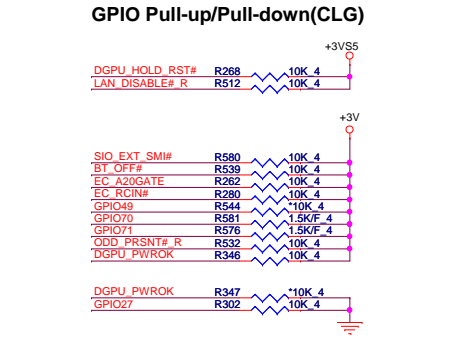
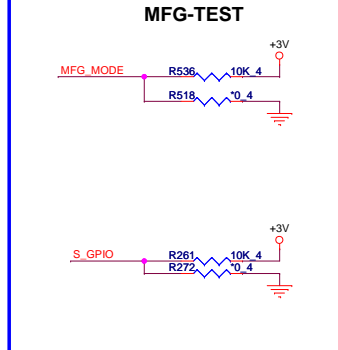
PROJECT : R33
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NB5

Size Custom	Document Number PCH 3/6 (PCIe/USB/CLK)	Rev 1A
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Cougar Point/Panther Point (GPIO,VSS_NCTF,RSVD)

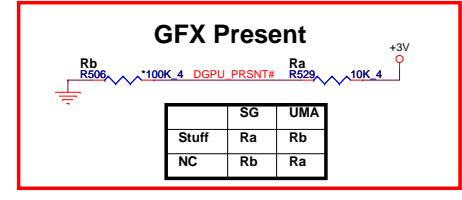
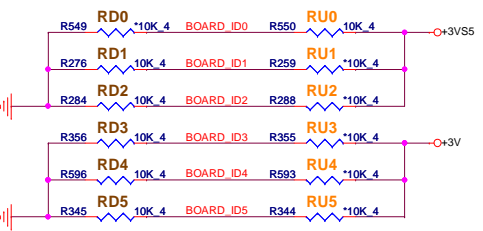
Clock Gen Power OK (CLG)



BOARD ID SETTING

- <8> BOARD_ID0 BOARD_ID0
- <8> BOARD_ID1 BOARD_ID1
- <8> BOARD_ID2 BOARD_ID2
- <8> BOARD_ID3 BOARD_ID3

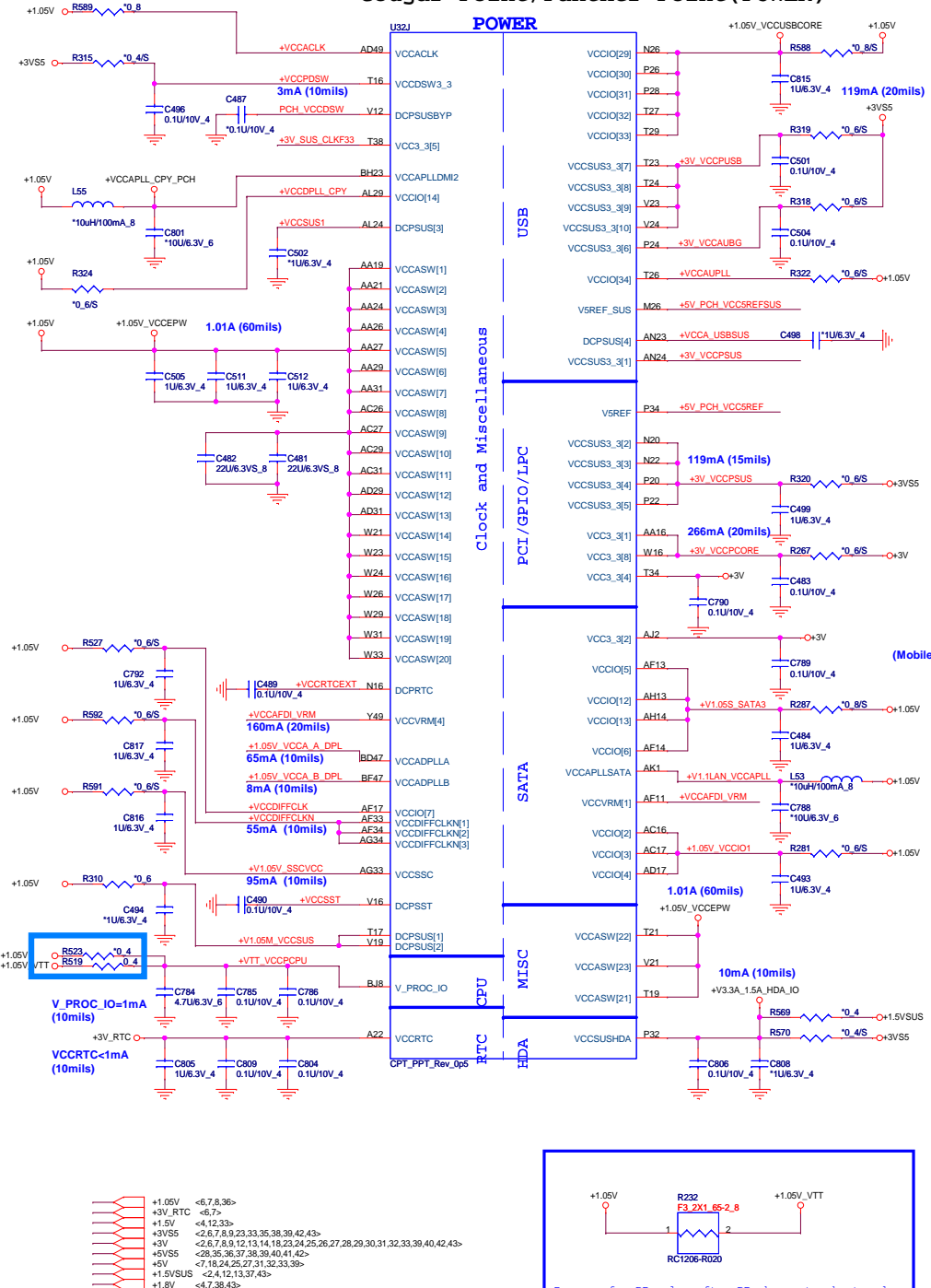
Model	BOARD_ID5	BOARD_ID4	BOARD_ID3	BOARD_ID2	BOARD_ID1	BOARD_ID0
R33 UMA	0	0	0	0	0	0
R33 DIS	0	0	0	0	0	1
	0	0	0	0	1	1
	0	0	0	1	1	1
	0	0	0	0	0	0



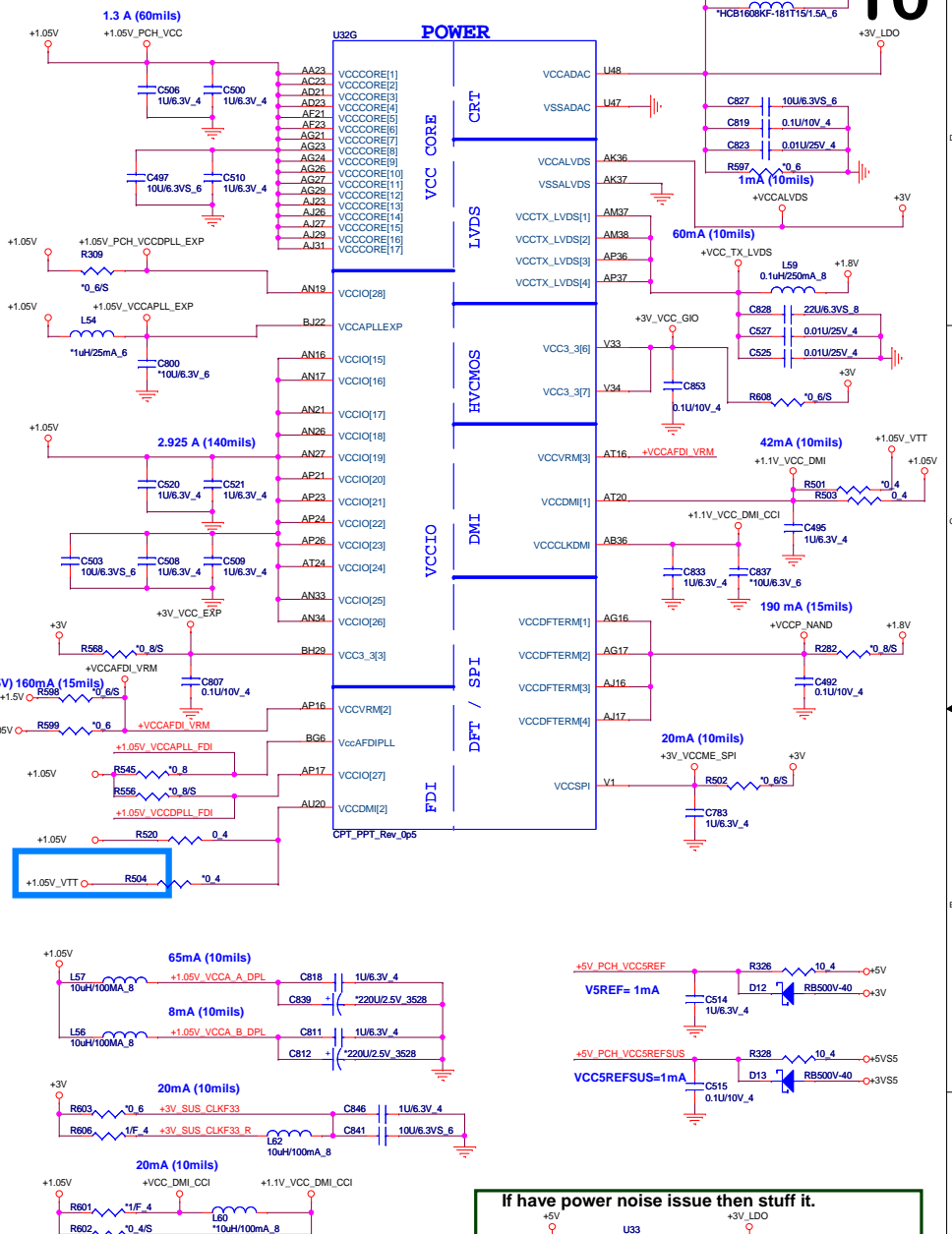
PROJECT : R33
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Size	Document Number	Rev
Custom	PCH 4/6 (GPIO/MISC)	1A
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Cougar Point/Panther Point (POWER)

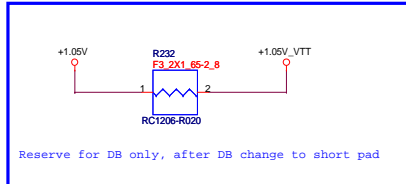


COUGAR POINT/Panther Point (POWER)



If have power noise issue then stuff it.

U33 6810T21U
Vin, GND, Vout

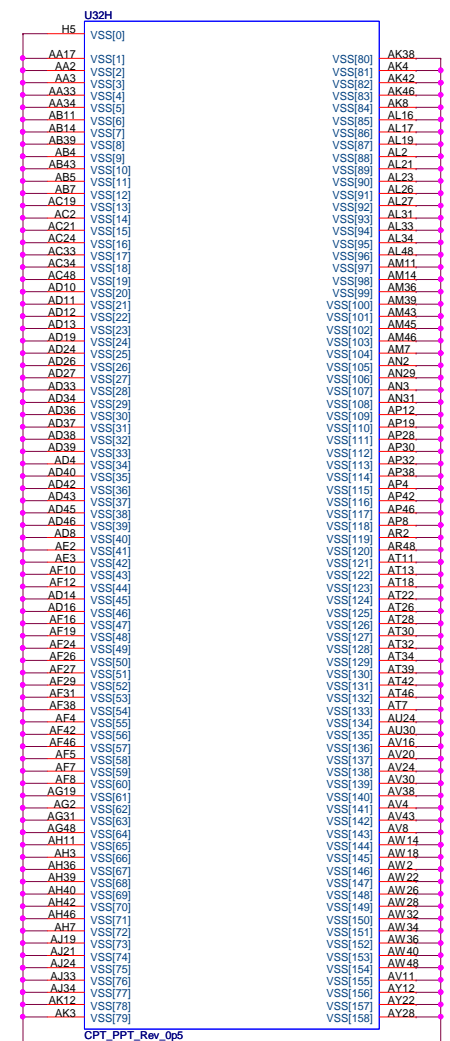
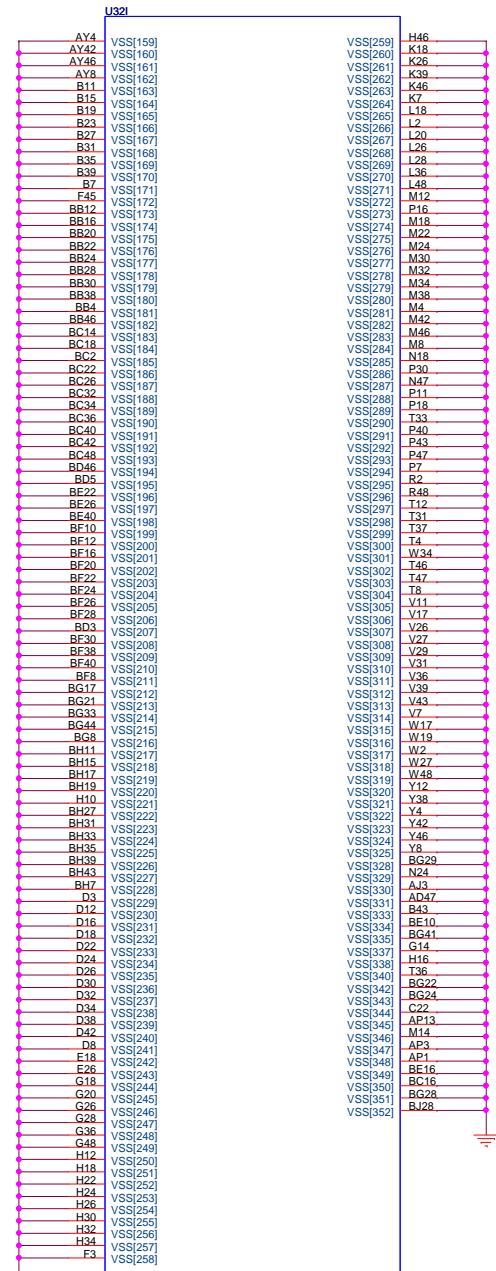


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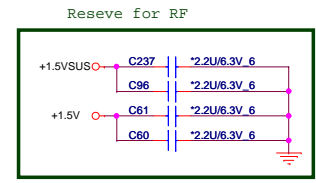
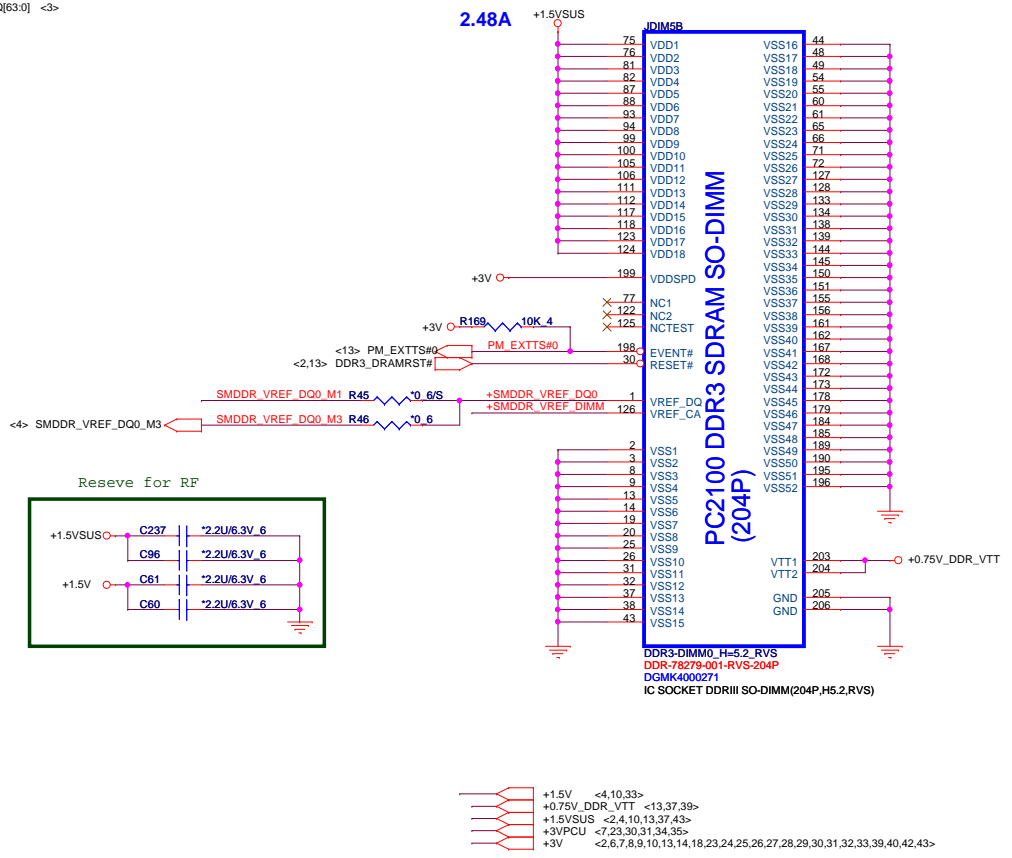
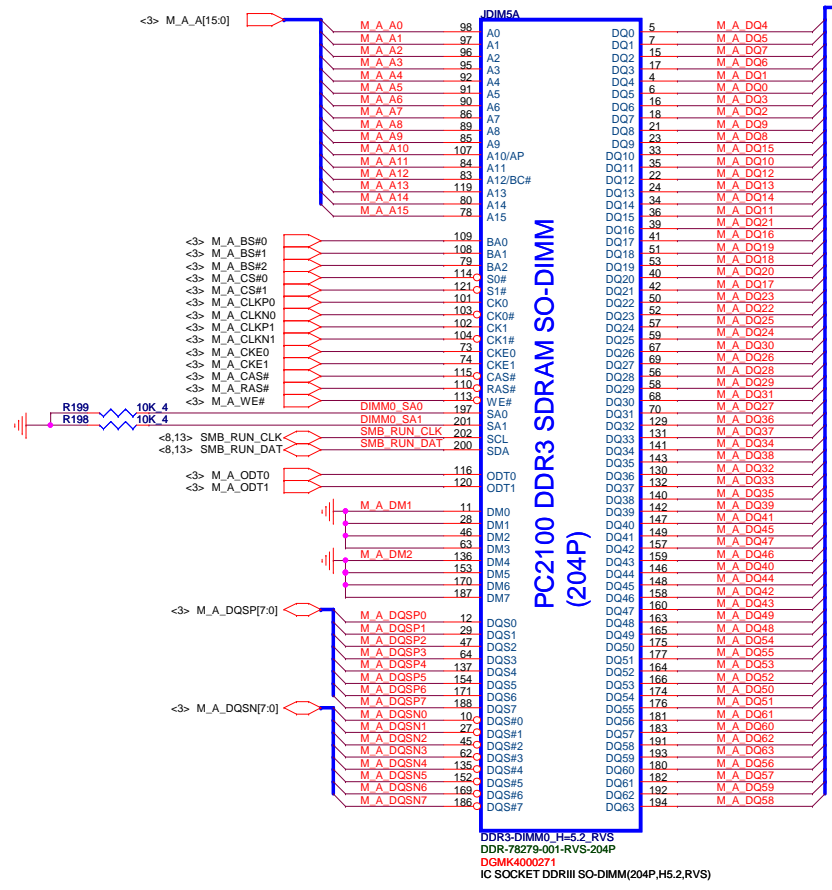
Date	Document Number	Rev
Wednesday, August 31, 2011 <td>PCH 5/6 (POWER) <td>1A</td> </td>	PCH 5/6 (POWER) <td>1A</td>	1A

Cougar Point/Panther Point (GND)

Cougar Point/Panther Point (GND)



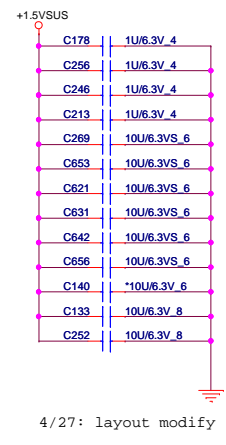
	PROJECT : R33	
	Quanta Computer Inc.	
	Size Custom	Document Number PCH 6/6 (GND)
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- +1.5V <4,10,33>
- +0.75V_DDR_VTT <13,37,39>
- +1.5VSUS <2,4,10,13,37,43>
- +3VPCU <7,23,30,31,34,35>
- +3V <2,6,7,8,9,10,13,14,18,23,24,25,26,27,28,29,30,31,32,33,39,40,42,43>

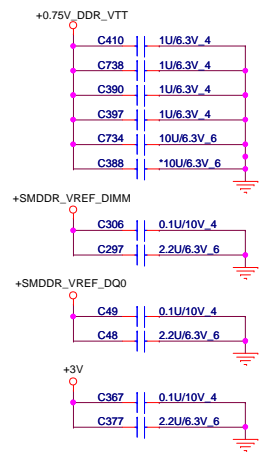
del M2 solution

VREF DQ0 M2 Solution

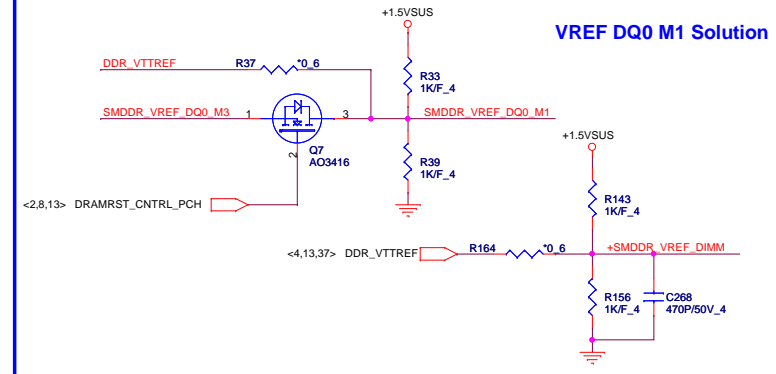


4/27: layout modify

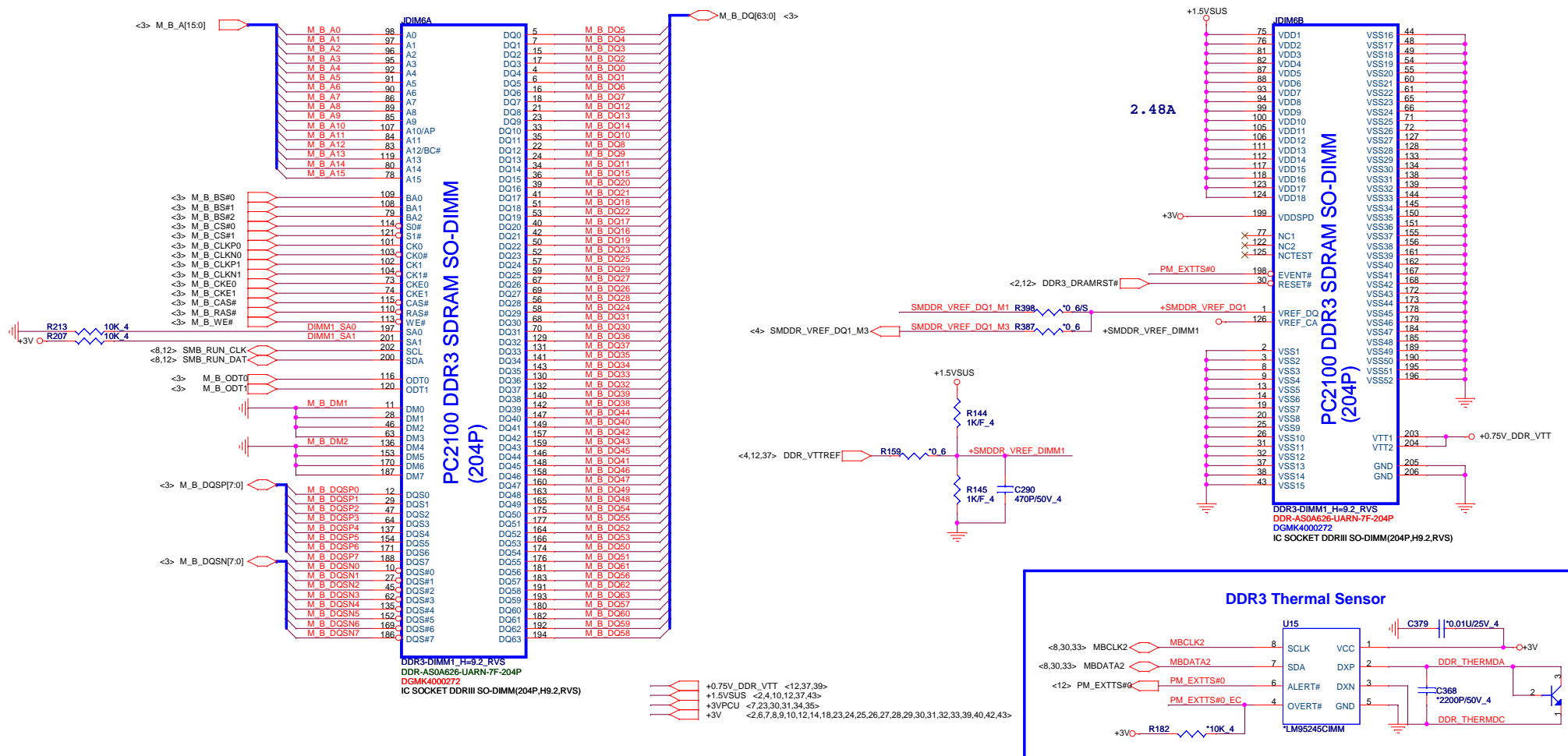
Place these Caps near So-Dimm0.



VREF DQ0 M1 Solution



	PROJECT : R33		Rev 1A
	Quanta Computer Inc.		
	Size Custom	Document Number DDR3 DIMM0-RVS (5.2H)	
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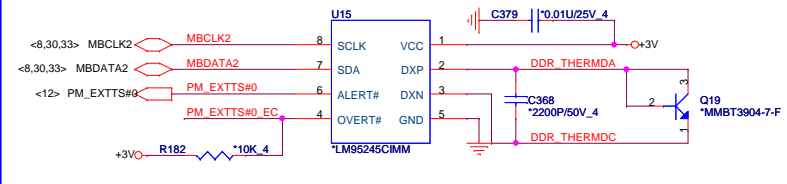


2.48A

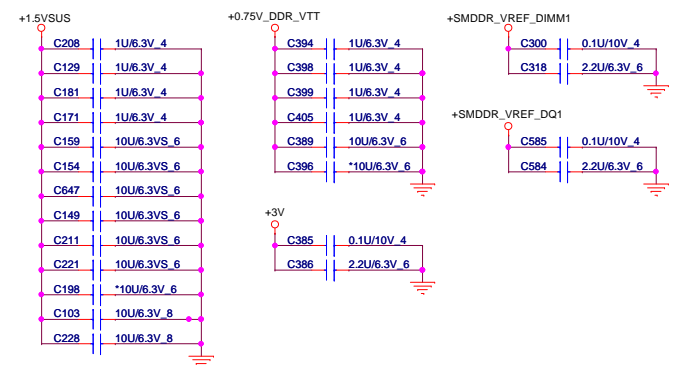
PC2100 DDR3 SDRAM SO-DIMM (204P)

DDR3-DIMM1_H=9.2_RVS
 DDR-A50A626-UARN-7F-204P
 DGMK400272
 IC SOCKET DDRIII SO-DIMM(204P,H9.2,RVS)

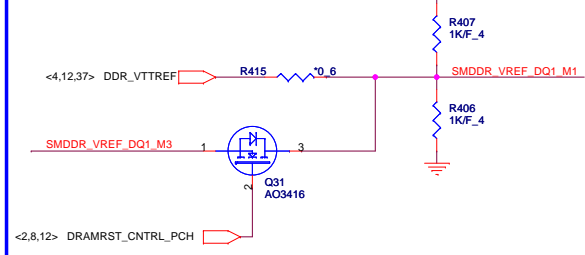
DDR3 Thermal Sensor



Place these Caps near So-Dimm1.



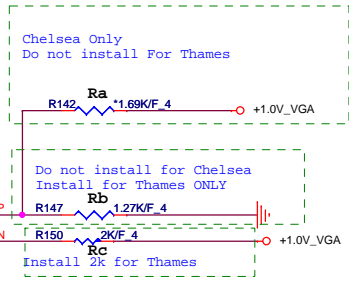
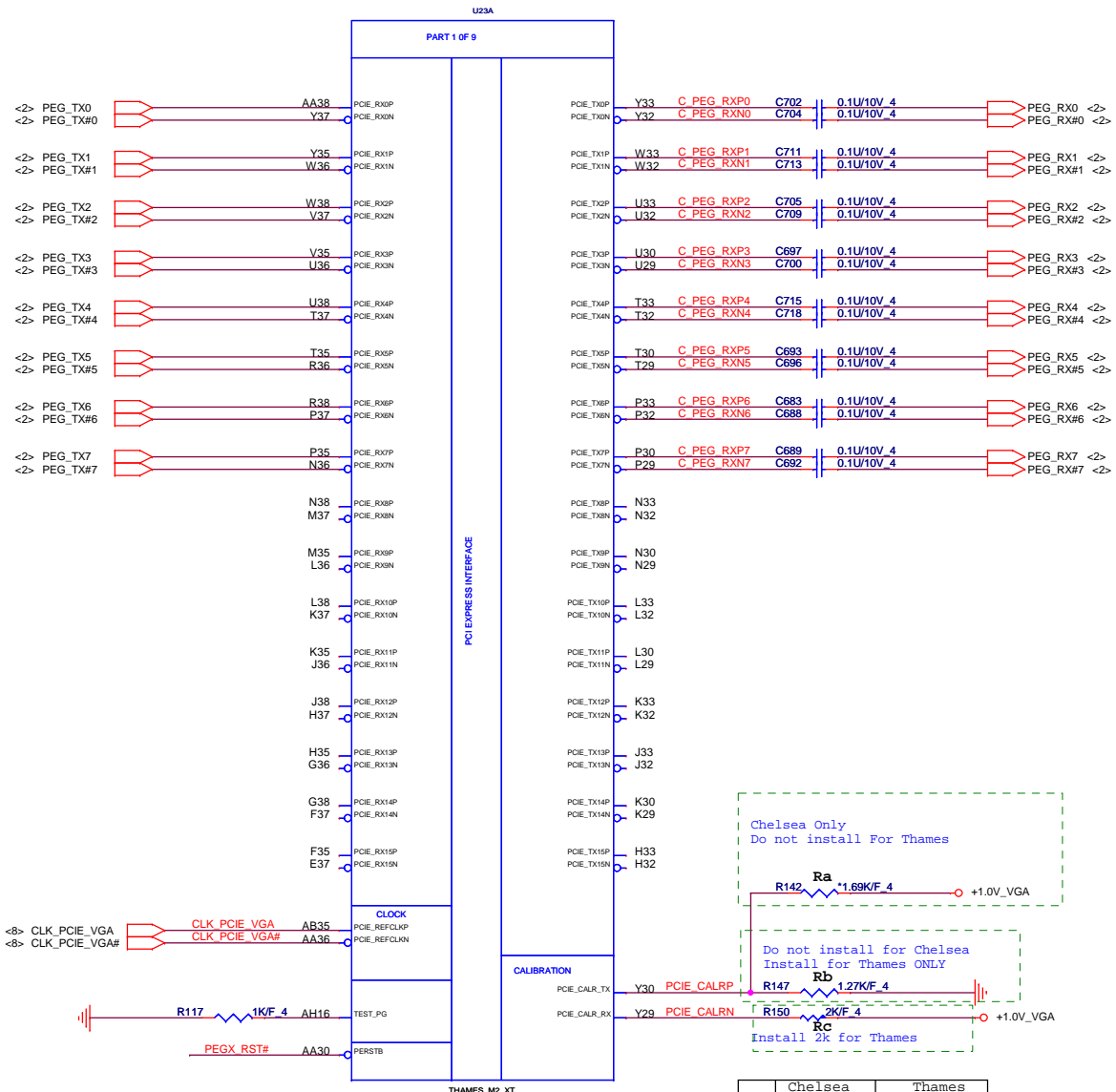
VREF DQ1 M1 Solution



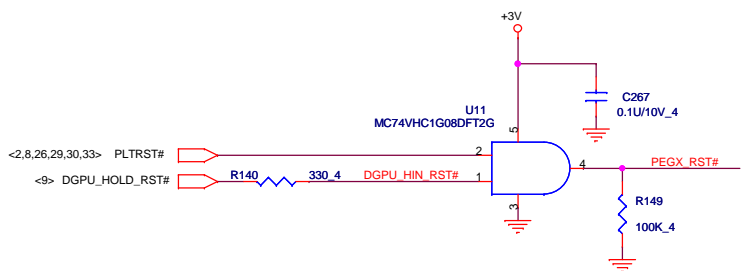
del M2 solution

PROJECT : R33
Quanta Computer Inc.

Size Custom	Document Number DDR3 DIMM1-RVS (9.2H)	Rev 1A
Date: Wednesday, August 31, 2011 Sheet 13 of 43		



	Chelsea	Thames
Ra	1.69K	n/a
Rb	n/a	1.27K
Rc	1K	2K



<16,18,19,43> +1.0V_VGA



PROJECT : R33
Quanta Computer Inc.

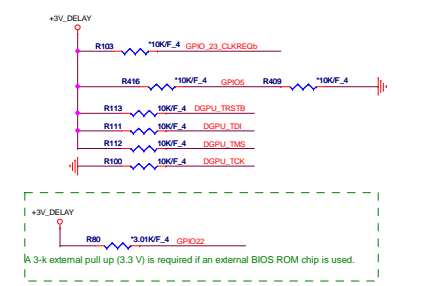
Size Custom	Document Number THAMES_PCIE_Interface	Rev 1A
Date: Wednesday, August 31, 2011		Sheet 14 of 43

MEM_ID[3:0]	Vendor	Type	Vendor P/N
0000	Hynix- D (VEGA)	64Mx16 *8, 900Mhz	H5TQ1G63DFR-11C
0001	Micron- G die	64Mx16 *8, 900Mhz	MT41J64M16JT-107G:G
0010	Samsung- G die	64Mx16 *8, 900Mhz	K4W1G1646G-BC11
0011	Hynix- B (VEGA)	128Mx16 *8, 900Mhz	H5TQ2G63BFR-11C
0100	Micron- D die	128Mx16 *8, 900Mhz	MT41J128M16HA-107G:D
0101	Samsung- C die	128Mx16 *8, 900Mhz	K4W2G1646C-HC11
0110	Hynix- B (VEGA)	128Mx16 *4, 900Mhz	H5TQ2G63BFR-11C
0111	Micron- D die	128Mx16 *4, 900Mhz	MT41J128M16HA-107G:D
1000	Samsung- C die	128Mx16 *4, 900Mhz	K4W2G1646C-HC11
1010			
1011			
1100			
1101			
1110			
1111			

GPIO16 GPIO20 GPIO15

Thames XT	PWRCNTL2	PWRCNTL1	PWRCNTL0	V-CORE
L	0	0	0	1.0V
M	0	0	1	0.9V
H	0	1	0	0.875V
	0	1	1	0.85V
	1	0	0	0.8V
	1	0	1	0.75V

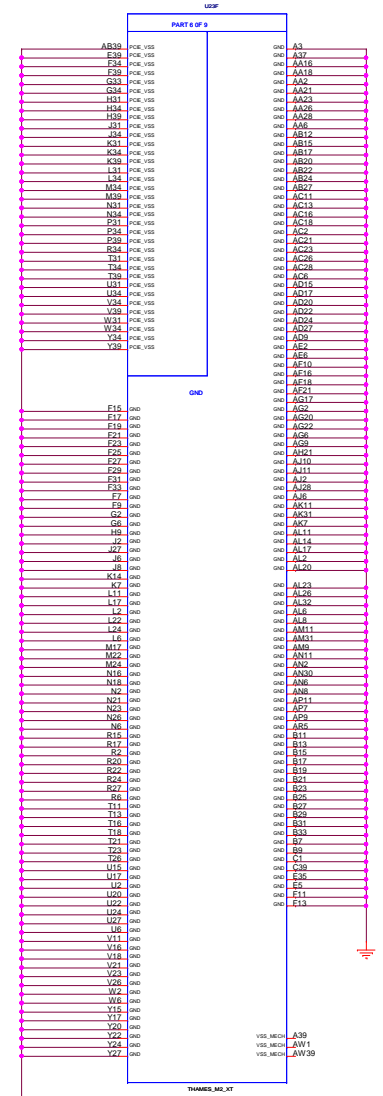
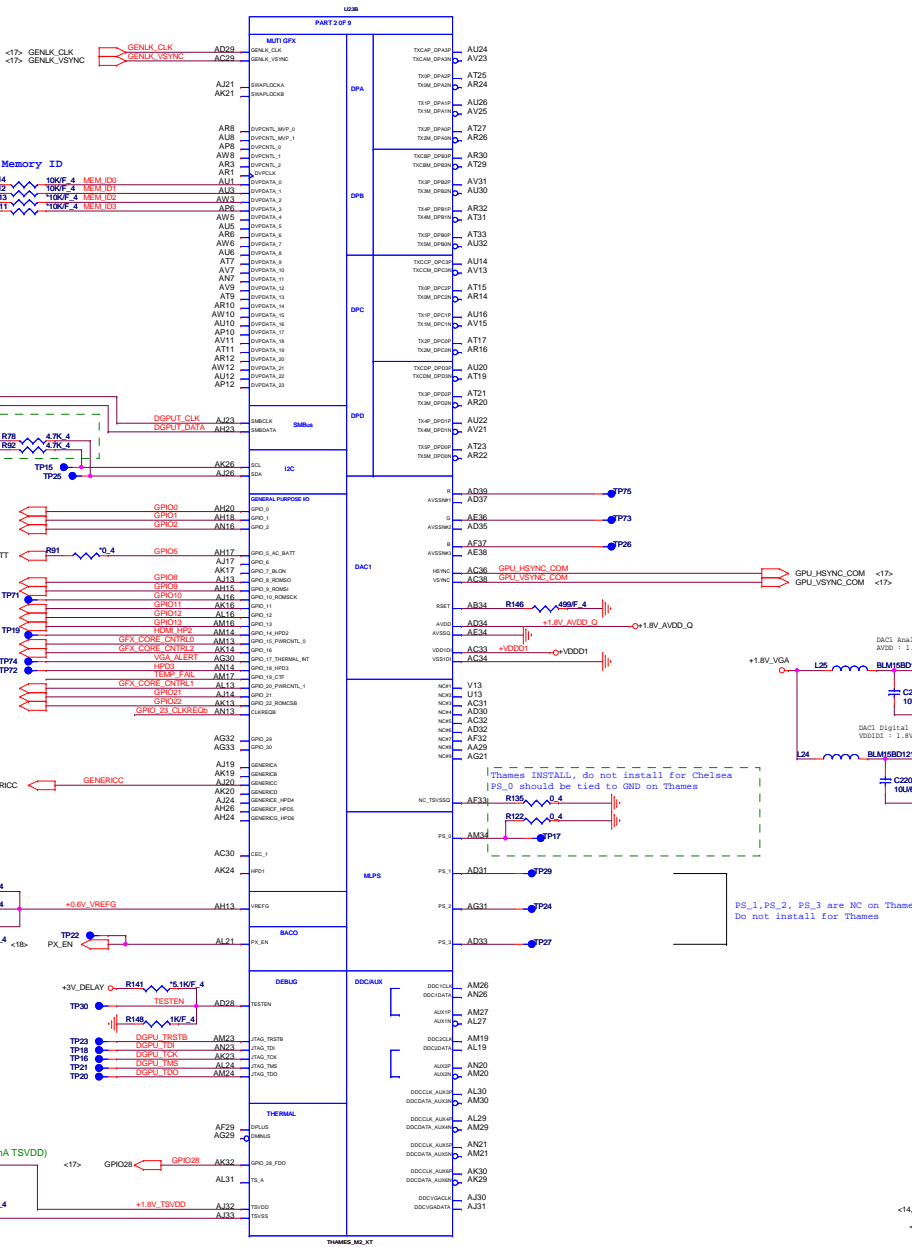
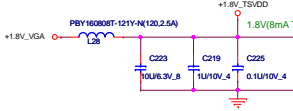
Access to SMBus and SDA/SCL is mandatory on all designs
Add test points on SMBus and SDA/SCL for debug



A 3-k external pull up (3.3 V) is required if an external BIOS ROM chip is used.



Reserve for Power Play



Thames INSTALL, do not install for Chelsea
PS_0 should be tied to GND on Thames

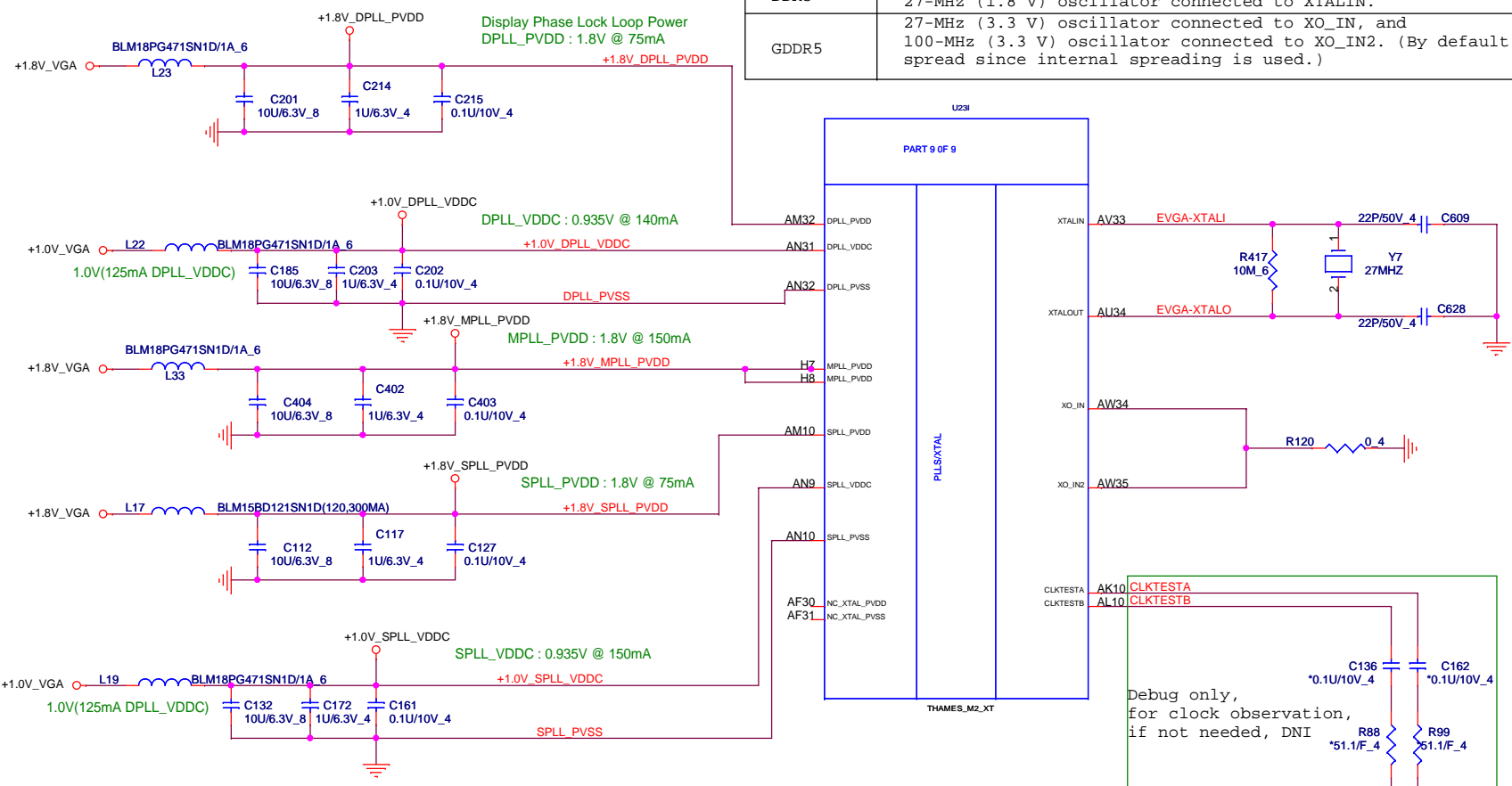
PS_1, PS_2, PS_3 are NC on Thames
Do not install for Thames



PROJECT : R33
Quanta Computer Inc.

Docu: **THAMES_Main & GND**

Date: Wednesday, August 31, 2011 | Sheet 15 of 20

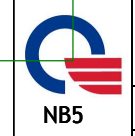
Memory Type	
DDR3	27-MHz (± 30 ppm) crystal connected to XTALIN/XTALOUT, or 27-MHz (1.8 V) oscillator connected to XTALIN.
GDDR5	27-MHz (3.3 V) oscillator connected to XO_IN, and 100-MHz (3.3 V) oscillator connected to XO_IN2. (By default, this clock should not be spread since internal spreading is used.)



<14,18,19,43> +1.0V_VGA  +1.0V_VGA
 <15,18,19,43> +1.8V_VGA  +1.8V_VGA

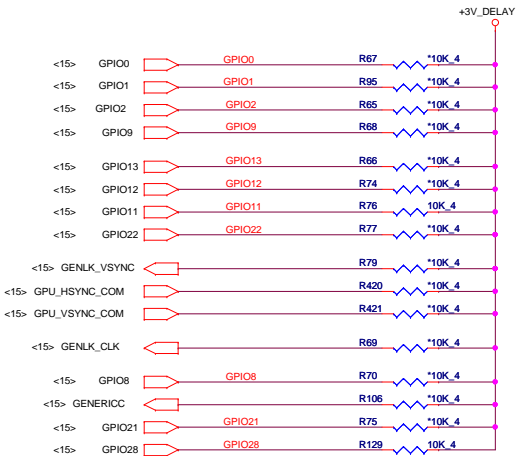
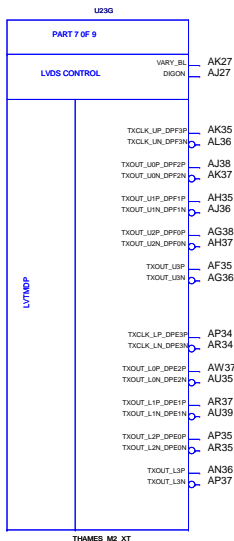
Debug only,
 for clock observation,
 if not needed, DNI

route 50ohms
 single-ended/
 100ohms diff and keep short



PROJECT : R33
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Date: Wednesday, August 31, 2011 Sheet 16 of 43		



CONFIGURATION STRAPS -- SEE EACH DATABOOK FOR STRAP DETAILS
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

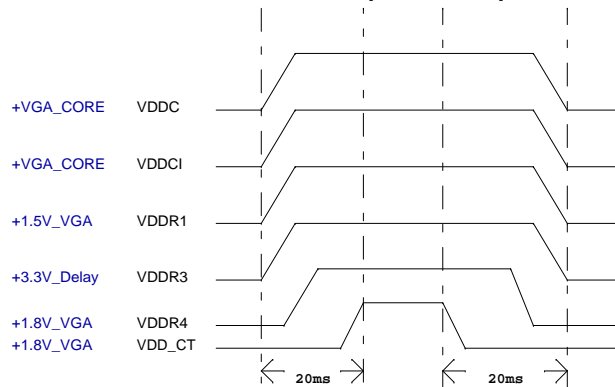
STRAPS	MLPS	GPIO PIN	DESCRIPTION OF DEFAULT SETTINGS	Default Setting
MLPS_DISABLE	NA	GPIO_28_FDO	Enable MLPS, NA for Thames/Whistler/Seymour 0: Enable MLPS, disable GPIO PINSTRAP 1: Disable MLPS, enable GPIO PINSTRAP	X
TX_PWRS_ENB	PS_1[4]	GPIO0	Transmitter Power Savings Enable 0: 50% TX output swing 1: Full TX output swing	X
TX_DEEMPH_EN	PS_1[5]	GPIO1	PCIe Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled	X
BIF_GEN3_EN_A	PS_1[1]	GPIO2	PCIe Gen3 Enable (NOTE: RESERVED for Thames/Whistler/Seymour) 0: GEN3 not supported at power-on 1: GEN3 supported at power-on	1
BIF_VGA_DIS	PS_2[4]	GPIO9	VGA Control 0: VGA controller capacity enabled 1: VGA controller capacity disabled (for multi-GPU)	0
ROMIDCFG[2:0]	PS_0[3..1]	GPIO[13:11]	Serial ROM type or Memory Aperture Size Select If GPIO22 = 0, defines memory aperture size If GPIO22 = 1, defines ROM type 100 - 512kbit M25P05A (ST) 101 - 1Mbit M25P05A (ST) 101 - 4Mbit V25P30 (ST) 101 - 4Mbit V25P40 (ST) 101 - 8Mbit V25P80 (ST) 101 - 512kbit Pm25LV612 (Chingis) 101 - 1Mbit Pm25LV010 (Chingis)	XXX
BIOS_ROM_EN	PS_2[3]	GPIO22	Enable external BIOS ROM device 0: Disabled 1: Enabled	X
AUD[1] AUD[0]	NA NA	HSYNC VSYNC	00 - No audio function 01 - Audio for DP only 10 - Audio for DP and HDMI if dongle is detected 11 - Audio for both DP and HDMI HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.	XX
CEC_DIS	PS_0[4]	GENLK_VSYNC	Enable CEC function. Reserved for Thames/Whistler/Seymour 0: Disabled 1: Enabled	X
RESERVED RESERVED RESERVED RESERVED	PS_1[3] PS_1[2] NA NA	GENLK_CLK GPIO8 GPIO21 GENERICC	Reserved Reserved Reserved Reserved (for Thames/Whistler/Seymour only)	0 0 0 0
AUD_PORT_CONN_PINSTRAP[2] AUD_PORT_CONN_PINSTRAP[1] AUD_PORT_CONN_PINSTRAP[0]	PS_3[5] PS_3[4] PS_0[5]	NA NA NA	STRAPS TO INDICATE THE NUMBER OF AUDIO CAPABLE DISPLAY OUTPUTS 111 = 0 usable endpoints 110 = 1 usable endpoints 101 = 2 usable endpoints 100 = 3 usable endpoints 011 = 4 usable endpoints 010 = 5 usable endpoints 001 = 6 usable endpoints 000 = all endpoints are usable	XXX

Memory Aperture size

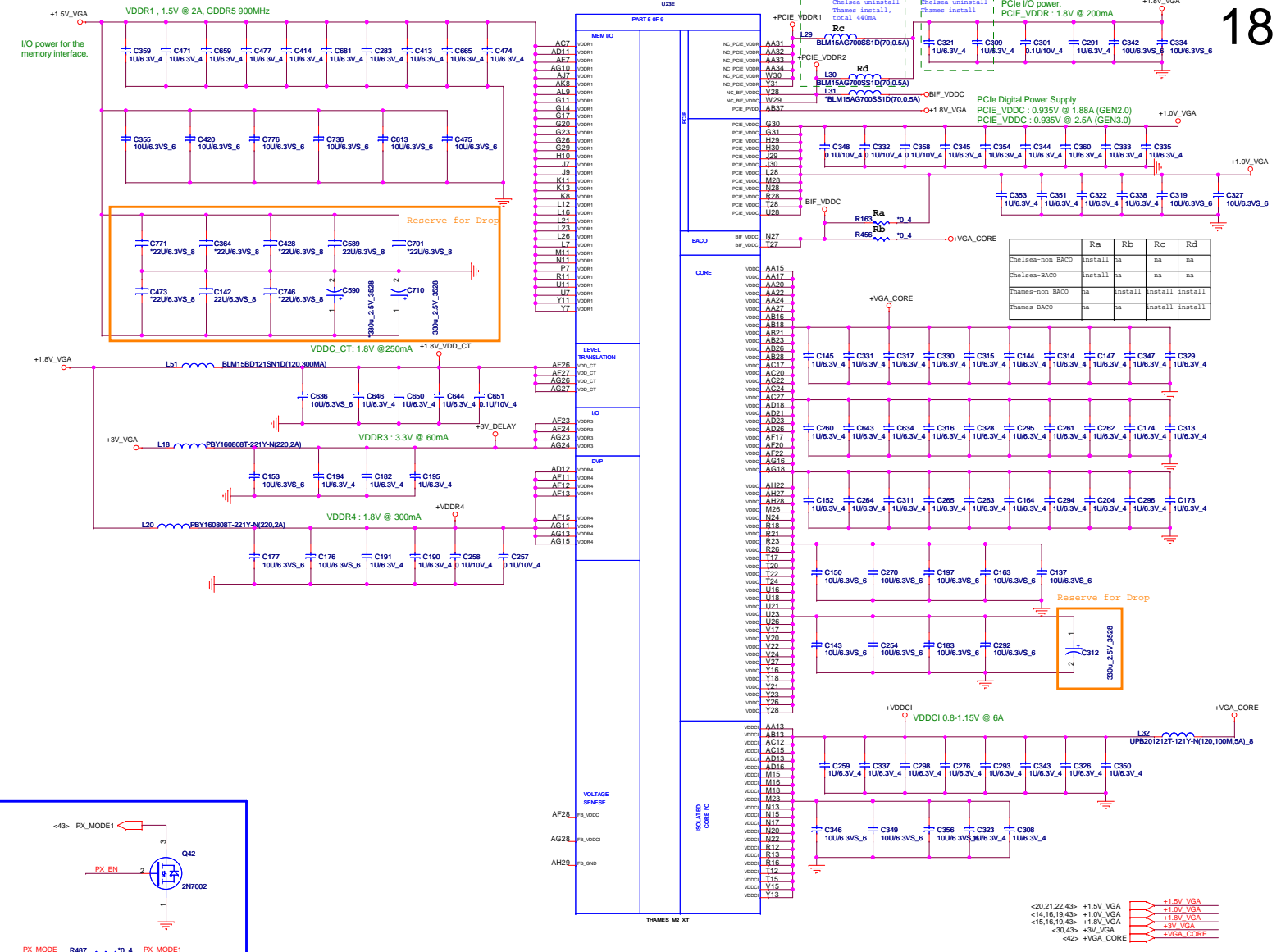
GPIO9 BIOSROM	GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0
0	256M	0	1
0	64M	0	1
0	32M	0	1
0	512M	1	0
0	1G	1	0
0	2G	1	1
0	4G	1	1

It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.

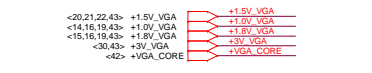
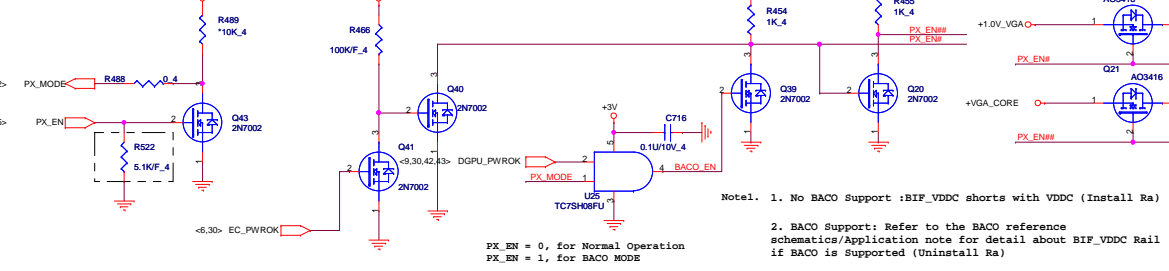
Power Up/Down Sequence



PROJECT : R33
Quanta Computer Inc.



Support BACO Mode



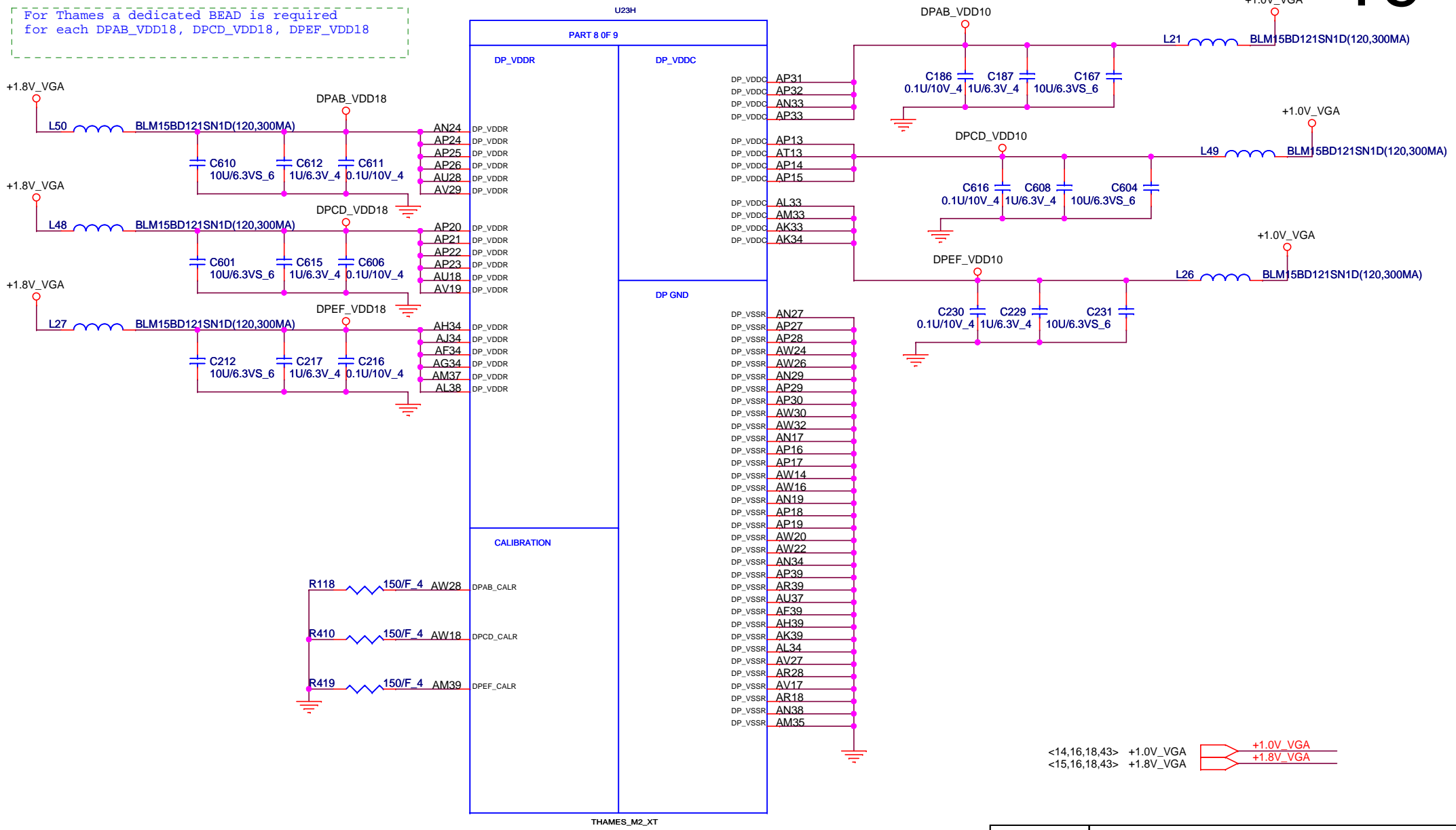
PROJECT : R33
Quanta Computer Inc.

Size Custom Document Number **THAMES_Power & BACO** Rev TA

Date: Wednesday, August 31, 2011 Sheet 18 of 43

For Thames a dedicated BEAD is required for each DPAB_VDD18, DPCD_VDD18, DPEF_VDD18

For Thames a dedicated BEAD is required for each DPAB_VDD10, DPCD_VDD10, DPEF_VDD10



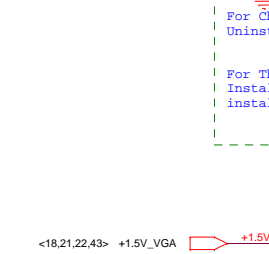
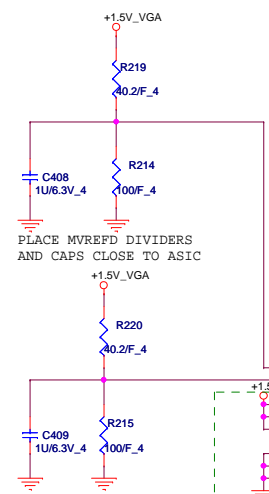
<14,16,18,43> +1.0V_VGA
 <15,16,18,43> +1.8V_VGA



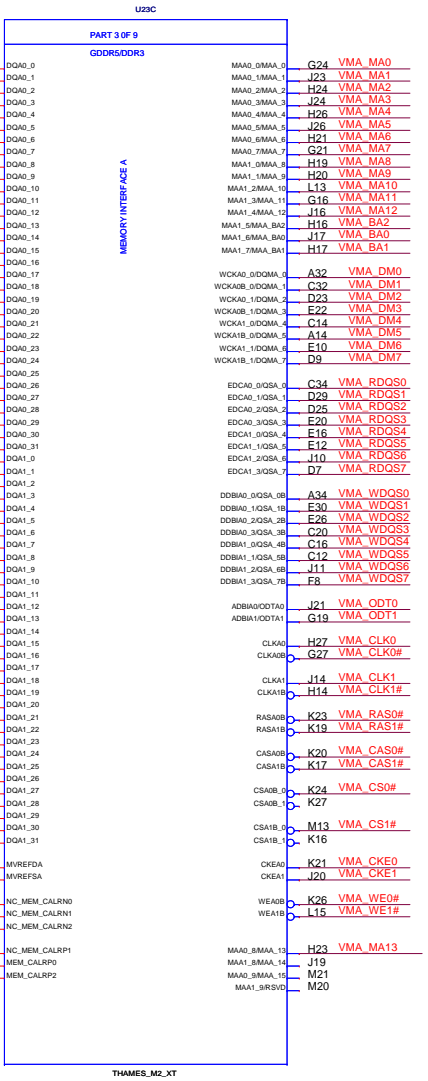
PROJECT : R33
Quanta Computer Inc.

Size Custom	Document Number THAMES_DP Powers	Rev 1A
Date: Wednesday, August 31, 2011		Sheet 19 of 43

- <21> VMA_ODT0 VMA ODT0
- <21> VMA_ODT1 VMA ODT1
- <21> VMA_RAS0# VMA RAS0#
- <21> VMA_RAS1# VMA RAS1#
- <21> VMA_CAS0# VMA CAS0#
- <21> VMA_CAS1# VMA CAS1#
- <21> VMA_WE0# VMA WE0#
- <21> VMA_WE1# VMA WE1#
- <21> VMA_CS0# VMA CS0#
- <21> VMA_CS1# VMA CS1#
- <21> VMA_CKE0 VMA CKE0
- <21> VMA_CKE1 VMA CKE1
- <21> VMA_CLK0 VMA CLK0
- <21> VMA_CLK0# VMA CLK0#
- <21> VMA_CLK1 VMA CLK1
- <21> VMA_CLK1# VMA CLK1#
- <21> VMA_WDQS[7..0] VMA WDQS[7..0]
- <21> VMA_RDQS[7..0] VMA RDQS[7..0]
- <21> VMA_DM[7..0] VMA DM[7..0]
- <21> VMA_DQ[63..0] VMA DQ[63..0]
- <21> VMA_MA[13..0] VMA MA[13..0]
- <21> VMA_BA0 VMA BA0
- <21> VMA_BA1 VMA BA1
- <21> VMA_BA2 VMA BA2

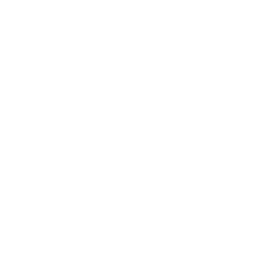
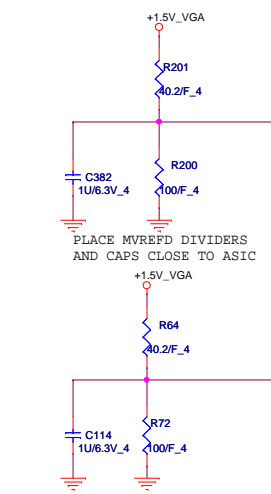


<18,21,22,43> +1.5V_VGA

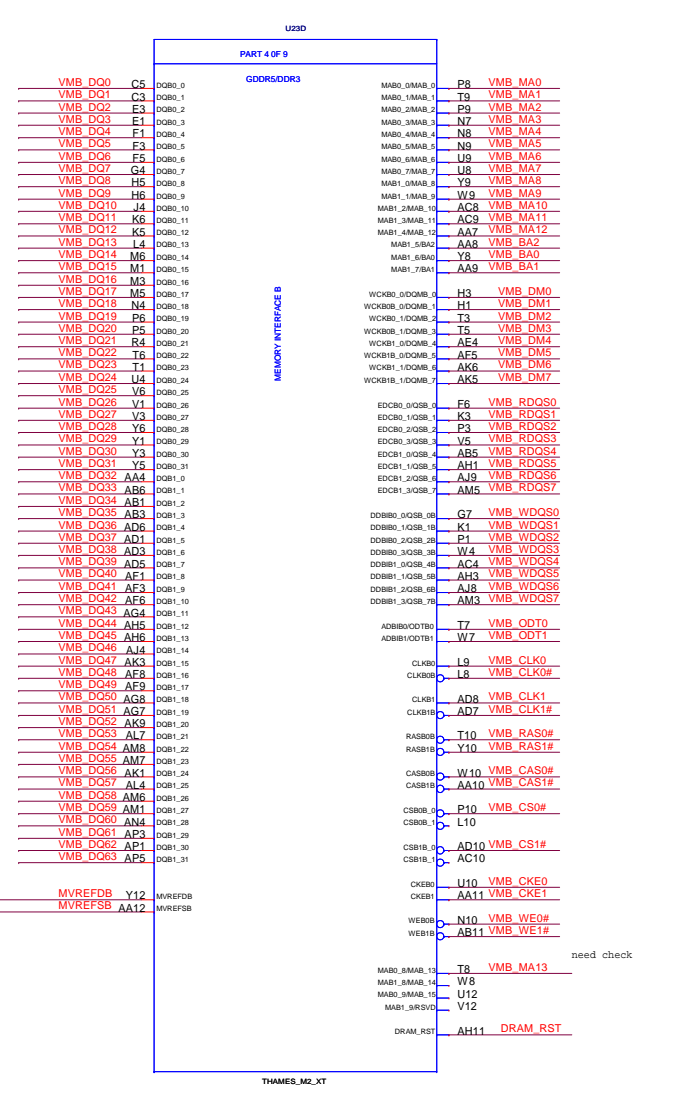


THAMES_M2_XT

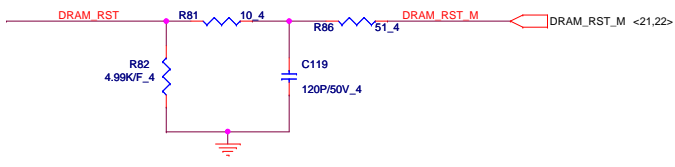
- <22> VMB_ODT0 VMB ODT0
- <22> VMB_ODT1 VMB ODT1
- <22> VMB_RAS0# VMB RAS0#
- <22> VMB_RAS1# VMB RAS1#
- <22> VMB_CAS0# VMB CAS0#
- <22> VMB_CAS1# VMB CAS1#
- <22> VMB_WE0# VMB WE0#
- <22> VMB_WE1# VMB WE1#
- <22> VMB_CS0# VMB CS0#
- <22> VMB_CS1# VMB CS1#
- <22> VMB_CKE0 VMB CKE0
- <22> VMB_CKE1 VMB CKE1
- <22> VMB_CLK0 VMB CLK0
- <22> VMB_CLK0# VMB CLK0#
- <22> VMB_CLK1 VMB CLK1
- <22> VMB_CLK1# VMB CLK1#
- <22> VMB_WDQS[7..0] VMB WDQS[7..0]
- <22> VMB_RDQS[7..0] VMB RDQS[7..0]
- <22> VMB_DM[7..0] VMB DM[7..0]
- <22> VMB_DQ[63..0] VMB DQ[63..0]
- <22> VMB_MA[13..0] VMB MA[13..0]
- <22> VMB_BA0 VMB BA0
- <22> VMB_BA1 VMB BA1
- <22> VMB_BA2 VMB BA2



<18,21,22,43> +1.5V_VGA



THAMES_M2_XT



need check

PROJECT : R33
Quanta Computer Inc.

Size Custom	Document Number THAMES_MEM_Interface	Rev 1A
Date: Wednesday, August 31, 2011	Sheet 20	of 43

CHANNEL A: 256MB/512MB DDR3

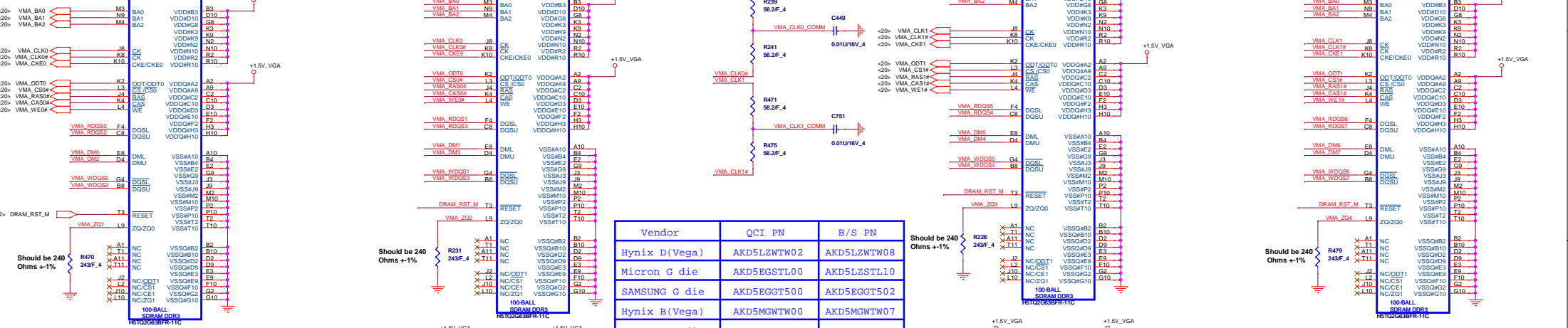
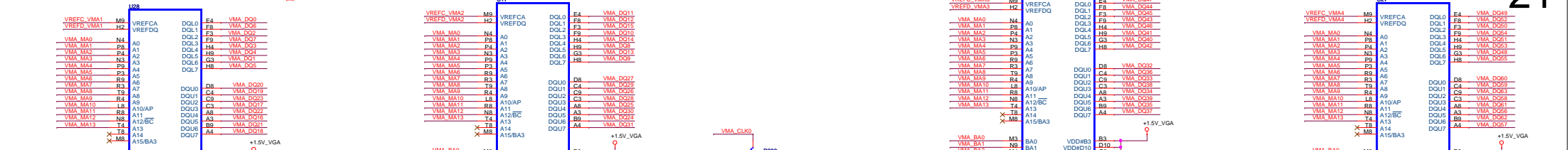
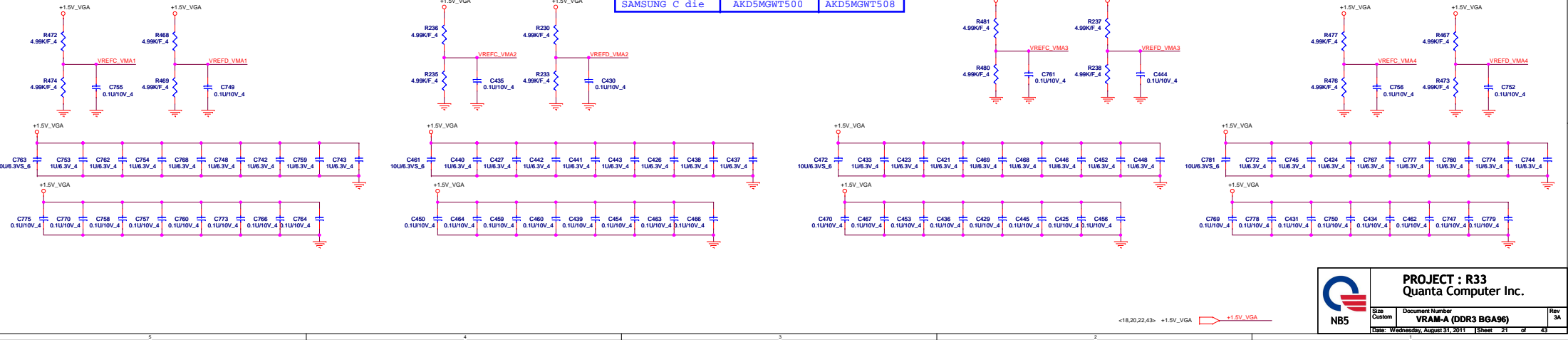
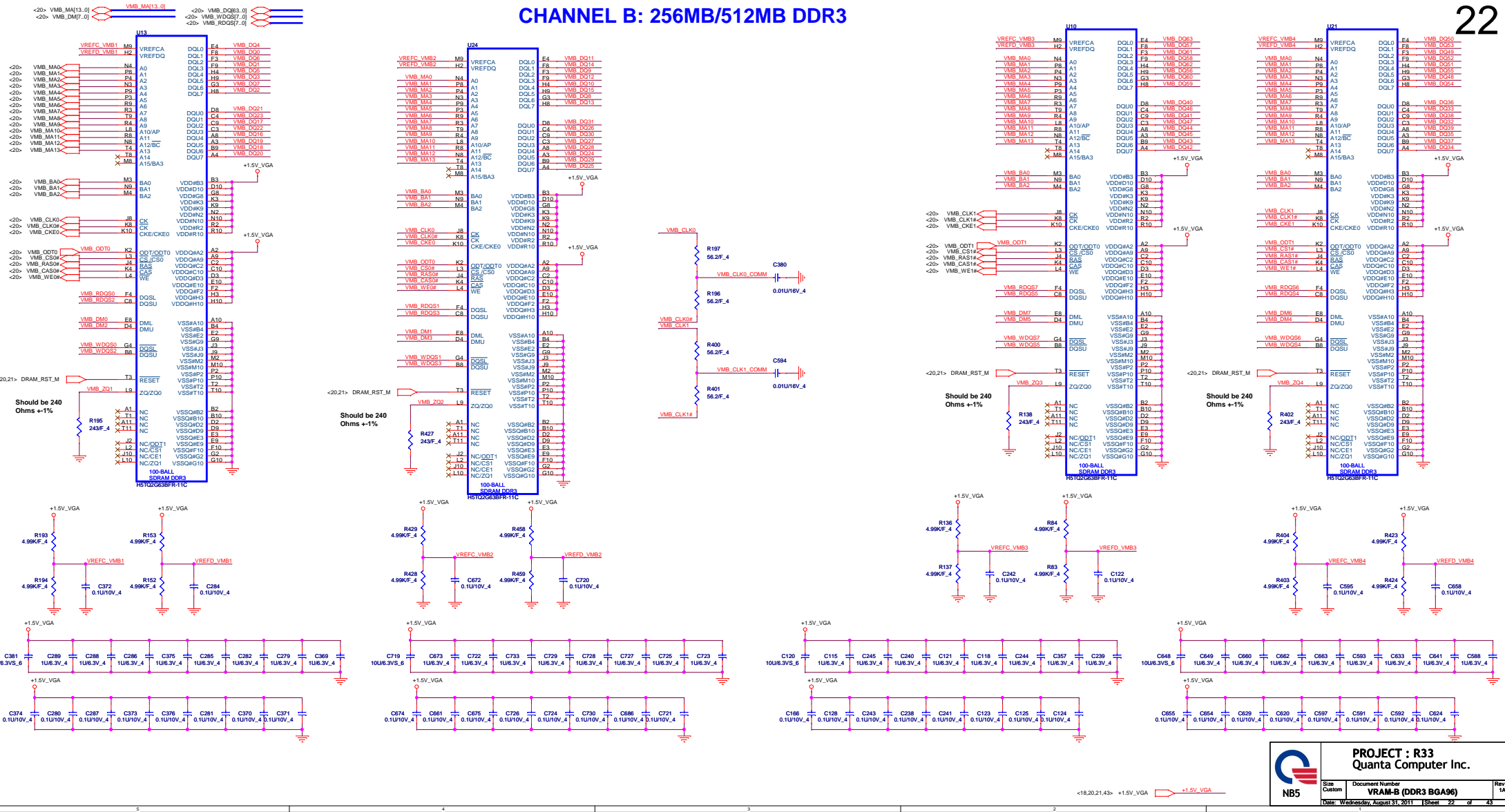


Table with 3 columns: Vendor, QCI PN, B/S PN. Rows include Hynix D(Vega), Micron G die, SAMSUNG G die, Hynix B(Vega), and SAMSUNG C die.



Project: R33 Quanta Computer Inc. NBS logo. Includes fields for Site Custom, Document Number VRAM-A (DDR3 BGA96), Date: Wednesday, August 31, 2011, Sheet 21 of 43, and Rev 3A.

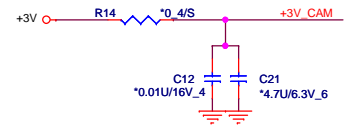
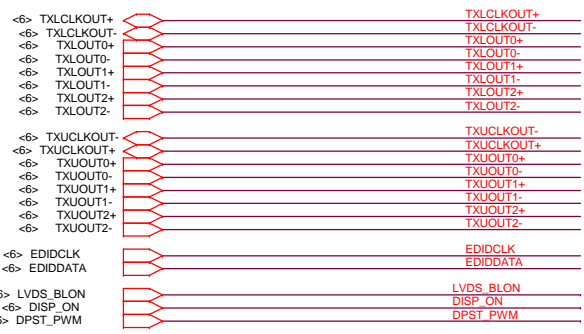
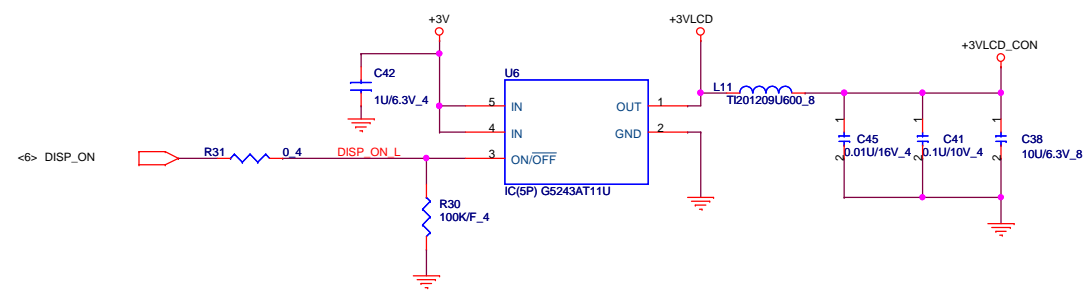
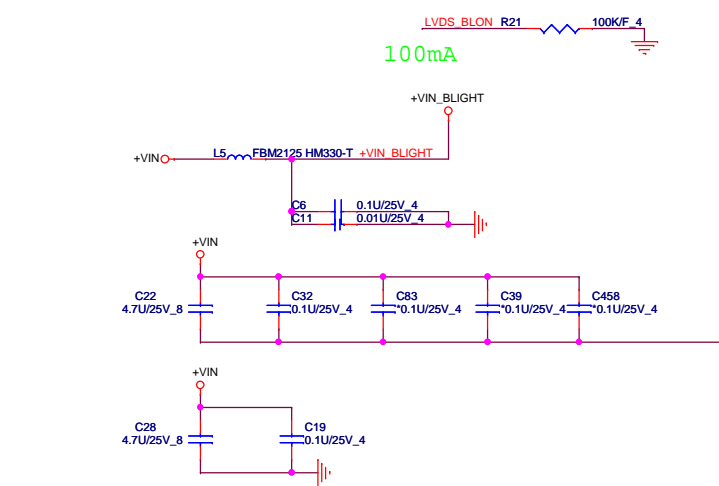
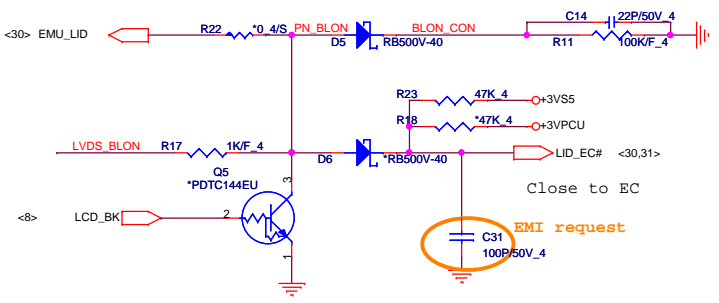
CHANNEL B: 256MB/512MB DDR3



PROJECT : R33
Quantia Computer Inc.

NB5	Site Custom	Document Number	Rev
		VRAM-B (DDR3 BGA96)	1A
	Date: Wednesday, August 31, 2011 Sheet 22 of 43		

LID Switch

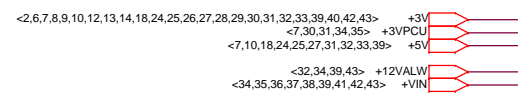
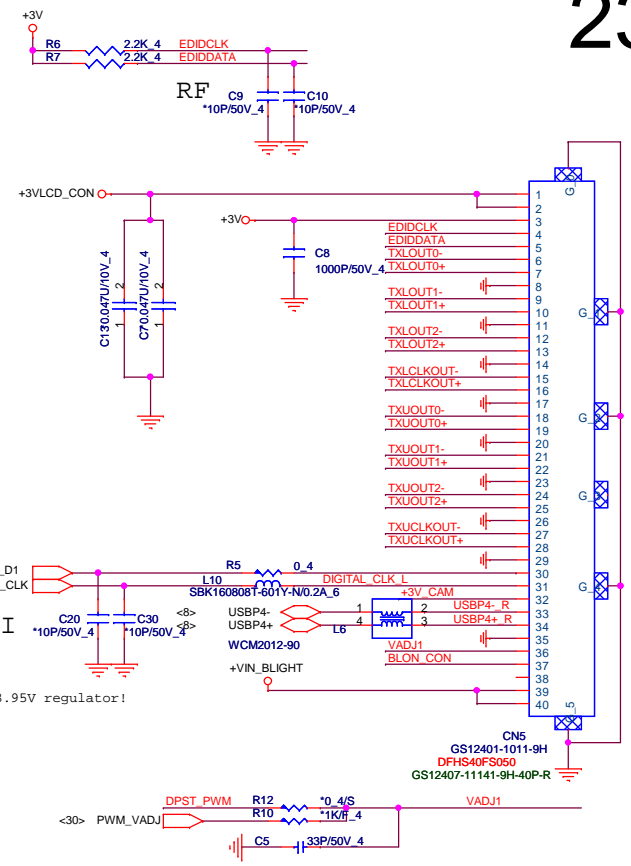


follow L6 location

USBP4- R8 *0.4 USBP4- R

USBP4+ R9 *0.4 USBP4+ R

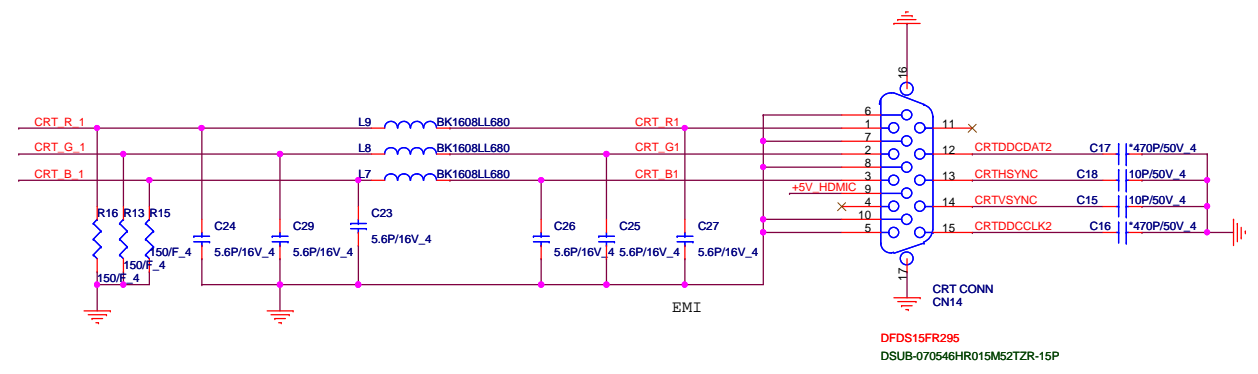
Please note that 2011 camera is +3V a We do not need to use 5V -> 3.95V regulator!



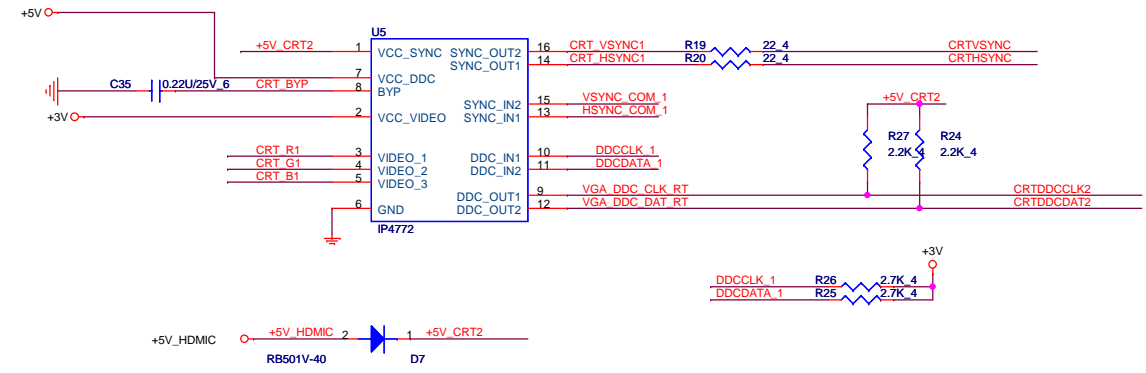
PROJECT : R33
Quanta Computer Inc.

Size Custom	Document Number LCD CONN/LID/CAM	Rev 1A
Date: Wednesday, August 31, 2011 Sheet 23 of 43		

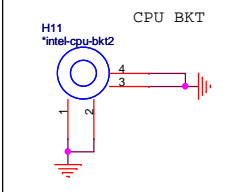
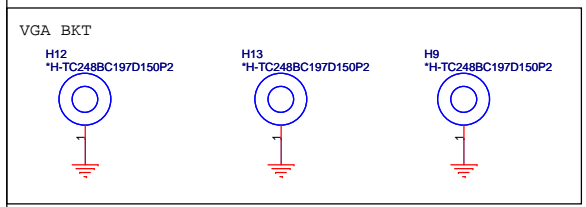
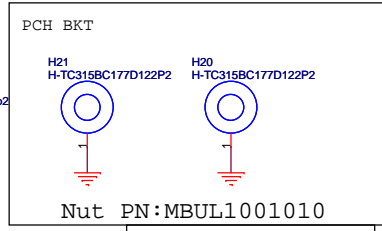
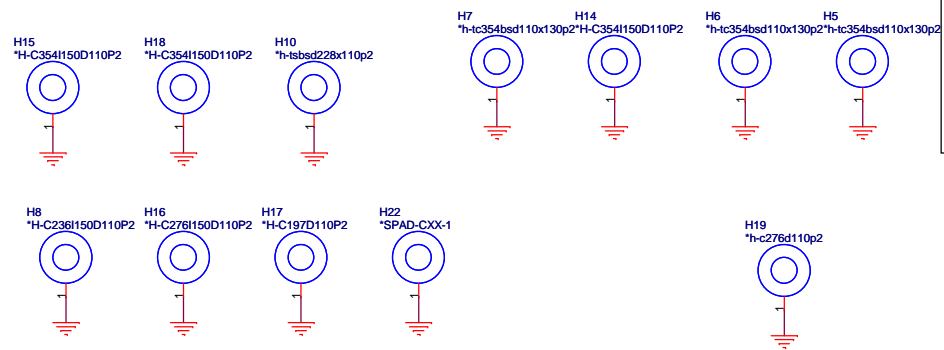
CRT PORT



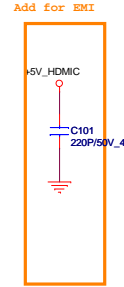
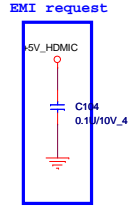
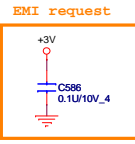
- <6> CRT_R
- <6> CRT_G
- <6> CRT_B
- <6> HSYNC_COM
- <6> VSYNC_COM
- <6> DDCCLK_1
- <6> DDCDATA_1



HOLE

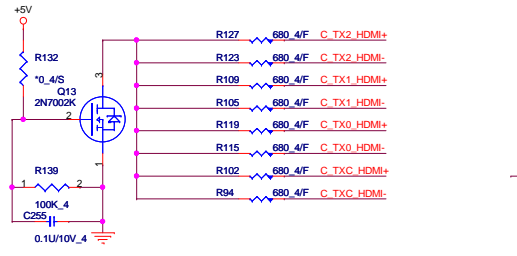
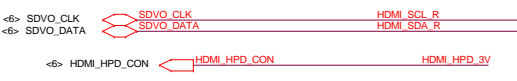


	PROJECT : R33 Quanta Computer Inc.	
	Size Custom	Document Number CRT,Hole
Date: Wednesday, August 24, 2011 Sheet 24 of 43		

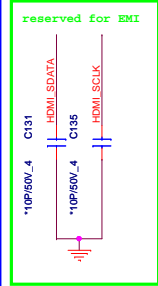
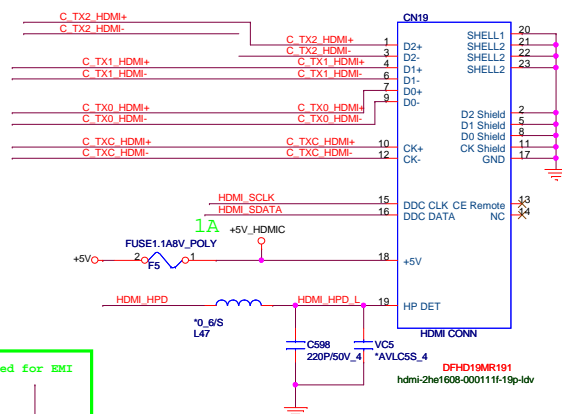
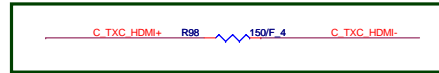
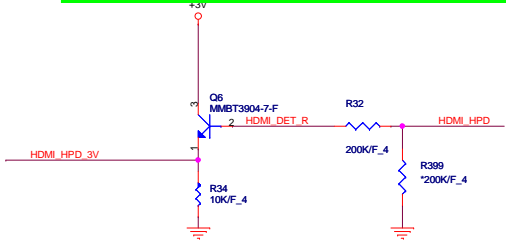
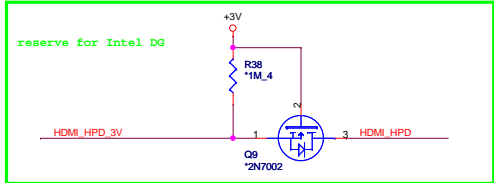
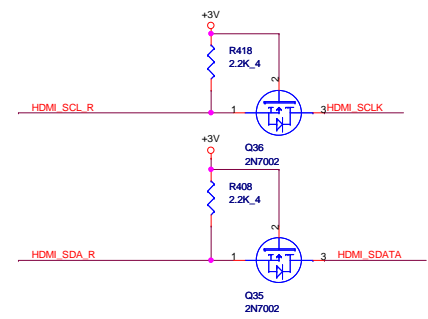


close to HDMI conn

<6>	IN_CLK#	IN_CLK#	C141	0.1U/10V_4	C TXC HDMI-
<6>	IN_CLK	IN_CLK	C148	0.1U/10V_4	C TXC HDMI+
<6>	IN_D0#	IN_D0#	C180	0.1U/10V_4	C TX0 HDMI-
<6>	IN_D0	IN_D0	C189	0.1U/10V_4	C TX0 HDMI+
<6>	IN_D1#	IN_D1#	C157	0.1U/10V_4	C TX1 HDMI-
<6>	IN_D1	IN_D1	C169	0.1U/10V_4	C TX1 HDMI+
<6>	IN_D2#	IN_D2#	C200	0.1U/10V_4	C TX2 HDMI-
<6>	IN_D2	IN_D2	C210	0.1U/10V_4	C TX2 HDMI+



DISCRETE HDMI I2C SELECT Close to HDMI Connector



NB5

PROJECT : R33
Quanta Computer Inc.

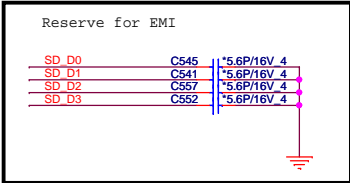
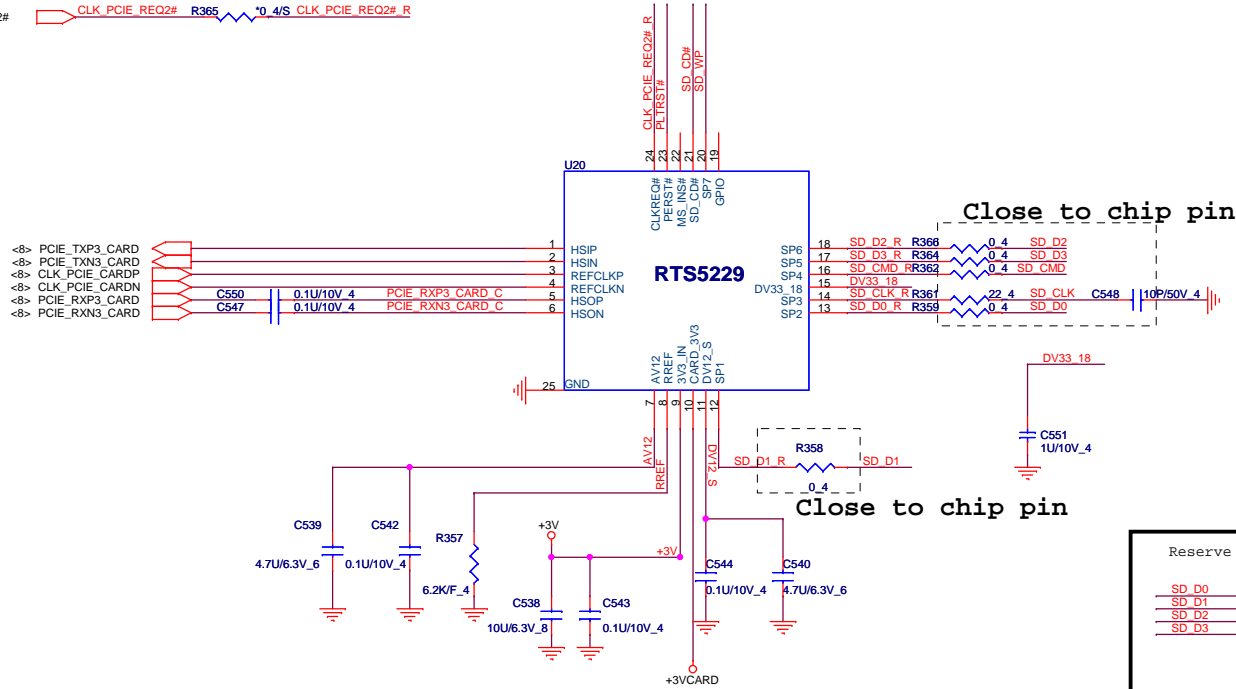
Size Custom Document Number
HDMI CONN

Date: Wednesday, August 24, 2011 Sheet 25 of 43

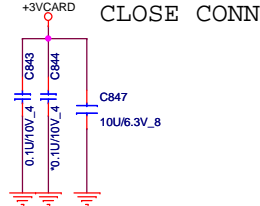
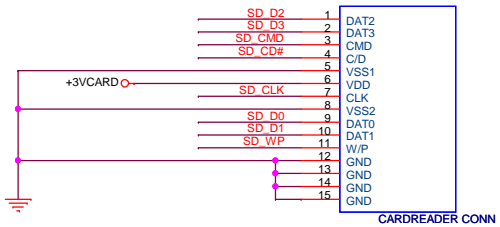
Rev
1A

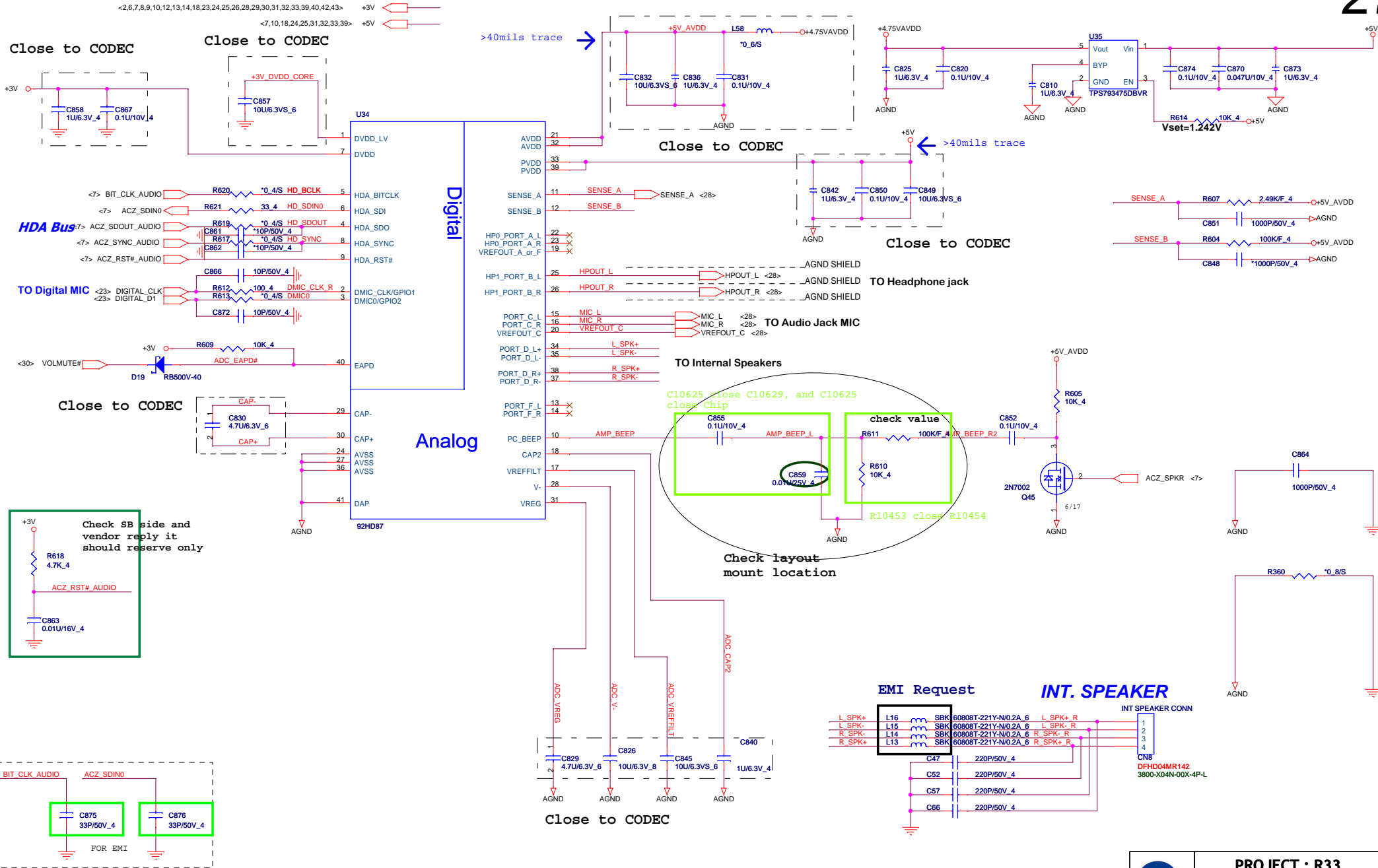
<2,8,14,29,30,33> PLTRST# 

<8> CLK_PCIE_REQ2#  R365 0.4/S CLK_PCIE_REQ2#_R

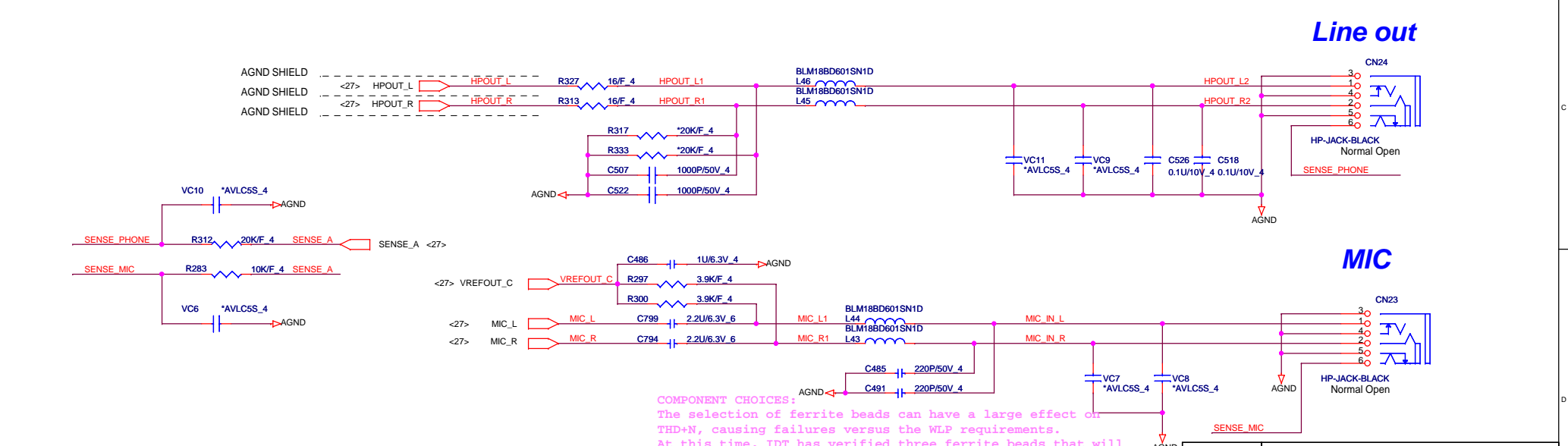
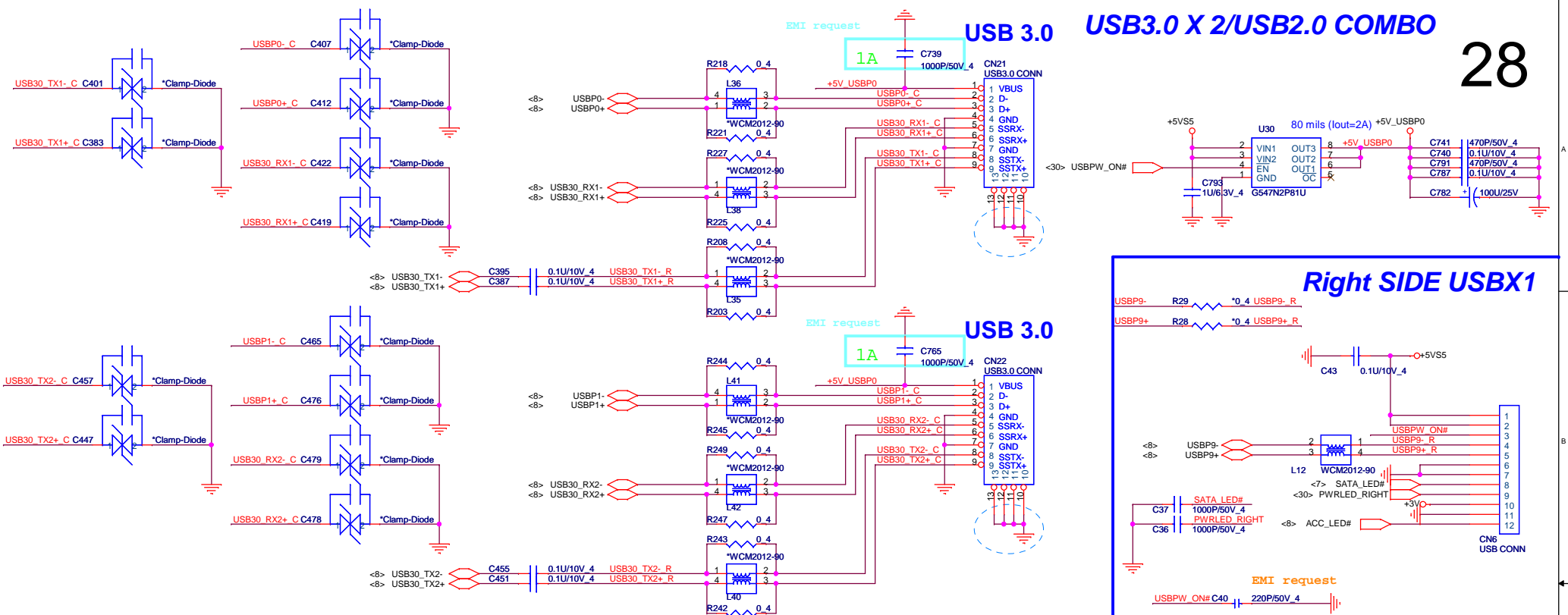


SD / MMC CARD READER






	PROJECT : R33 Quanta Computer Inc.	
	Size Custom Document Number Azalia 92HD80	Rev 1A
Date: Wednesday, August 31, 2011 Sheet 27 of 43		



COMPONENT CHOICES:
 The selection of ferrite beads can have a large effect on THD+N, causing failures versus the WLP requirements. At this time, IDT has verified three ferrite beads that will meet the WLP performance requirements:
 Murata: BLM18BD601SN1
 TDK: MMZ1608Y601BTA
 Taiyo Yuden: LF BK 1608HM601-T

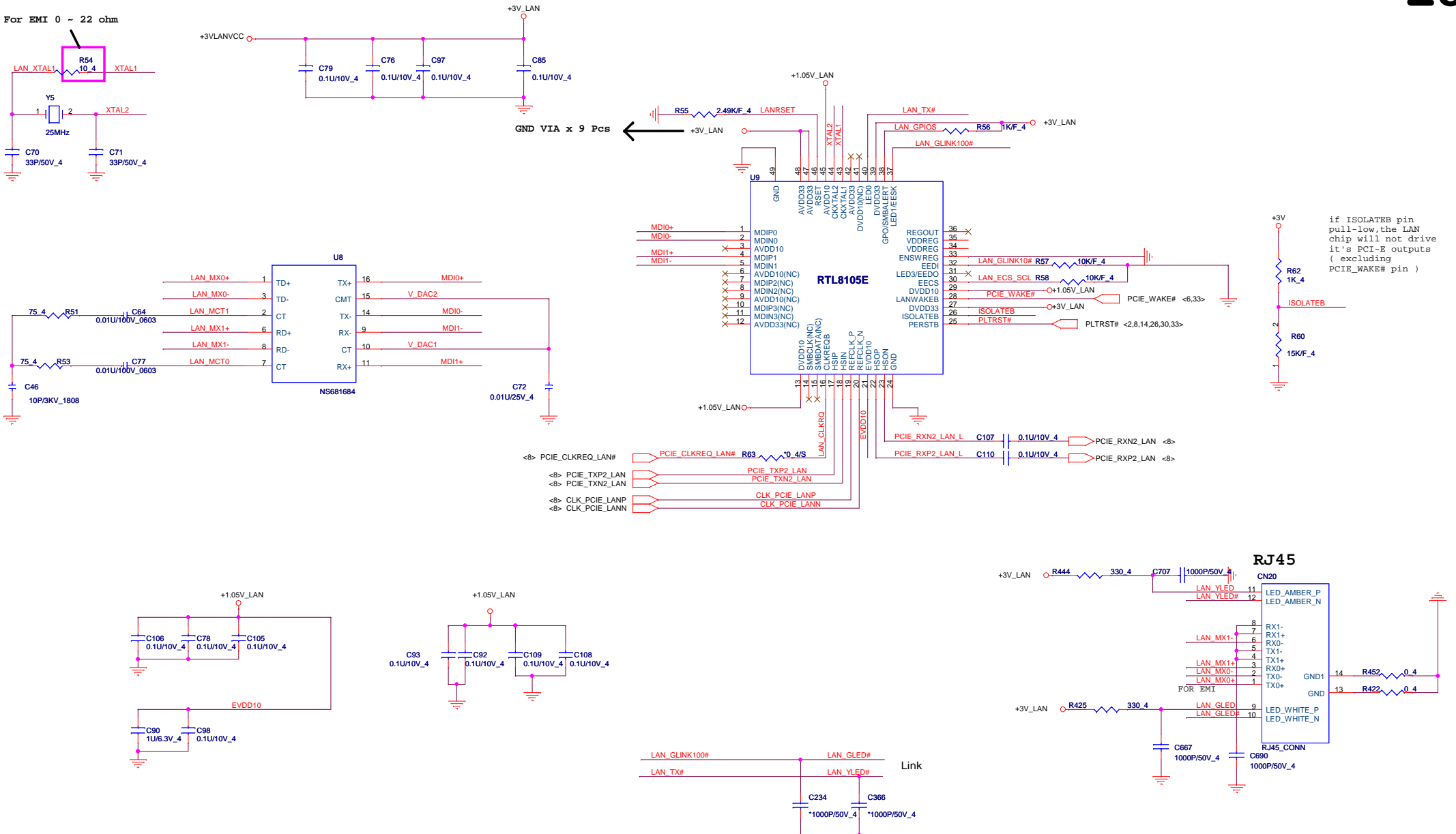


NB5

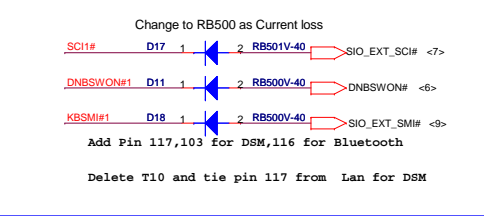
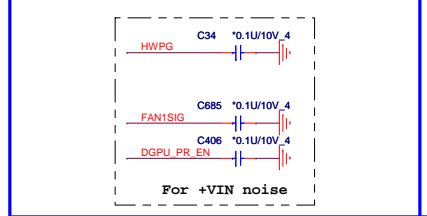
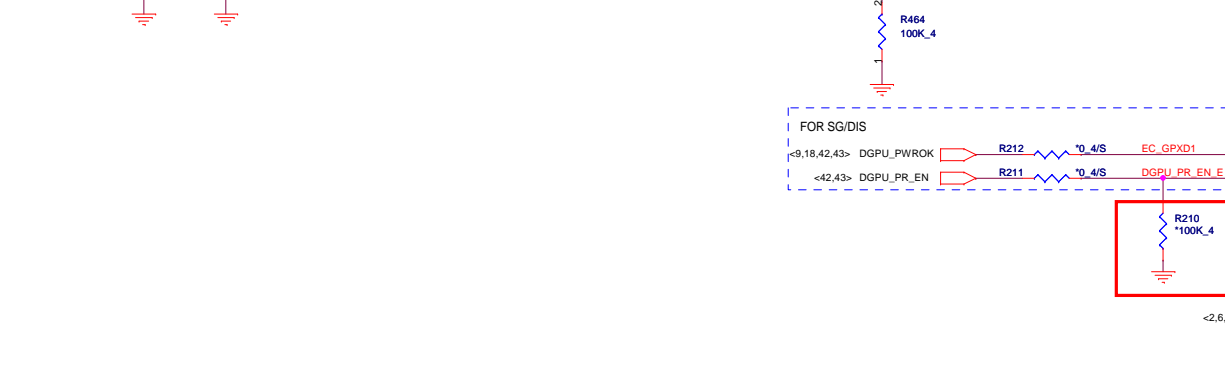
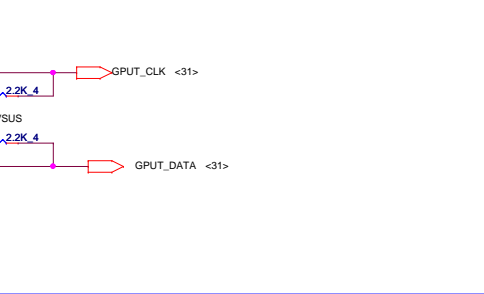
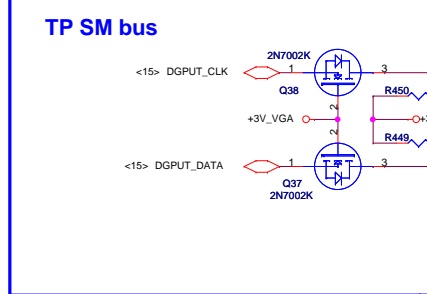
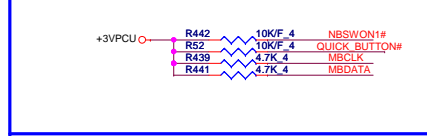
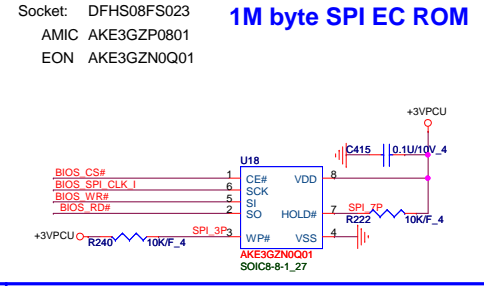
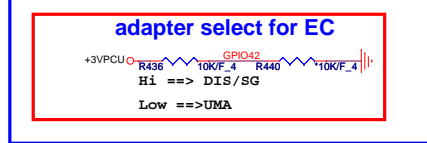
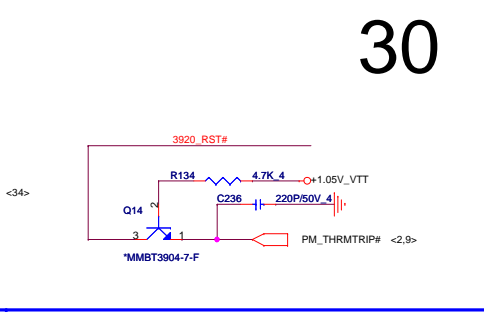
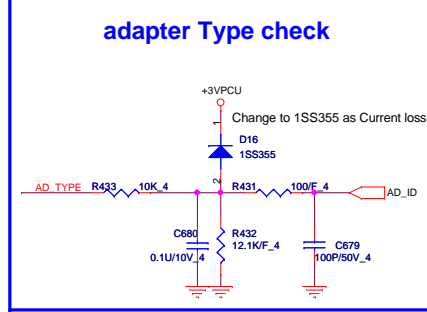
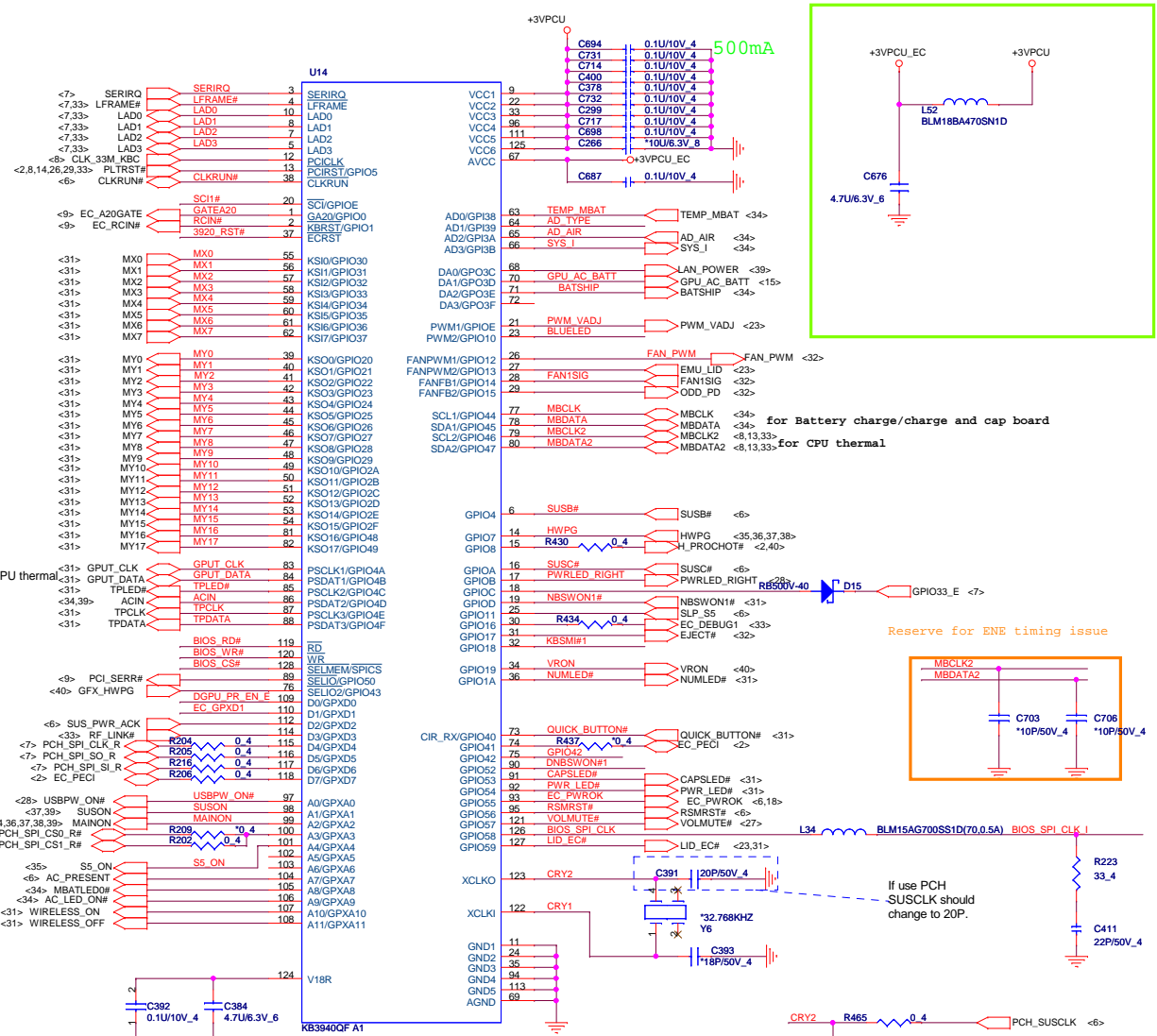
PROJECT : R33
 Quanta Computer Inc.

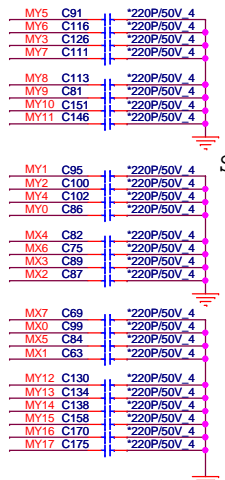
Rev 1A

Size Custom	Document Number USB/BT/Audio Jack	Rev 1A
Date: Monday, August 29, 2011 Sheet 28 of 43		

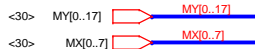
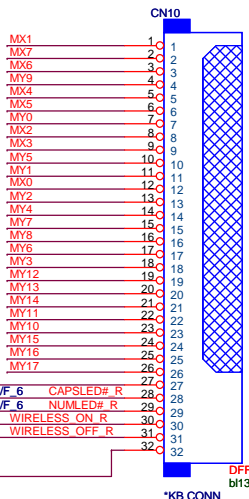


	PROJECT : R33	
	Quanta Computer Inc.	
	Size Custom	Document Number RTL 8105E/RJ45
Date: Wednesday, August 24, 2011 Sheet 29 of 43		

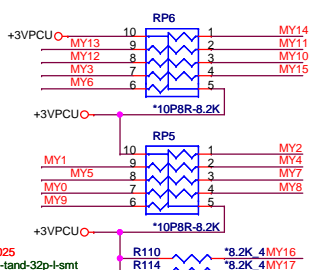




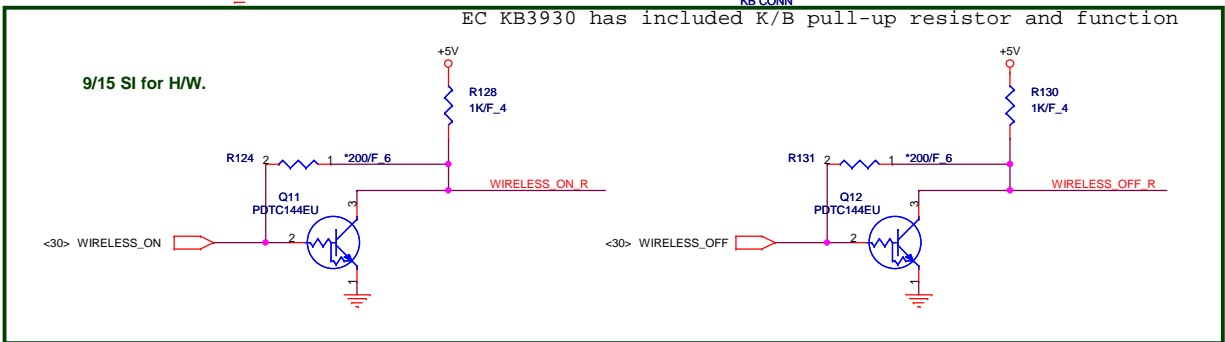
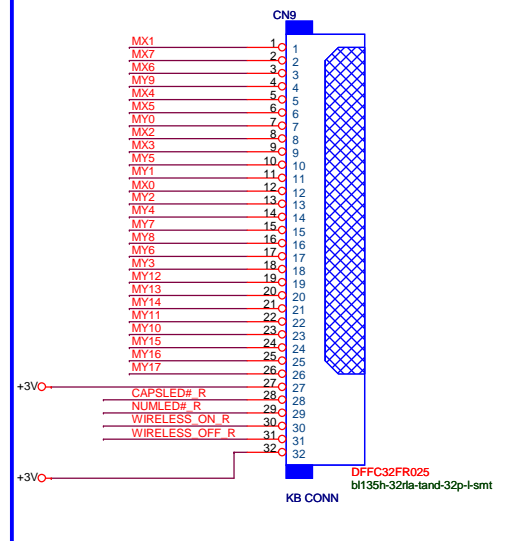
SI un-install



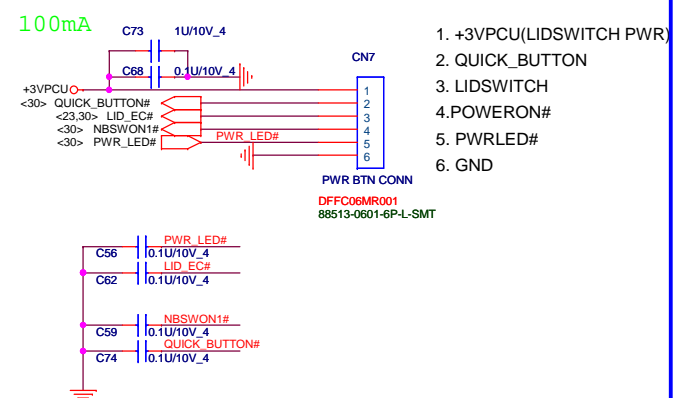
KEYBOARD PULL-UP



KEYBOARD Con.
Co-layout for 17" only

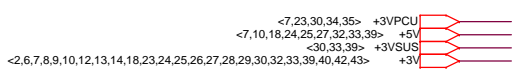
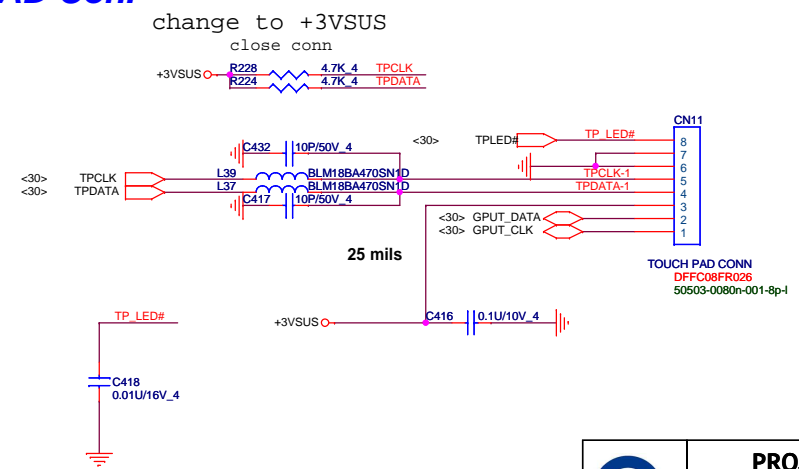


POWER BUTTON CONNECT



1. +3VPCU(LIDSWITCH PWR)
2. QUICK_BUTTON
3. LIDSWITCH
4. POWERON#
5. PWRLED#
6. GND

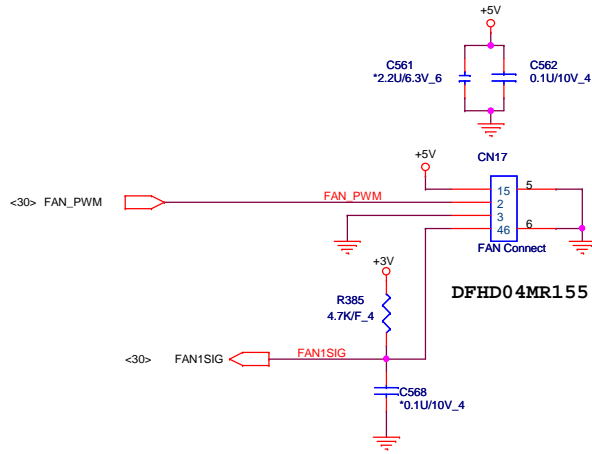
TOUCH PAD Con.



PROJECT : R33
Quanta Computer Inc.

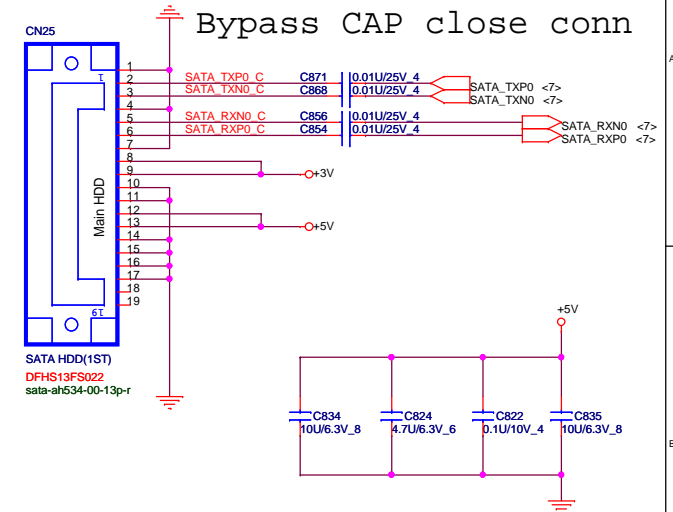
Size Custom	Document Number LED/KB/SW/TP	Rev 1A
Date: Wednesday, August 24, 2011 Sheet 31 of 43		

CPU FAN

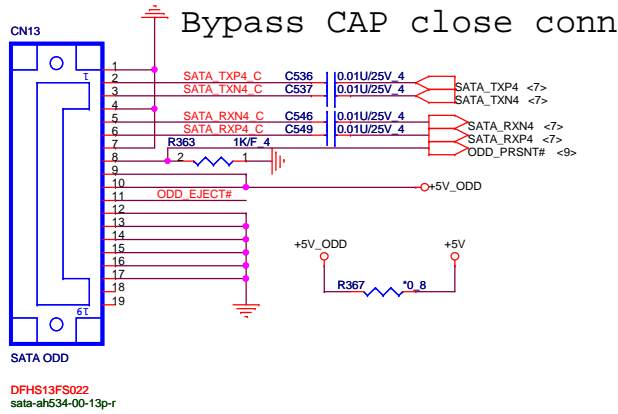


SATA HDD CONNECTOR

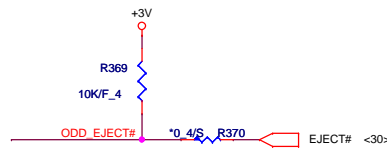
32



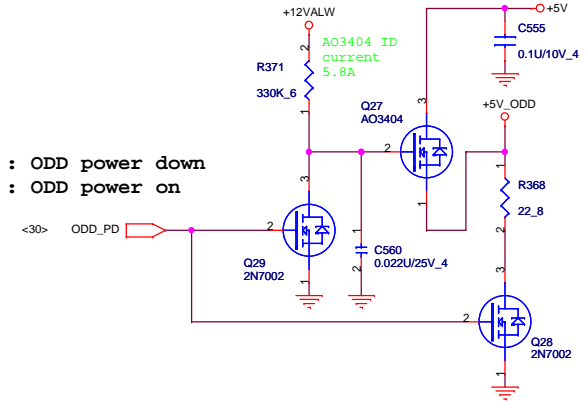
SATA ODD CONNECTOR



follow INTEL DG change eject PU to +3V.



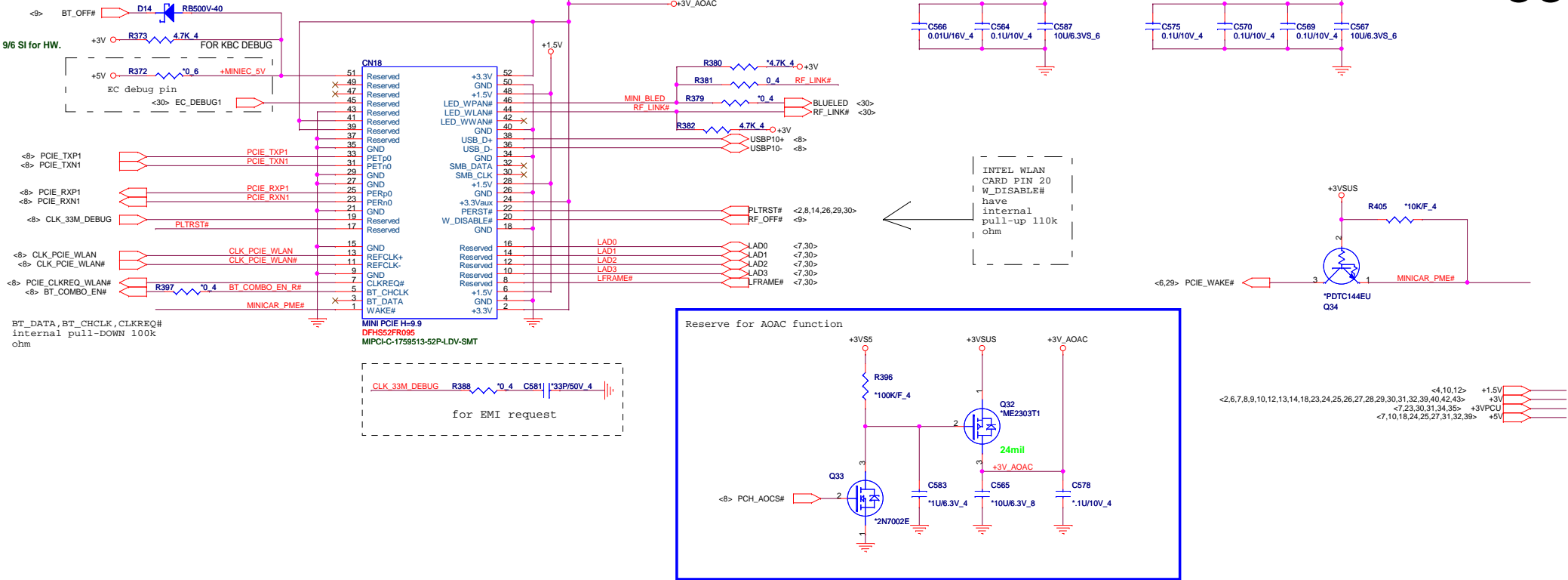
High : ODD power down
Low : ODD power on



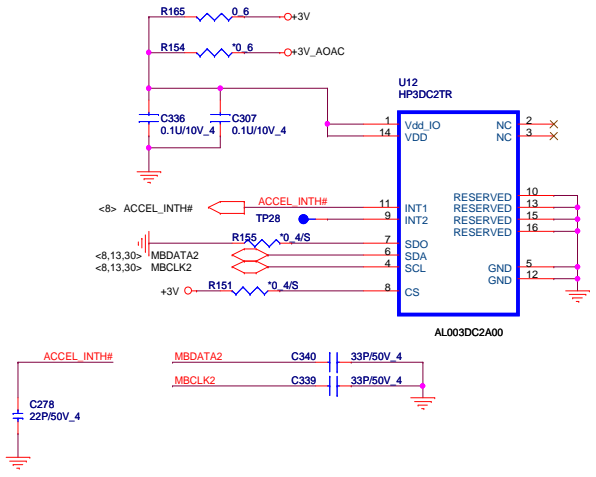
PROJECT : R33
Quanta Computer Inc.

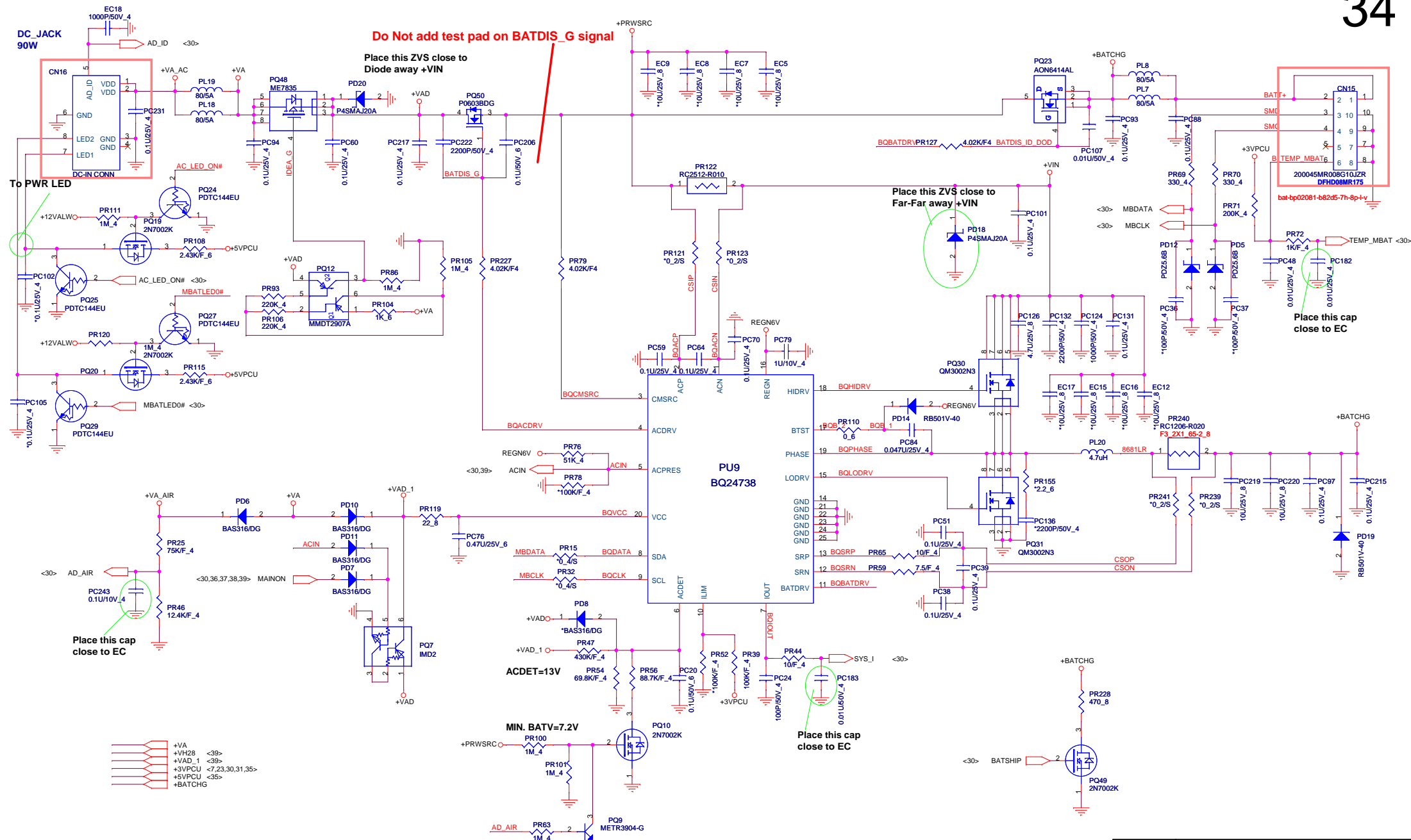
Size Custom	Document Number HDD/ODD/FAN	Rev 1A
Date: Thursday, August 25, 2011		Sheet 32 of 43

Mini PCI-E Card 1 WLAN



Accelerometer Sensor



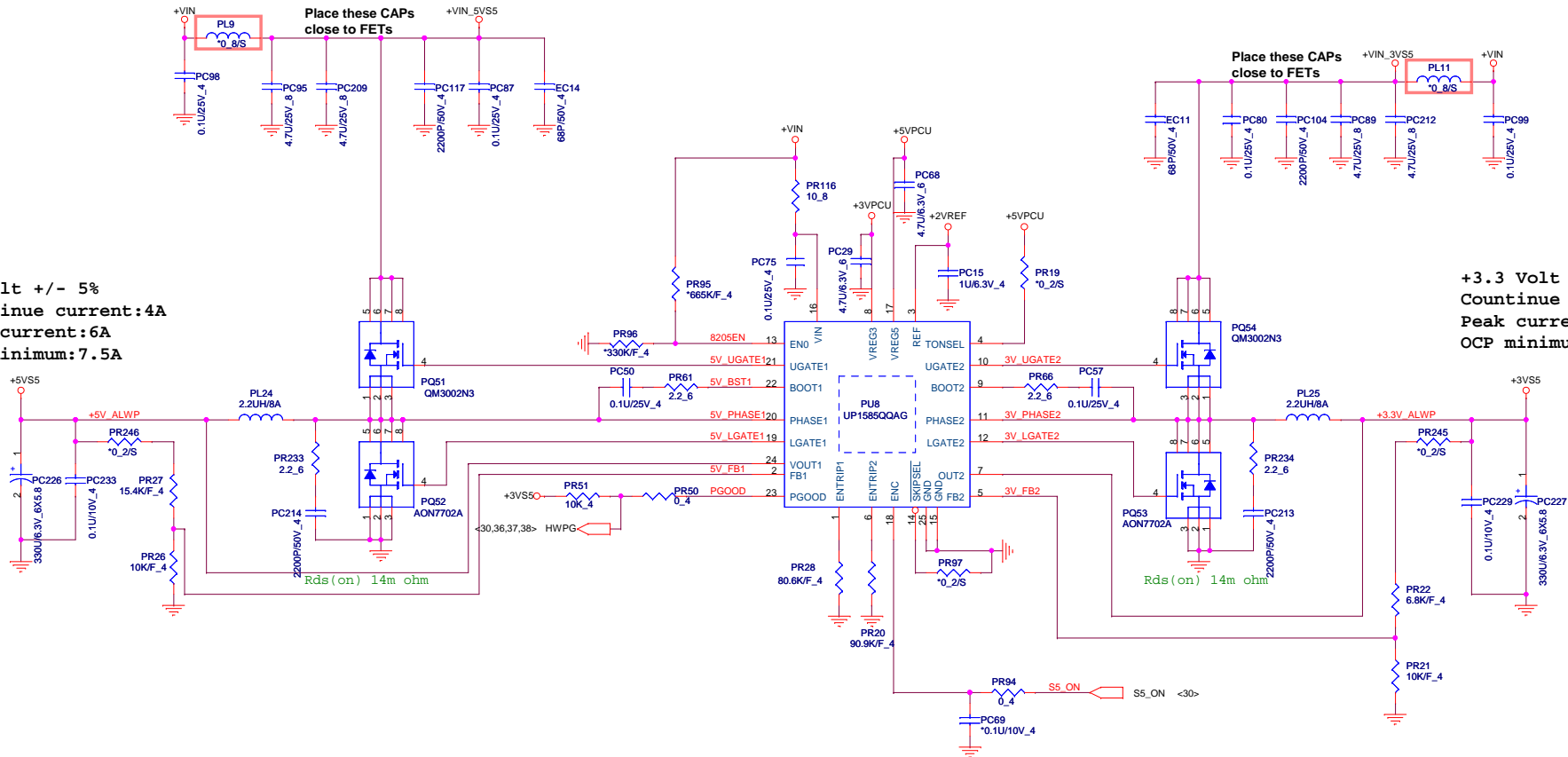



- +VA
- +VH28
- +VAD_1
- +3VPCU
- +5VPCU
- +BATCHG
- +BATSHIP

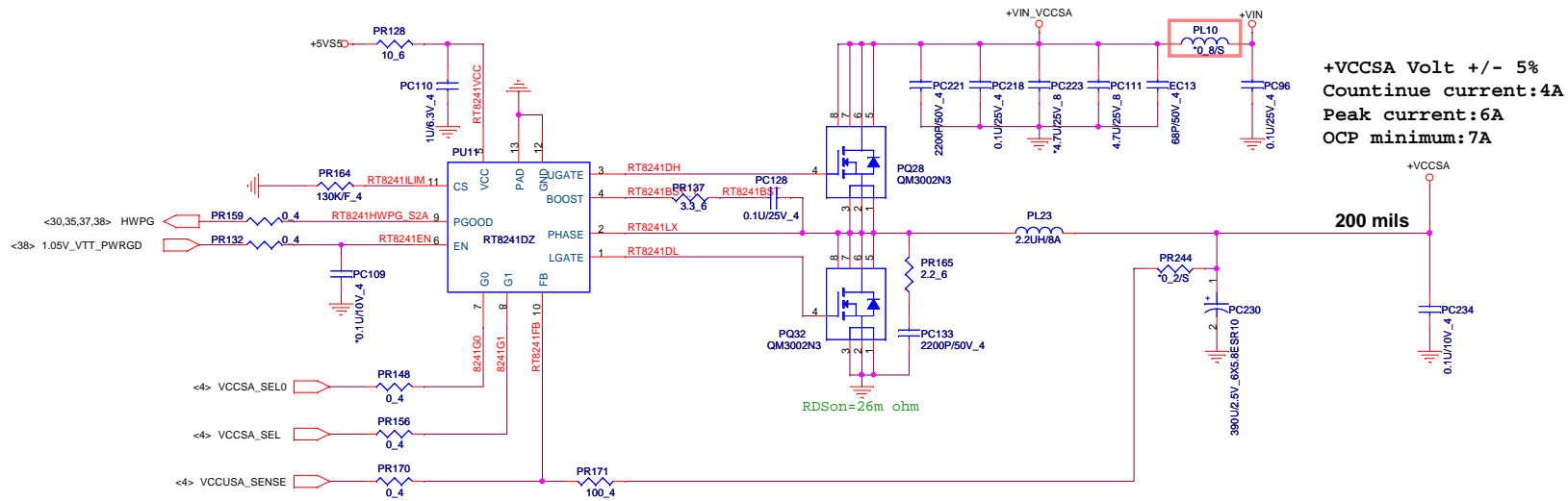
	PROJECT : R33	
	Quanta Computer Inc.	
	Size Custom	Document Number Charger (OZ8681)
Date: Wednesday, August 31, 2011 Sheet 34 of 43		

+5 Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A

+3.3 Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A

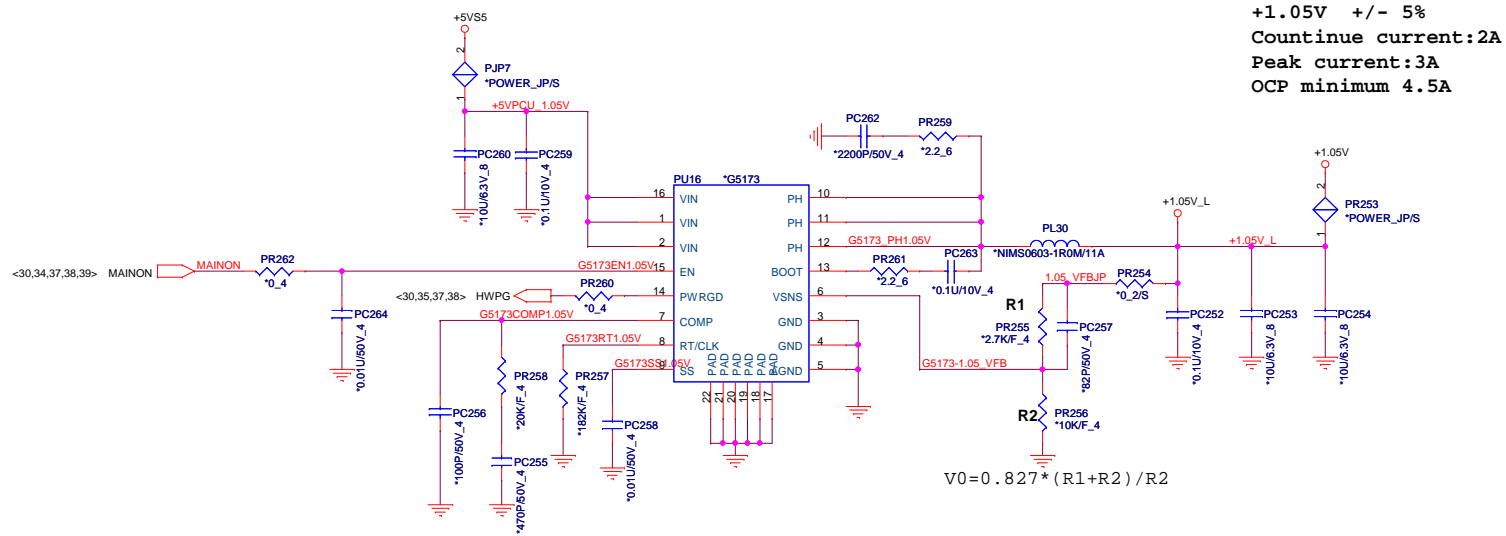


	PROJECT : R33 Quanta Computer Inc.		
	Size Custom	Document Number 3/5VPCU(RT8223P)	Rev 1A
	Date: Monday, August 29, 2011	Sheet	35 of 43

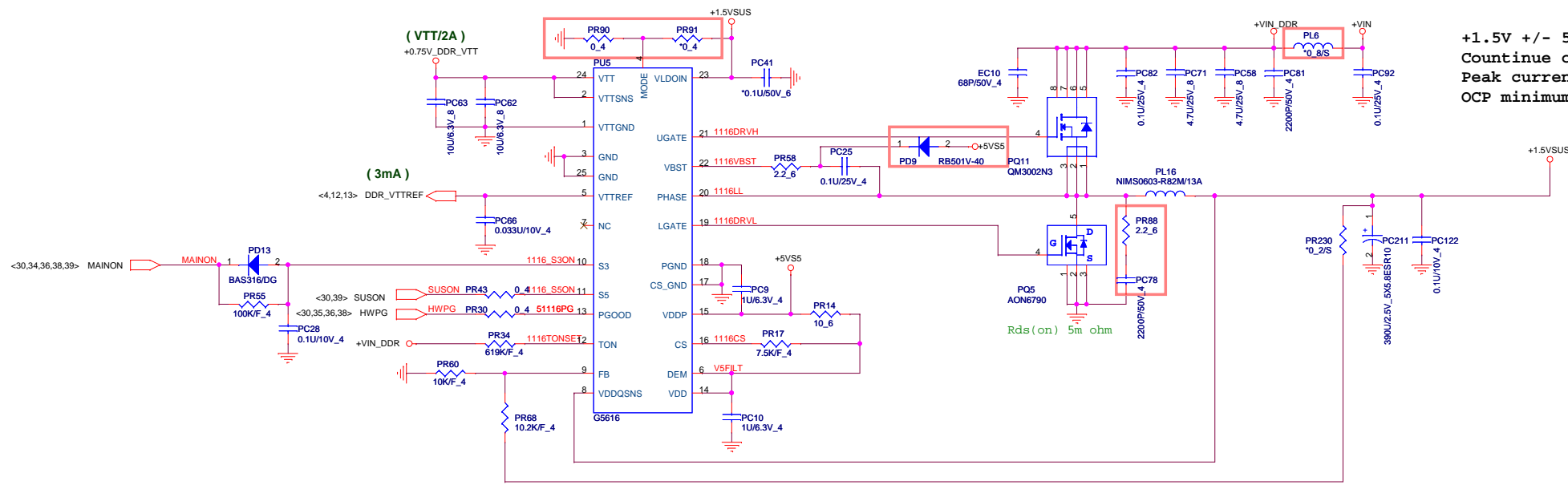


**CPU system agent
 voltage slew rate of 0.5 -10 mV/μs**


H_FC_C22	VCCSA_SEL	Vout
VID0	VID1	
0	0	0.9V
0	1	0.80V (SV-RT8241DZGQW) 0.85V (LV-RT8241EZGQW)
1	0	0.725V
1	1	0.675V

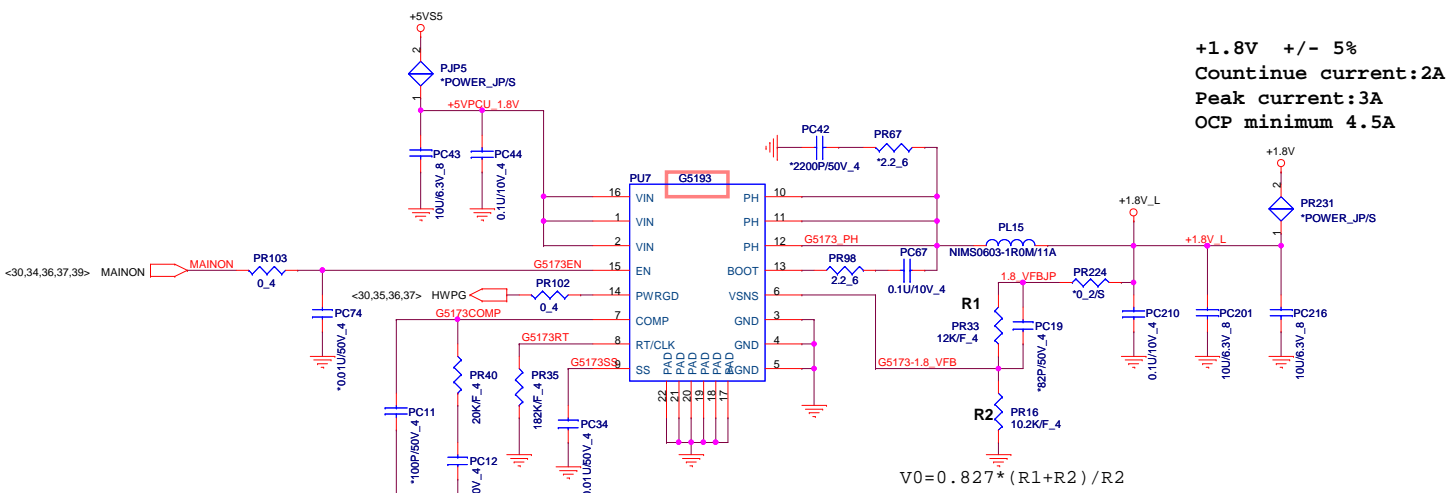
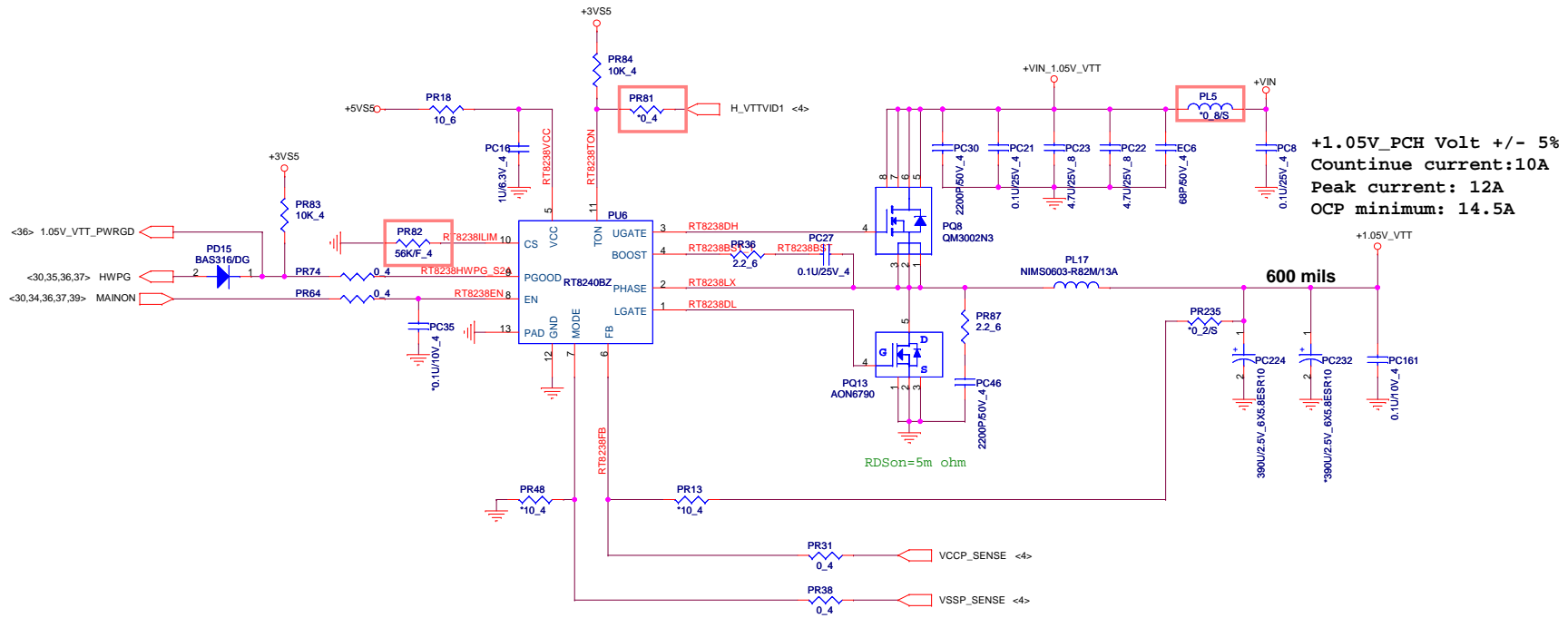



	PROJECT : R33		Date: Monday, August 29, 2011
	Quanta Computer Inc.		
	Size Custom Document Number VCCSA (RT8241EZ) Date:	Rev 1A Sheet 36 of 43	

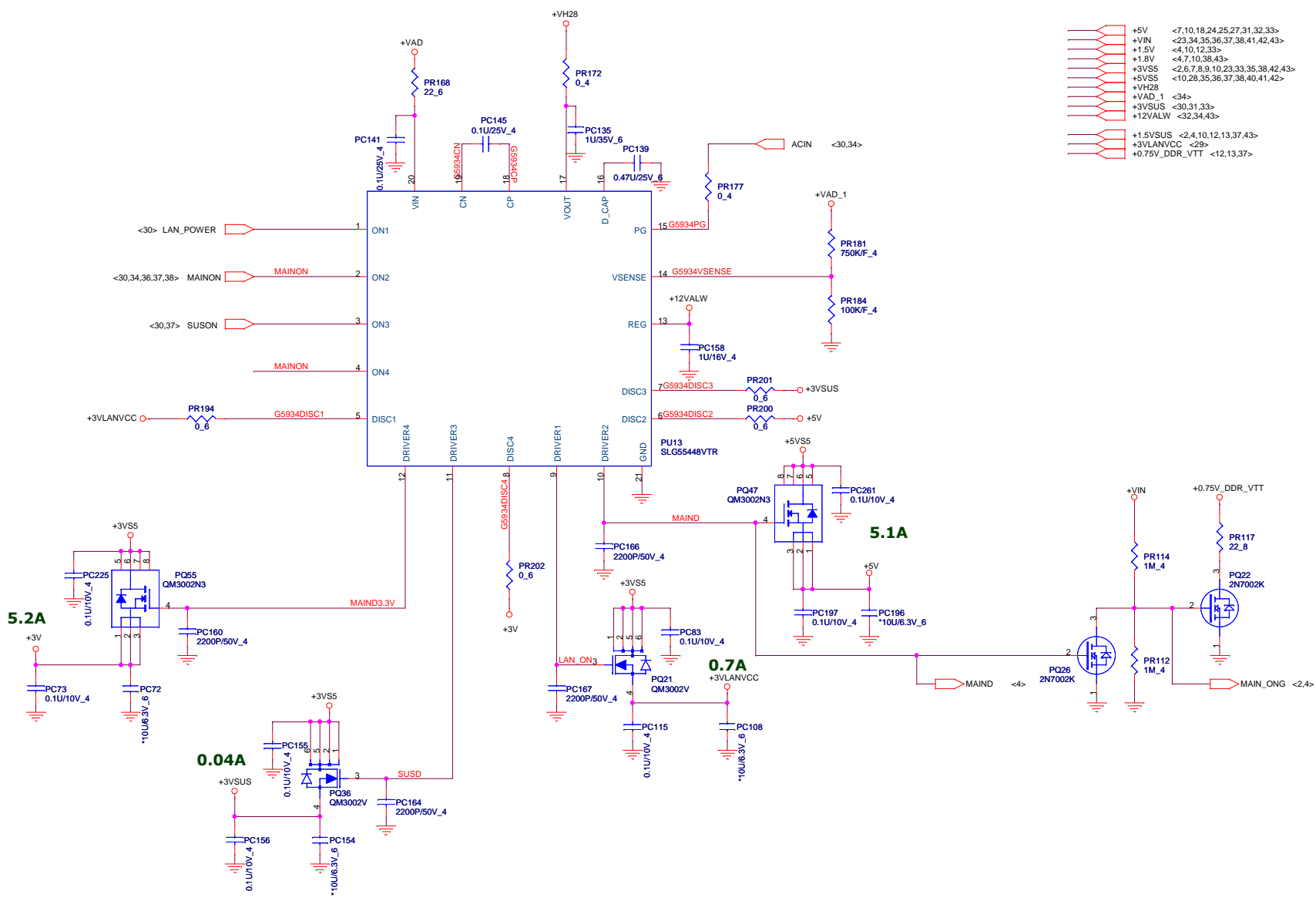


+1.5V +/- 5%
 Countinue current:10A
 Peak current:12A
 OCP minimum 15A

	PROJECT : R33		
	Quanta Computer Inc.		
	Size Custom	Document Number DDRIII(RT8207LGQW)	Rev 1A
Date: Wednesday, August 31, 2011		Sheet 37 of 43	

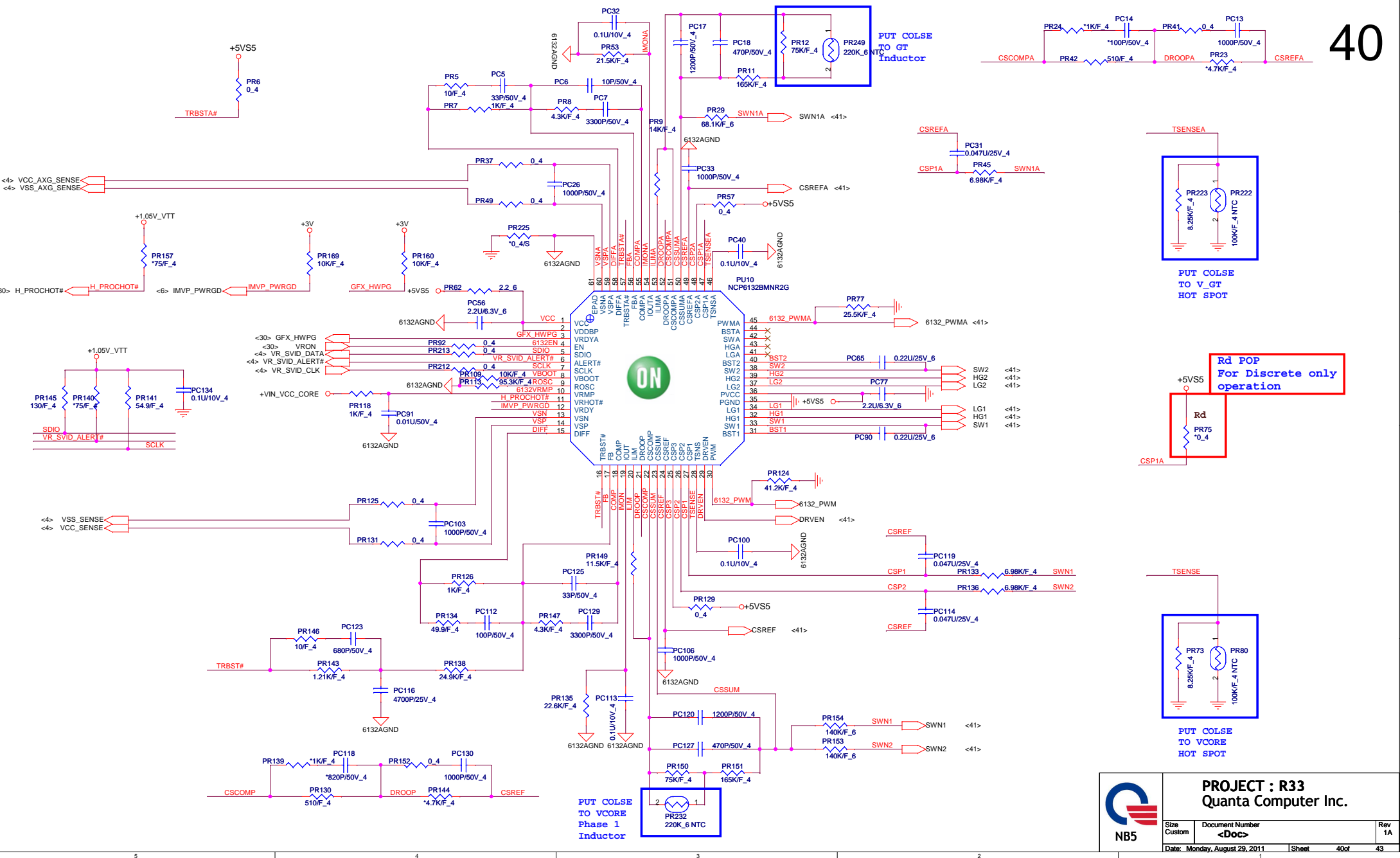


	PROJECT : R33 Quanta Computer Inc.		
	Size Custom	Document Number 1.0V(RT8228BZ)/1.8V(G5173)	Rev 1A
	Date: Wednesday, August 31, 2011 Sheet 36 of 43		

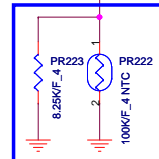


- +5V <7,10,18,24,25,27,31,32,33>
- +VIN <23,34,35,36,37,38,41,42,43>
- +1.5V <4,10,12,33>
- +1.8V <4,7,10,38,43>
- +3VS5 <2,6,7,8,9,10,23,33,35,38,42,43>
- +5VS5 <10,28,35,36,37,38,40,41,42>
- +VH28
- +VAD_1 <34>
- +3VSUS <30,31,33>
- +12VALW <32,34,43>
- +1.5VSUS <2,4,10,12,13,37,43>
- +3VLANVCC <29>
- +0.75V_DDR_VTT <12,13,37>

	PROJECT : R33		Rev 1A
	Quanta Computer Inc.		
	Size Custom	Document Number Dis-charge IC (G5934)	
Date: Monday, August 29, 2011 Sheet 39 of 43			

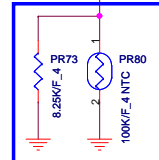
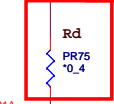


PUT COLSE
TO GT
Inductor



PUT COLSE
TO VGT
HOT SPOT

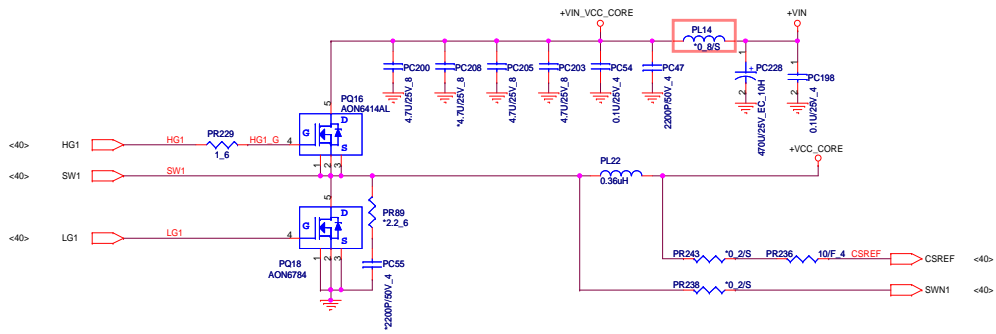
Rd POP
For Discrete only
operation



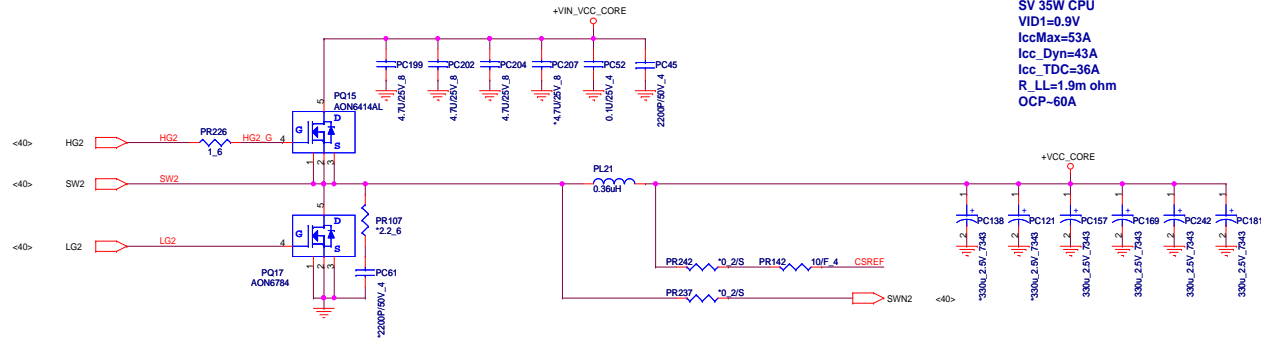
PUT COLSE
TO VCORE
HOT SPOT



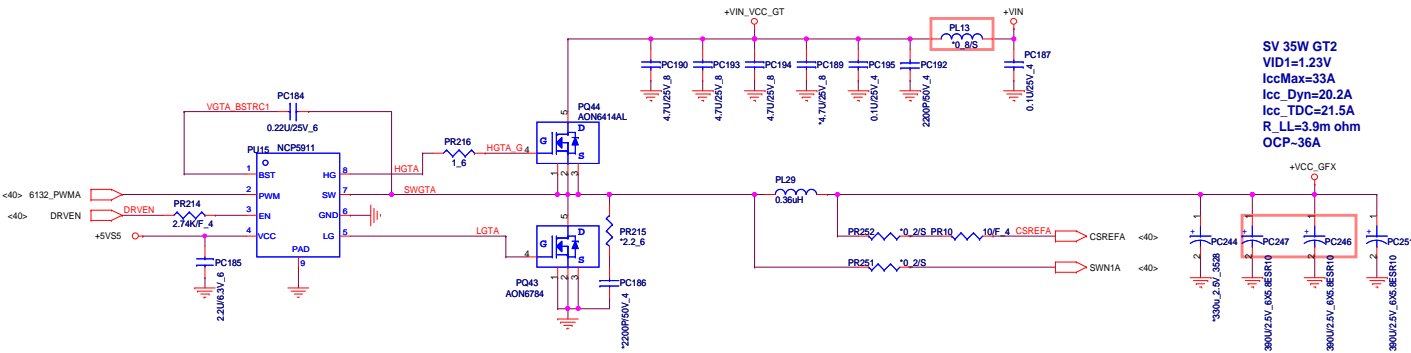
PROJECT : R33		
Quanta Computer Inc.		
Size Custom	Document Number <Doc>	Rev 1A
Date: Monday, August 29, 2011	Sheet 40 of	43

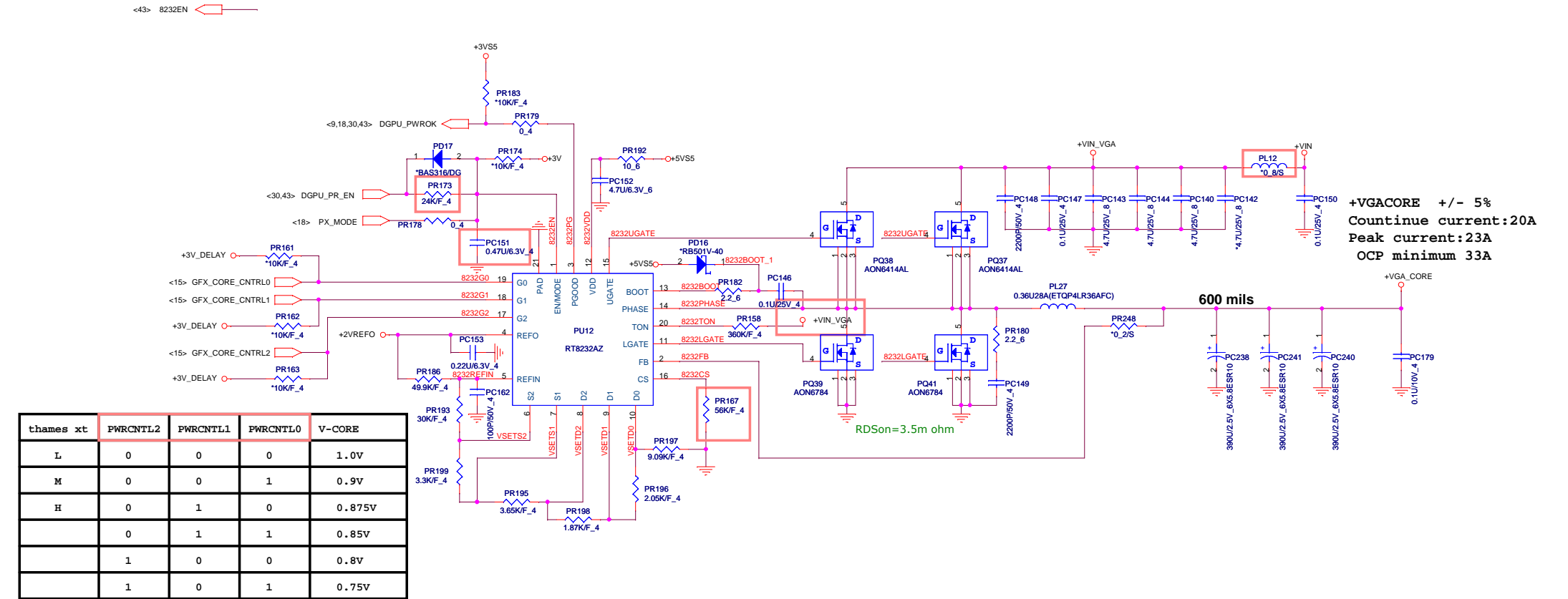


SV 35W CPU
 VID1=0.9V
 IccMax=53A
 Icc_Dyn=43A
 Icc_TDC=36A
 R_LL=1.9m ohm
 OCP=60A



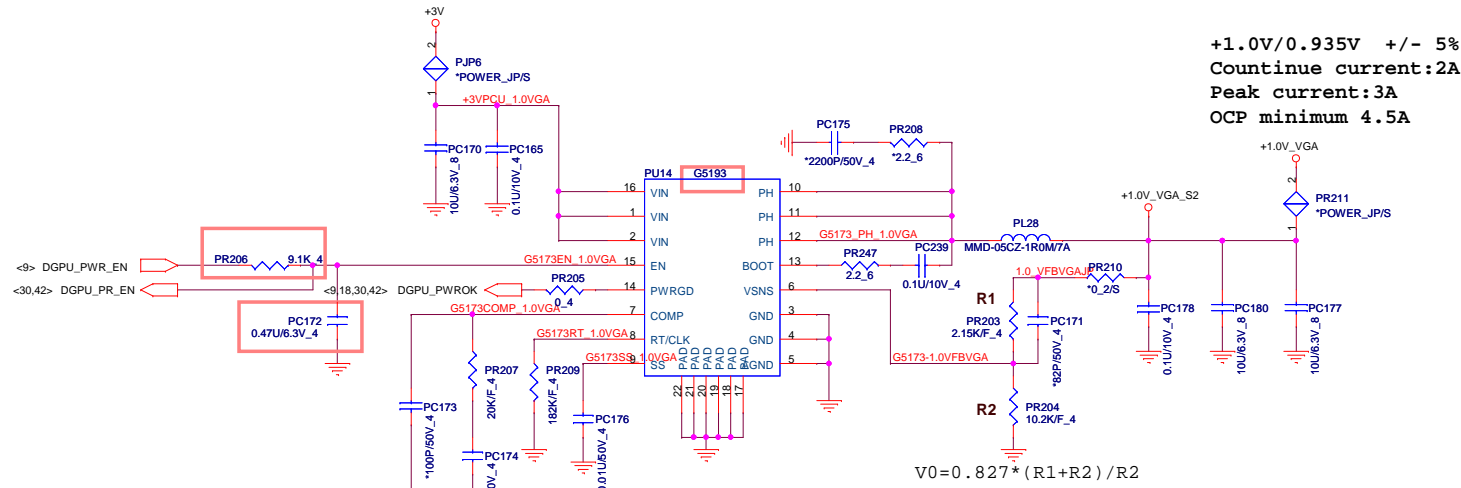
SV 35W GT2
 VID1=1.23V
 IccMax=33A
 Icc_Dyn=20.2A
 Icc_TDC=21.5A
 R_LL=3.9m ohm
 OCP=36A





thames xt	PWRCNTL2	PWRCNTL1	PWRCNTL0	V-CORE
L	0	0	0	1.0V
M	0	0	1	0.9V
H	0	1	0	0.875V
	0	1	1	0.85V
	1	0	0	0.8V
	1	0	1	0.75V

	PROJECT : R33 Quanta Computer Inc.		
	Size Custom	Document Number +VGA_CORE (RT8208/1.8V)	Rev 1A
	Date: Monday, August 29, 2011		Sheet 42 of 43

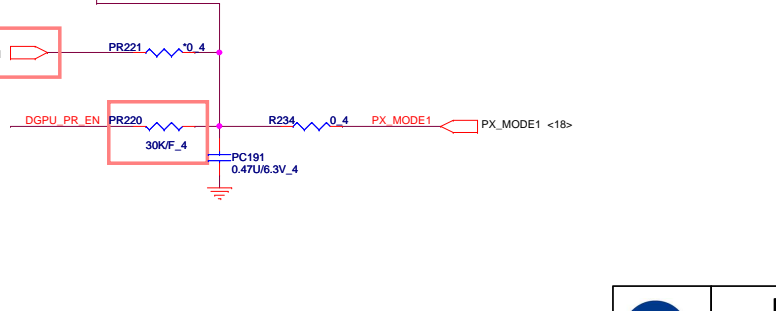
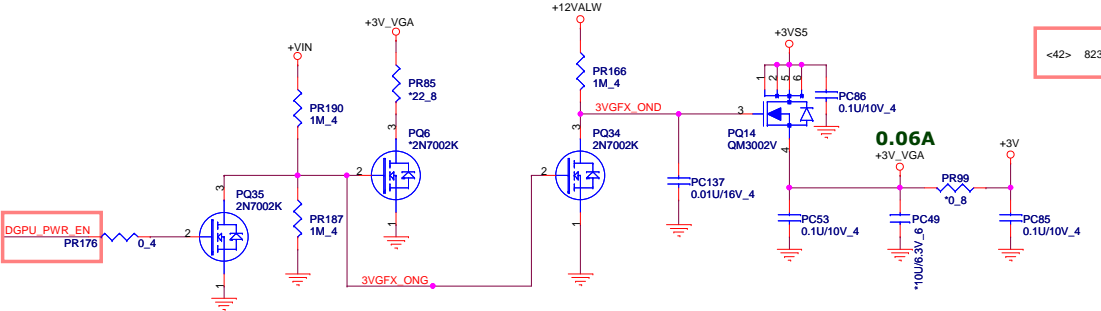
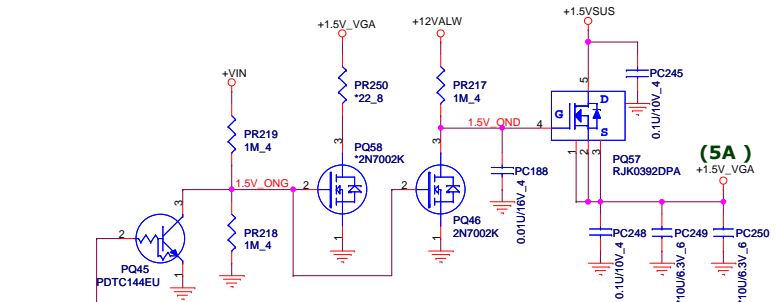
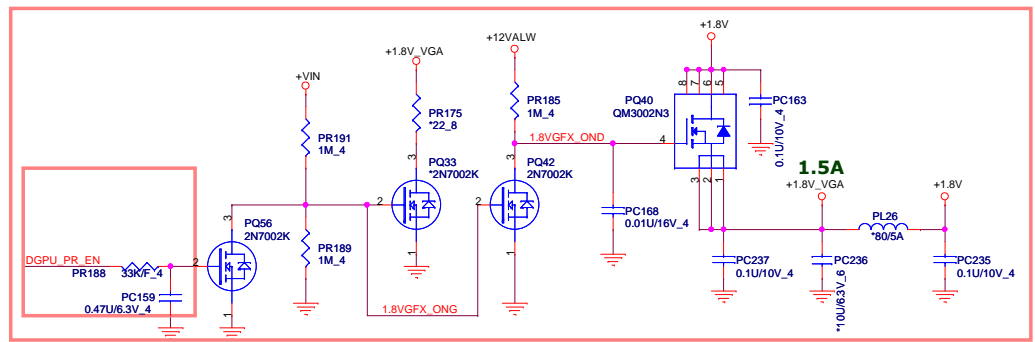


+1.0V/0.935V +/- 5%
Continue current:2A
Peak current:3A
OCV minimum 4.5A

- +3V <2,6,7,8,9,10,12,13,14,18,23,24,25,27,28,29,30,31,32,33,39,40,42>
- +VIN <23,34,35,36,37,38,39,41,42>
- +1.8V <4,7,10,38>
- +3V/SS <2,6,7,8,9,10,23,33,35,38,39,42>
- +5VSS <10,23,35,36,37,38,39,40,41,42>
- +3V_VGA <18>
- +12VALW <32,34,39>
- +1.5V/SUS <2,4,10,12,13,37>
- +1.5V_VGA <18,20,21,22>
- +1.8V_VGA <15,16,18,19>
- +3V_DELAY <15,17,18,42>
- +VGA_CORE <18,42>

$$V0 = 0.827 * (R1 + R2) / R2$$

Symour-XT	Voltage level	R1 Value	R1 P/N
17W	1.0V	2.15K	CS22152FB07
25W	0.935V	1.37K	CS21372FB19



PROJECT : R33
Quanta Computer Inc.

Size Custom	Document Number +VGCORE (RT8208/1.8V)	Rev 1A
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