
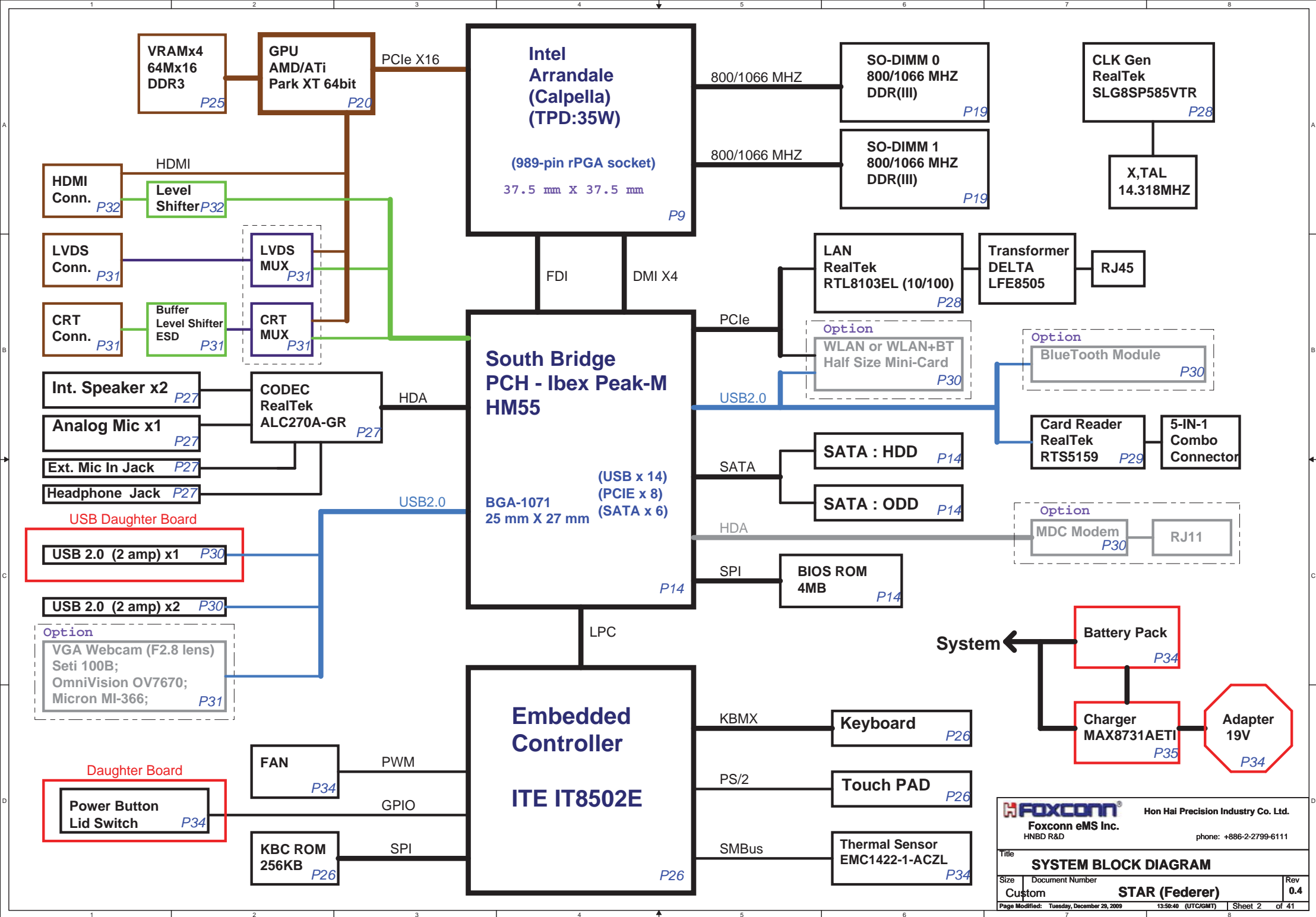
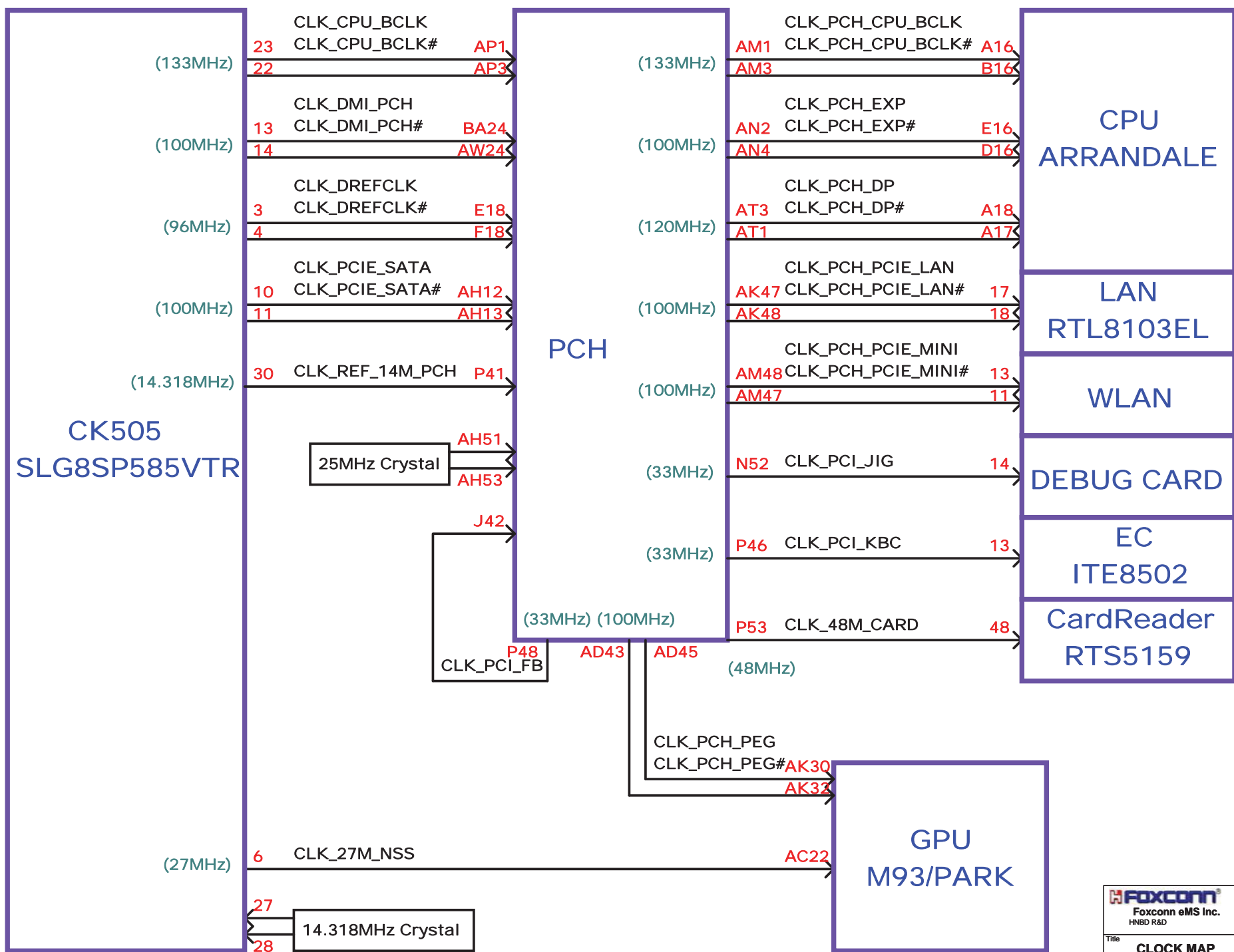


01	--	COVER SHEET	21	--	VGA_S3 (IO) 2/5
02	--	SYSTEM BLOCK DIAGRAM	22	--	VGA_S3 (DDR3) 3/5
03	--	CLOCK MAP	23	--	VGA_S3 (DP) 4/5
04	--	POWER MAP	24	--	VGA_S3 (POWER) 5/5
05	--	POWER SEQUENCY DIAGRAM	25	--	VRAM (DDR3)
06	--	POWER SEQUENCY TIMING	26	--	EC+KBC (IT8502E)
07	--	SMBUS MAP	27	--	CODEC/JACK/SPEAKER/MIC
08	--	RESET SIGNAL MAP	28	--	LAN (RTL8103EL)/CLOCK GEN
09	--	Calpella (DMI,PEG,FDI)	29	--	Card Reader
10	--	Calpella (CLK,MISC,JTAG)	30	--	WLAN/BT/MDC/USB/MOUNTING
11	--	Calpella (DDR3)	31	--	LVDS/CRT/Webcam
12	--	Calpella (POWER/GND)	32	--	HDMI
13	--	Calpella (GRAPHIC POWER)	33	--	DCIN/Battery/OCP/FAN
14	--	PCH (HDA,JTAG,SATA)	34	--	PWR_Charger MAX8731AETI
15	--	PCH (PCI-E,SMBUS,CLK)	35	--	5V/3.3V SN0608098RHB
16	--	PCH (DMI,FDI,GPIO,LVDS)	36	--	Vcore MAX17030
17	--	PCH (PCI,USB,NVRAM,GPIO)	37	--	1.1V VTT/+V1.05RUN
18	--	PCH (POWER)	38	--	1.5VDDR3+0.75V+V1.8RUN
19	--	DDR3(SO-DIMM_0&1)	39	--	PWR_Others power plane
20	--	VGA (PCI-E/STRAP) 1/5	40	--	CPU VREG & Decoupling
			41	--	ATVDD/+VPCIE

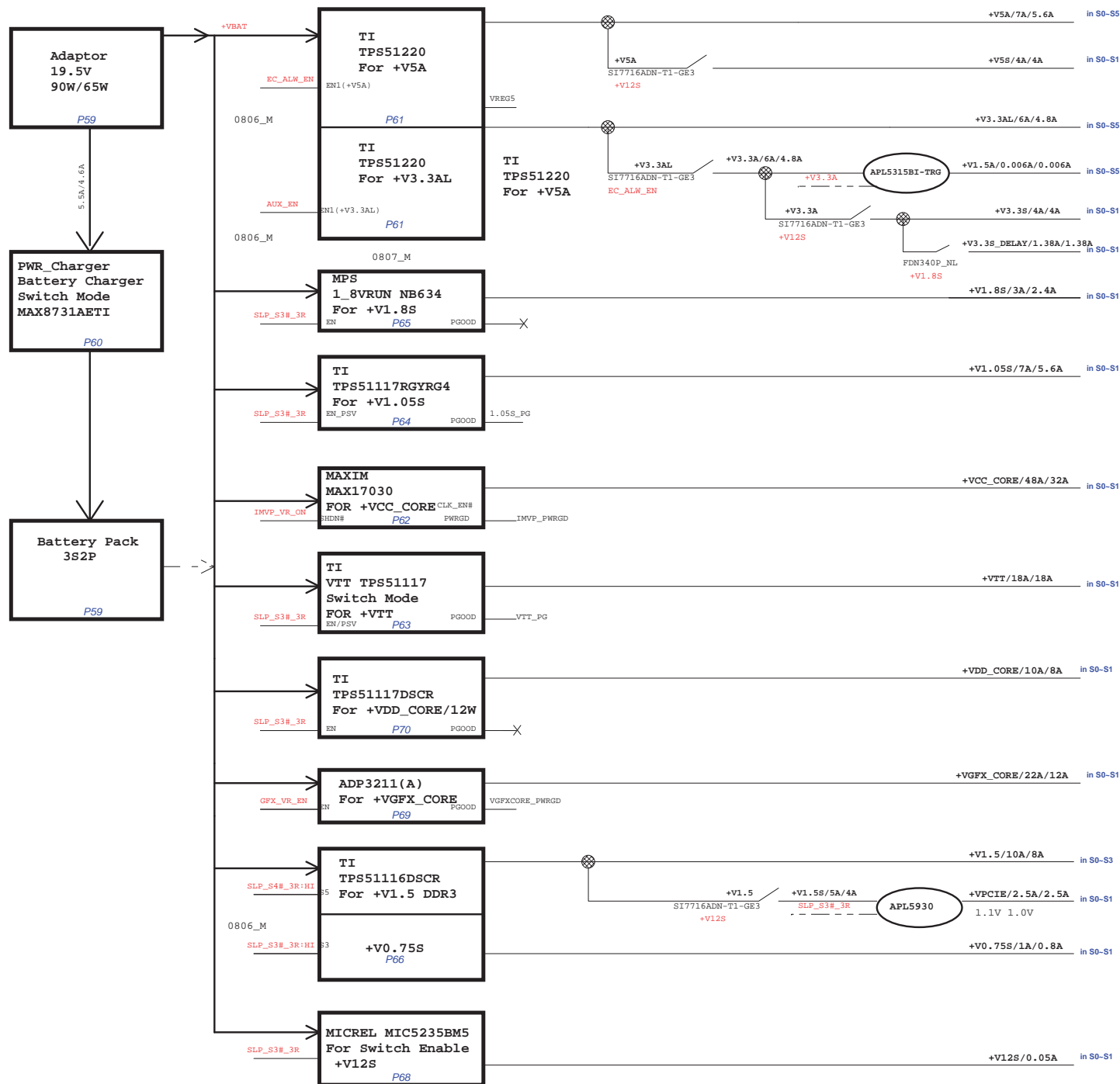
P. Leader	Check by	Design by

 Foxconn EMS Inc. HNBD R&D		Hon Hai Precision Industry Co. Ltd. phone: +886-2-2799-6111
Title		
Index Page		
Size	Document Number	Rev
Custom	STAR (Federer)	0.4
Page Modified: Tuesday, December 29, 2009 13:50:37 (UTC+GMT)		Sheet 1 of 41

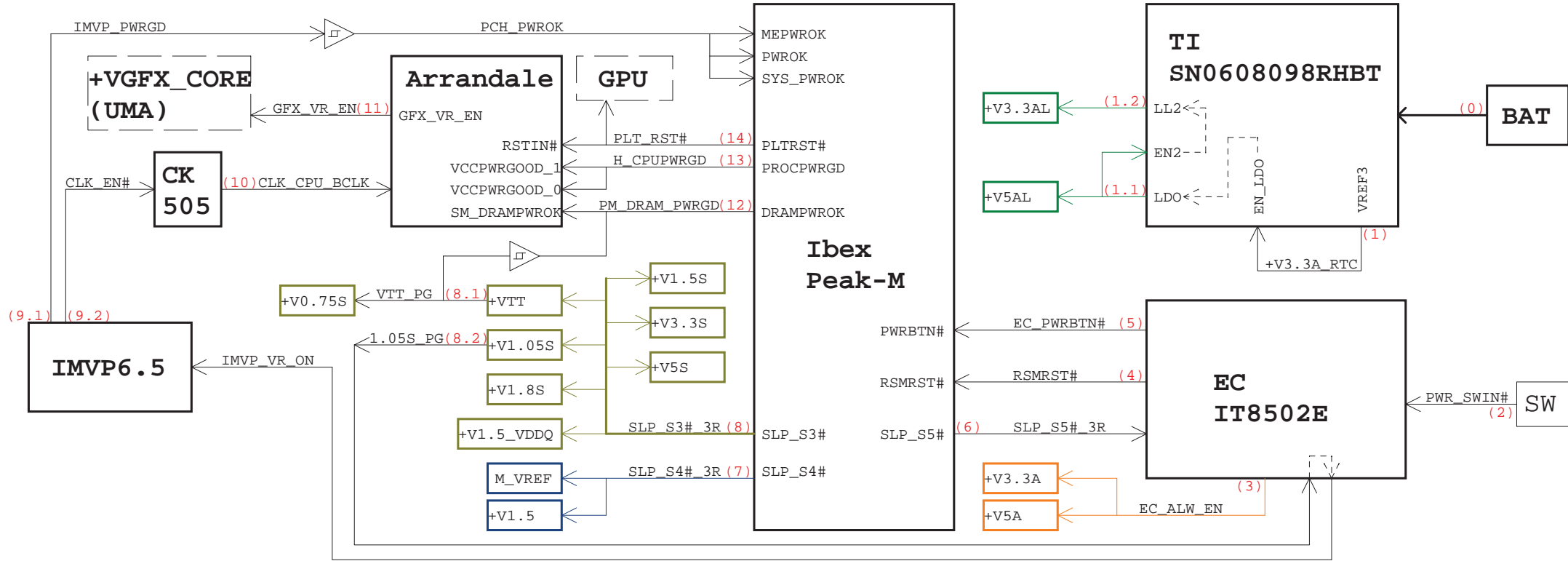




ADAPT_OC_IINP to IT8520
ACIN_EC to IT8520



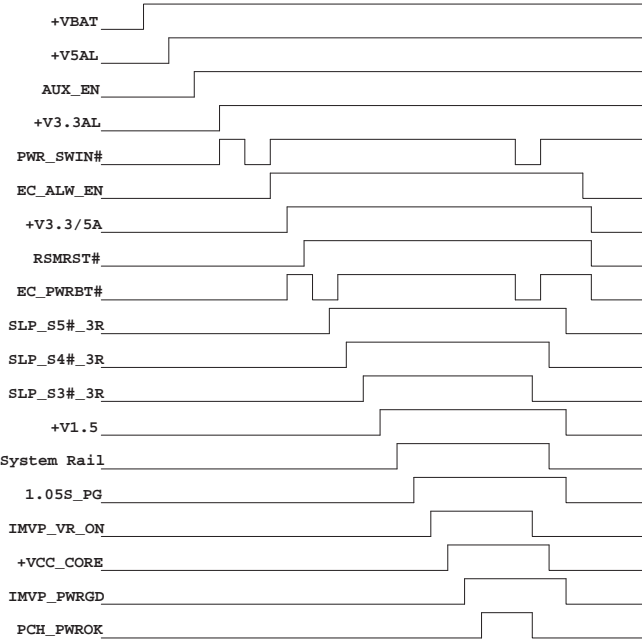
POWER SEQUENCY DIAGRAM



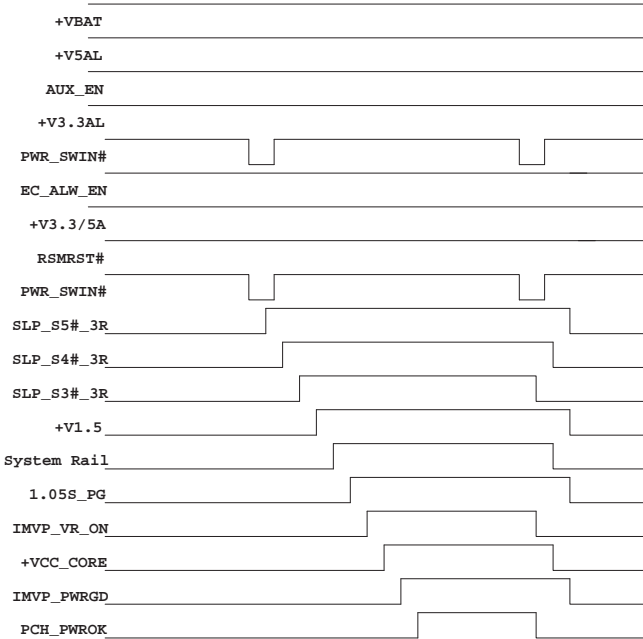
	Source Rail	EN	PG	Power Status				Remark
				S0	S3	AC S4/S5	DC S4/S5	
+VBAT				V	V	V	V	
+V5AL	+VBAT	+V3.3A_RTC		V	V	V	V	
+V3.3AL	+VBAT	+V5AL		V	V	V	V	
+V5A	+VBAT	EC_ALW_EN		V	V	V		
+V3.3A	+V3.3AL	EC_ALW_EN		V	V	V		
+V1.5	+VBAT	SLP_S4#_3R		V	V			
+V0.75S	+V1.5	VTT_PG		V				
+V1.5S	+V1.5	RUN_ON_LOAD		V				
+V1.5_VDDQ	+V1.5	RUN_ON_LOAD		V				
+VCC_CORE	+VBAT	IMVP_VR_ON	IMVP_PWRGD	V				
+VTT	+VBAT	SLP_S3#_3R	VTT_PG	V				
+VGFX_CORE	+VBAT	GFX_VR_EN		V				
+V1.8S	+VBAT	SLP_S3#_3R		V				
+V1.05S	+VBAT	SLP_S3#_3R	1.05S_PG	V				
+V5S	+V5A	RUN_ON_LOAD		V				
+V3.3S	+V3.3A	RUN_ON_LOAD		V				
+VDD_CORE	+VBAT	SLP_S3#_3R		V				
+V3.3S_Delay	+V3.3S	+V1.8S		V				
+VPCIE	+V1.5S	SLP_S3#_3R		V				

POWER SEQUENCE TIMING

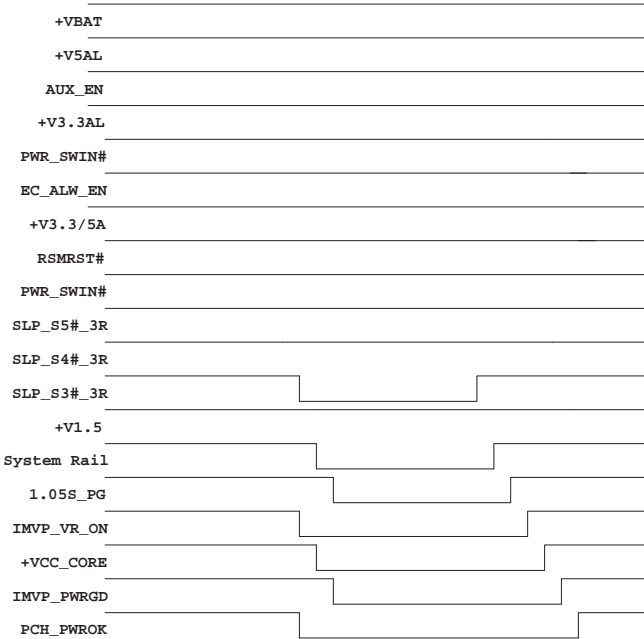
G3(OFF)->S0->S5



S5->S0->S5



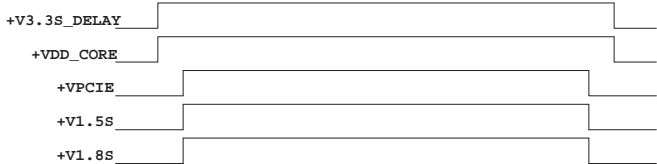
S0->S3->S0



M93 Sequence



Park Sequence



SMBUS&I2C MAP

Discrete
GPU

GPU
M93/Park
S3 Package

PCH

EC
ITE8502

DIMM0

DIMM1

CLOCK
GEN


WLAN

Temp
Sensor

Charger

Battery

RESET SIGNAL MAP



Hon Hai Precision Industry Co. Ltd.

Foxconn eMS Inc.

HNBD R&D

phone: +886-2-2799-6111

Title

RESET SIGNAL MAP

Size

Document Number

Rev

Custom

STAR (Federer)

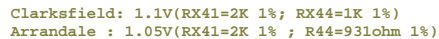
0.4

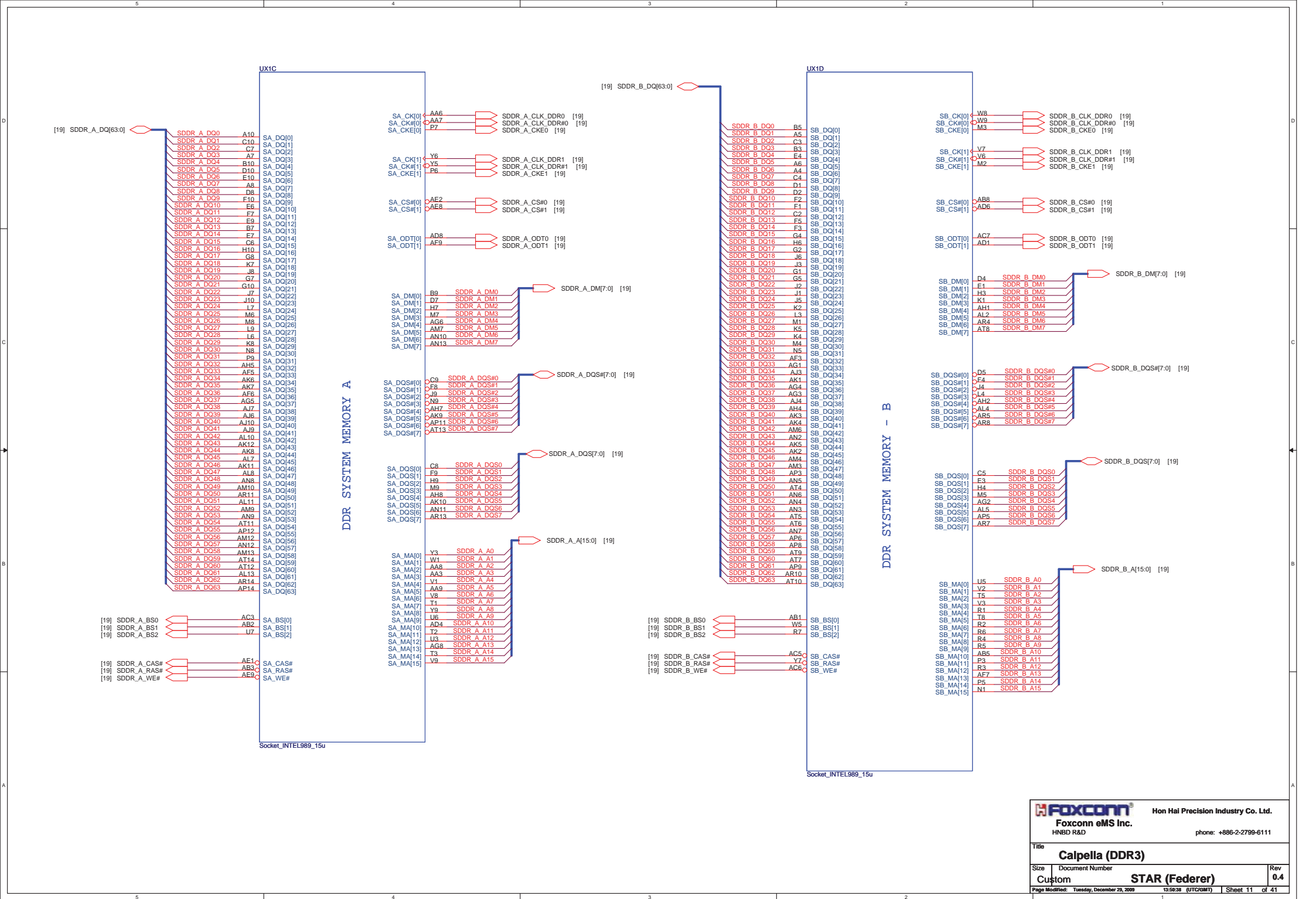
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13:59:41 (UTC/GMT)

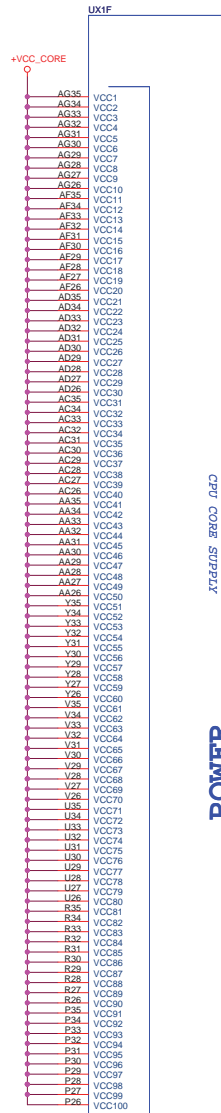
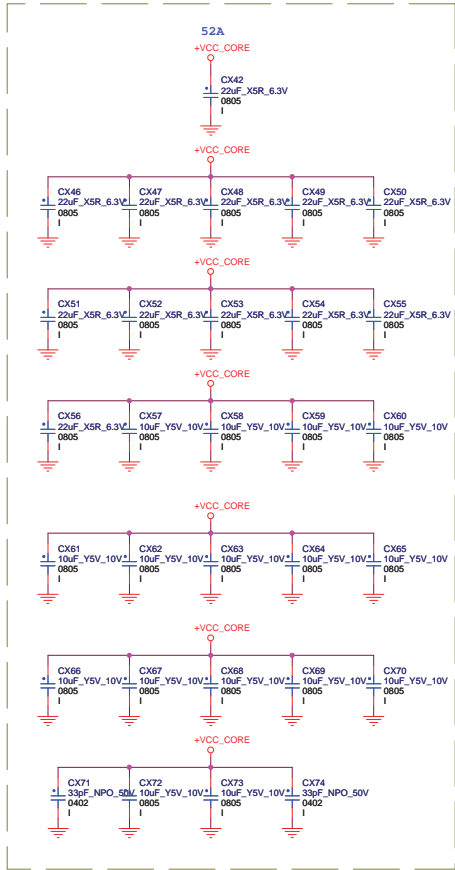
Sheet 8 of 41

Place close to chip

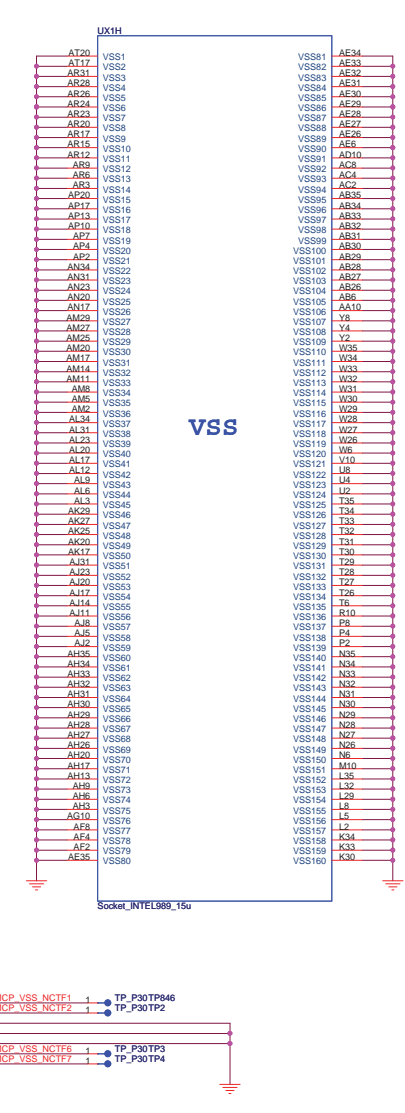
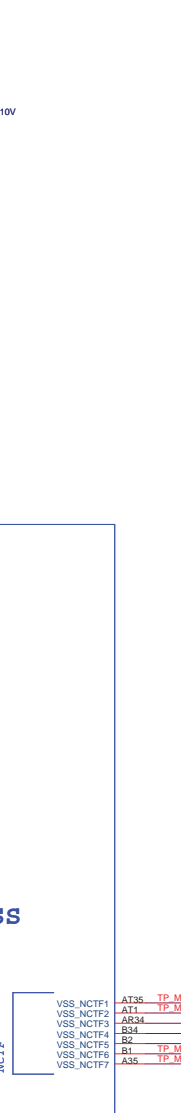
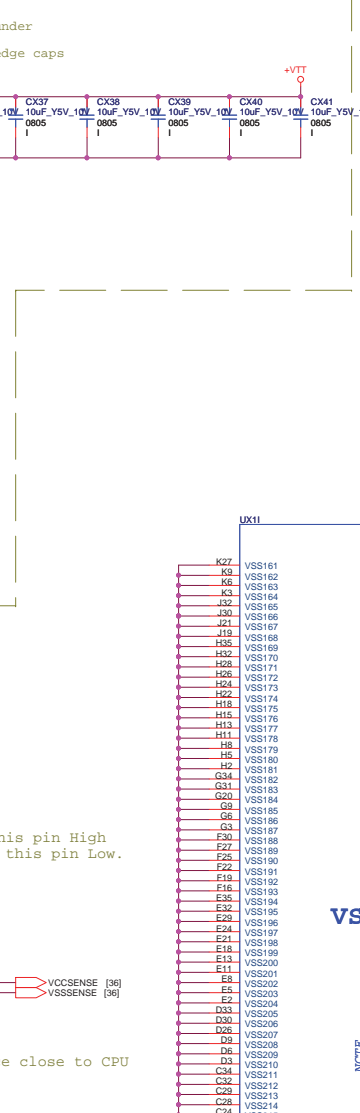
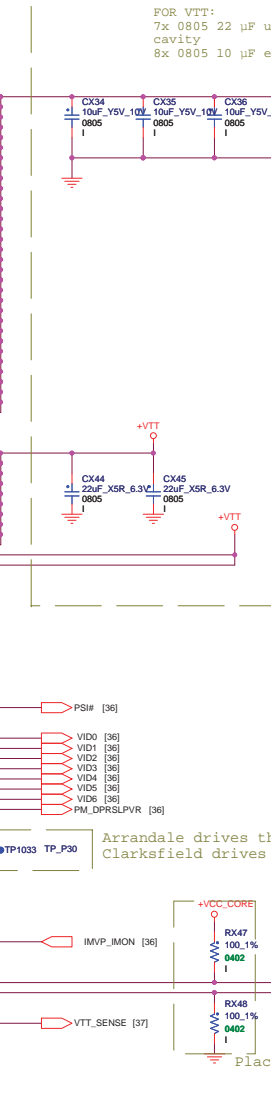
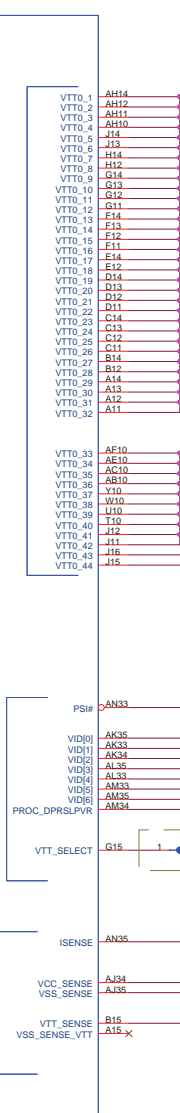


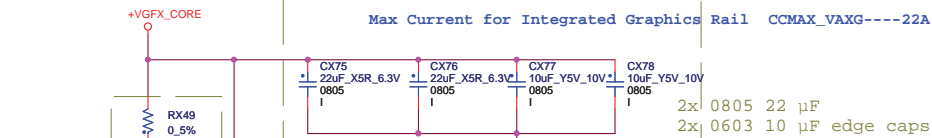


FOR VCC:
12x 0805 22 μ F inside cavity,
7x 0805 10 μ F under cavity and 9 x 0805 10 μ F
between inductor and socket on top layer



1.1V RAIL POWER
CPU CORE STRIPLEX
POWER
CPU VIDS
SENSE





Discrete GPU: Install
UMA: Not Install

Discrete GPU: Not Install
UMA: Install

UX1G

AT21	VAXG1
AT19	VAXG2
AT18	VAXG3
AT16	VAXG4
AR21	VAXG5
AR19	VAXG6
AR18	VAXG7
AR16	VAXG8
AP21	VAXG9
AP19	VAXG10
AP18	VAXG11
AP16	VAXG12
AN21	VAXG13
AN19	VAXG14
AN18	VAXG15
AN16	VAXG16
AM21	VAXG17
AM19	VAXG18
AM18	VAXG19
AM16	VAXG20
AL21	VAXG21
AL19	VAXG22
AL18	VAXG23
AK21	VAXG24
AK19	VAXG25
AK18	VAXG26
AK16	VAXG27
AJ21	VAXG28
AJ19	VAXG29
AJ18	VAXG30
AJ16	VAXG31
AH21	VAXG32
AH19	VAXG33
AH18	VAXG34
AH16	VAXG35
	VAXG36

GRAPHICS

POWER

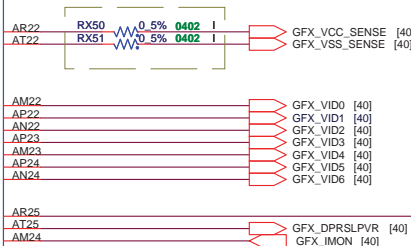
FDI

PBG & IMT

Socket_INTEL989_15u

+VTTQ [10,12,17,18,28,36,37,40]
+V GFX_CORE [40]
+V1.5_VDDQ [10,18,28,30,39]
+V1.8SQ [18,38,39]

Discrete GPU: Not Install
UMA: Install



Discrete GPU: Install
UMA: Not Install



Discrete GPU: Not Install
UMA: Install

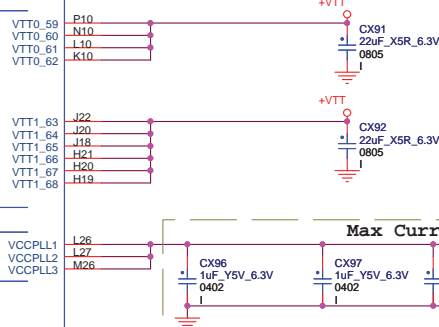


FOR_DDR3:
5x 0402 1 uF
2x 0805 22 uF

DDR3 - 1.5V RAILS

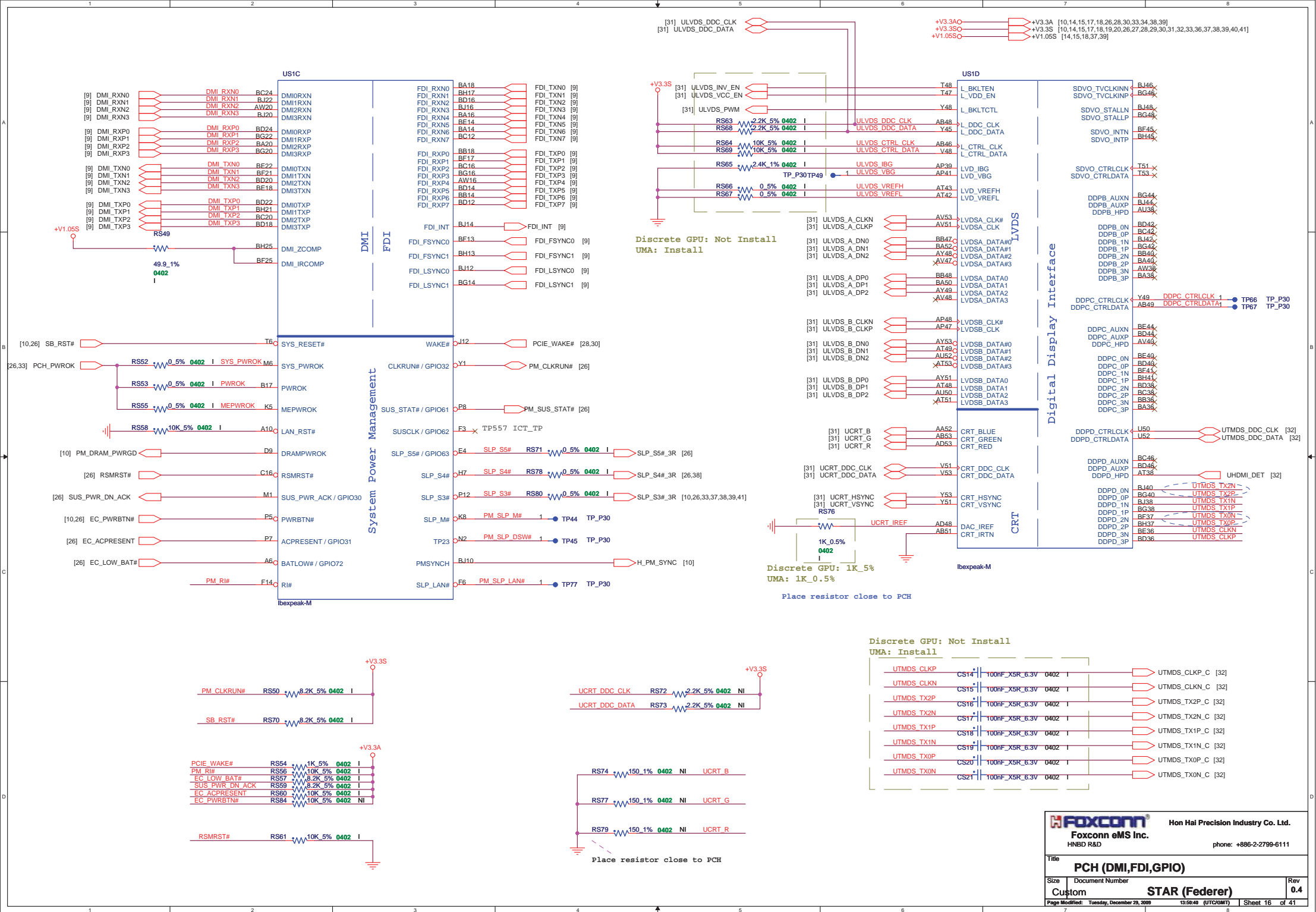
1.1V

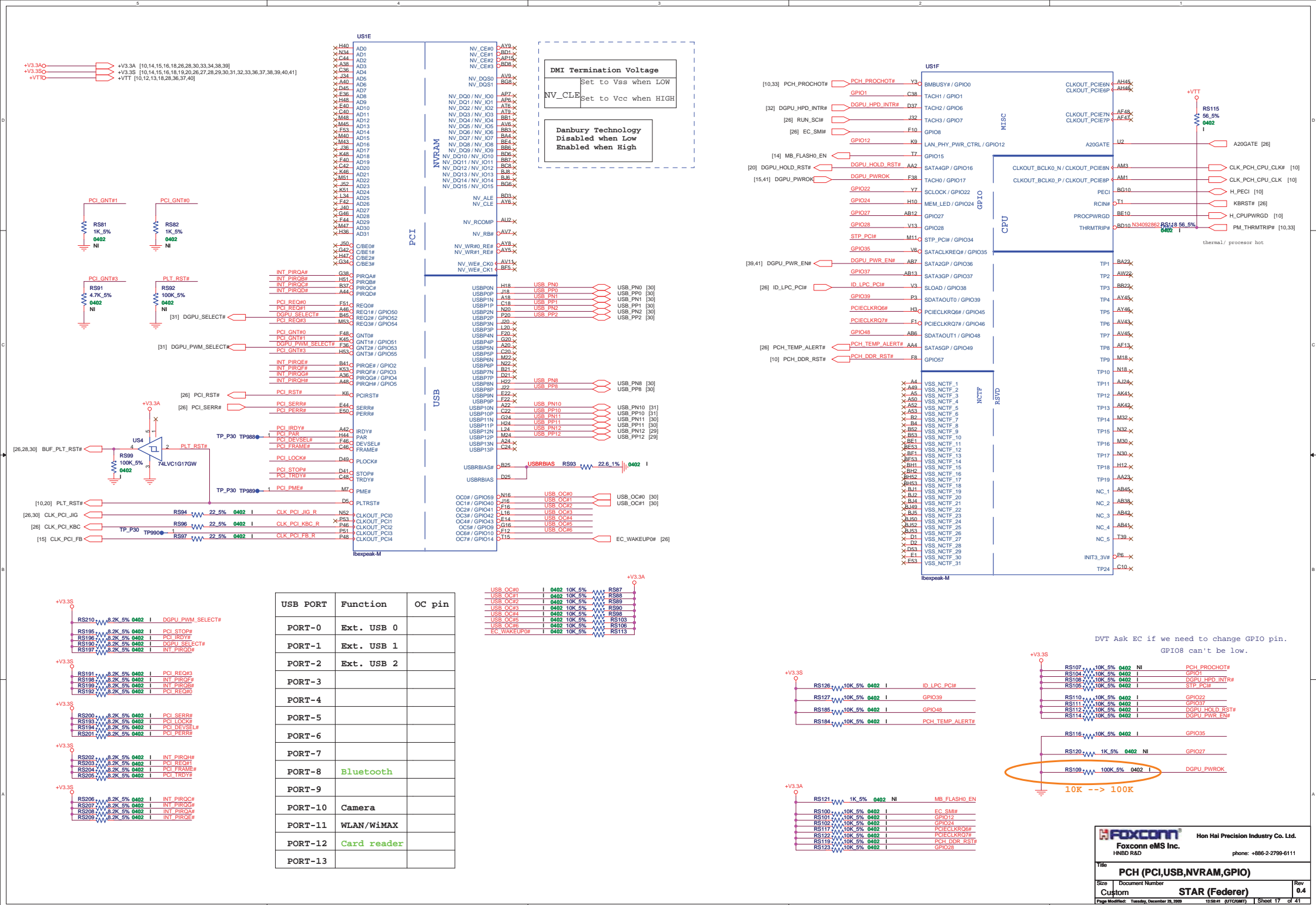
1.8V

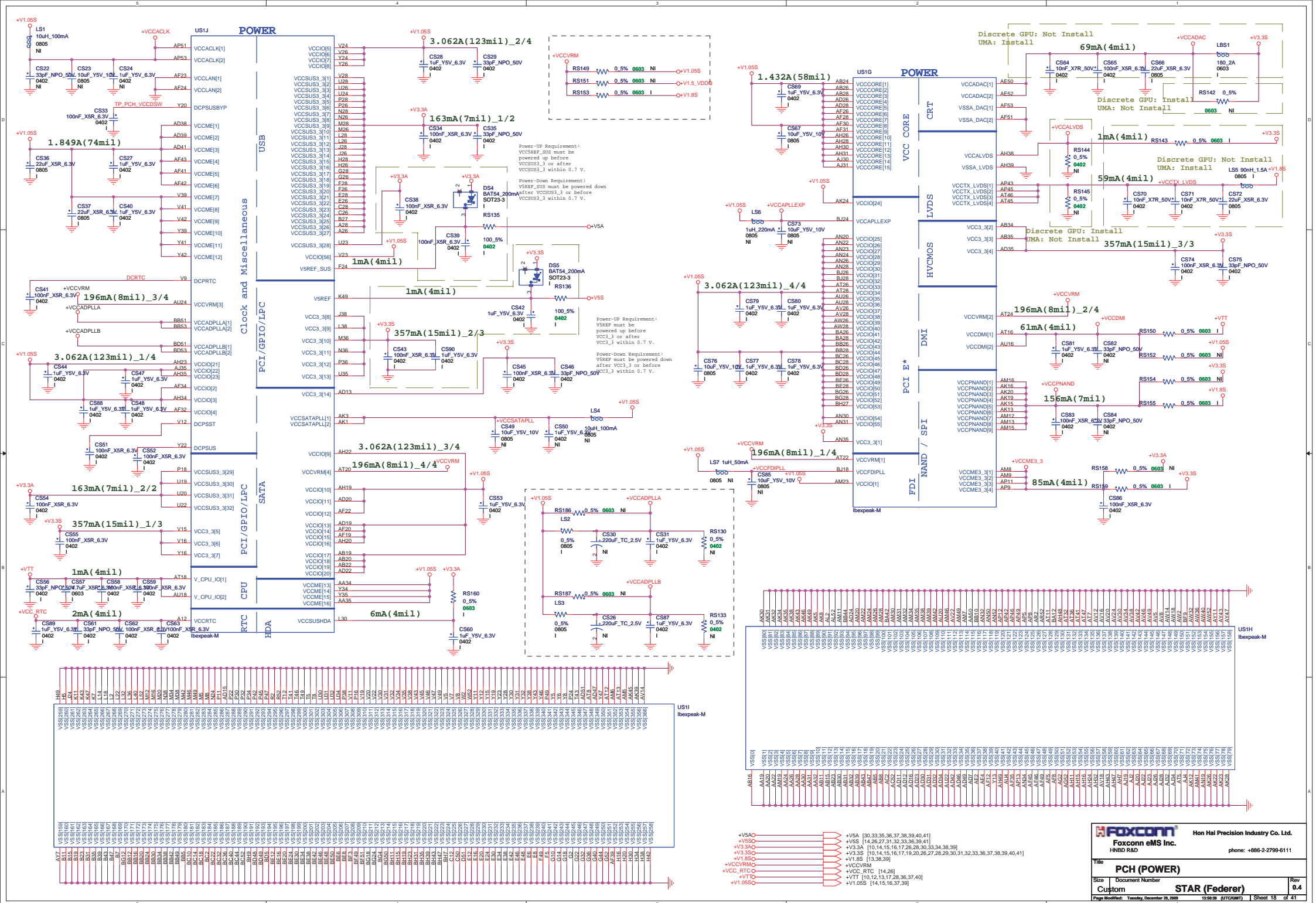


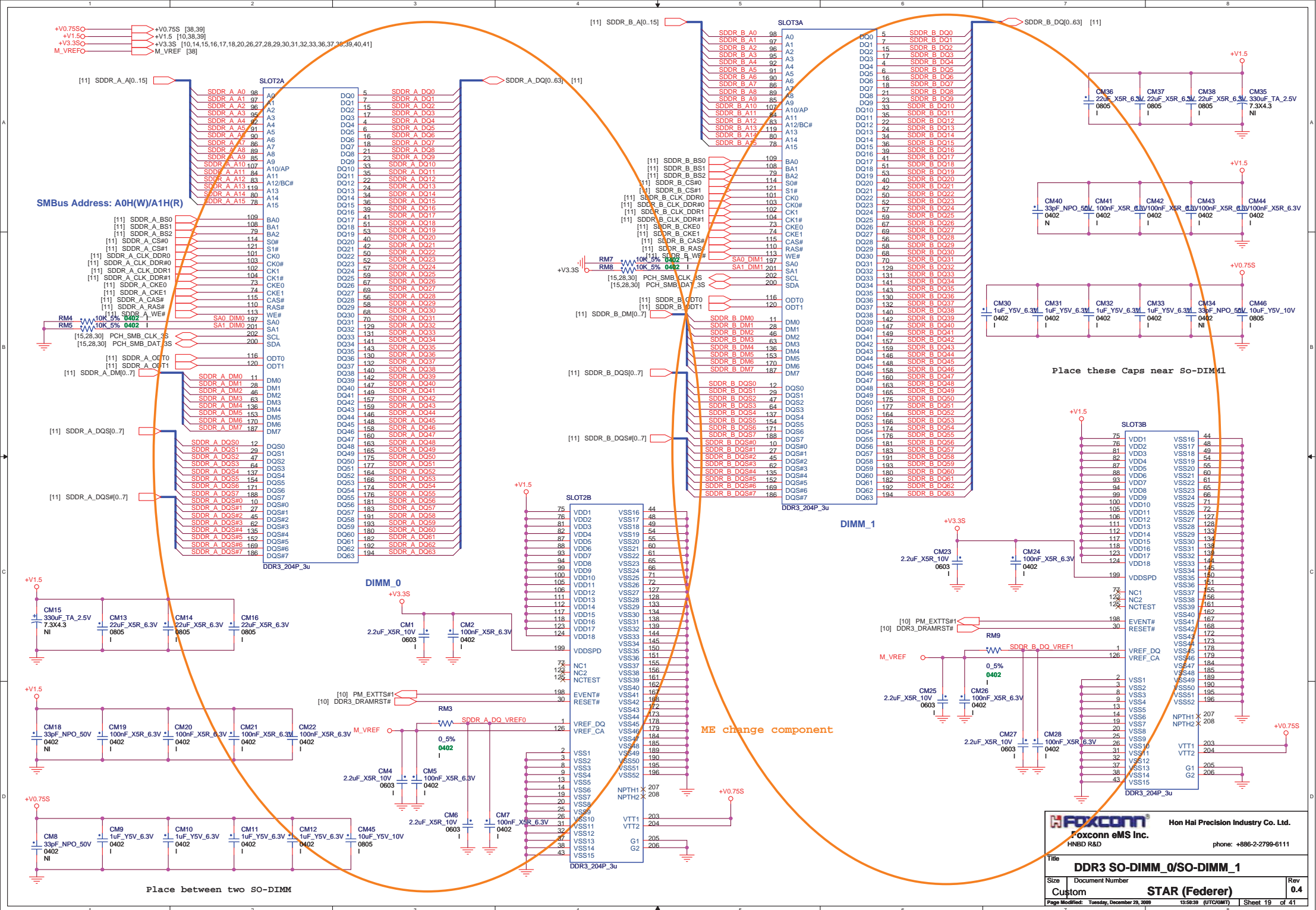
FOR_VTT:
1x 0805 2.2 uF
2x 0805 1 uF
1x 0805 22 uF
1x 0603 4.7 uF

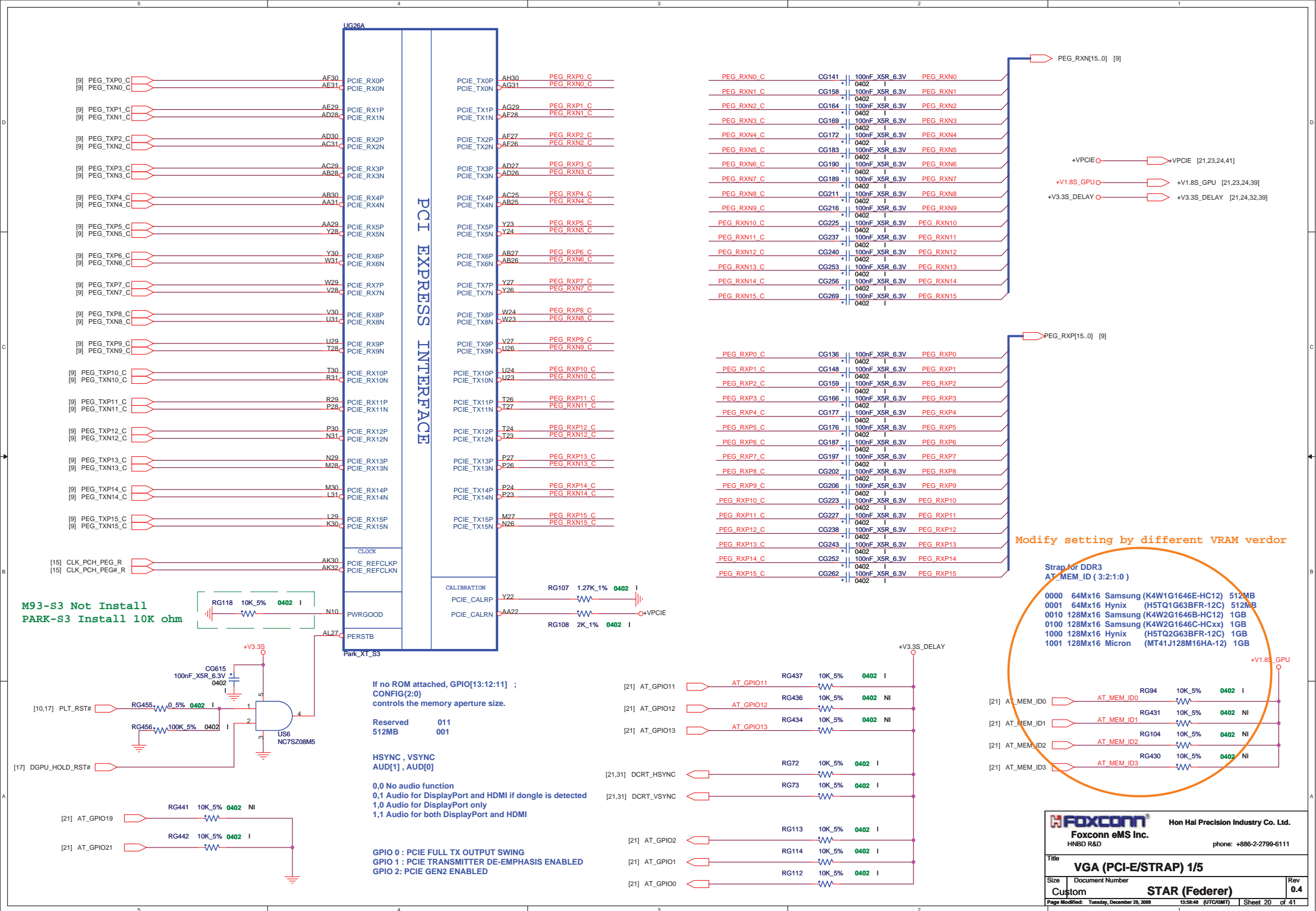
Max Current for VCCPLL Rail 1.35A







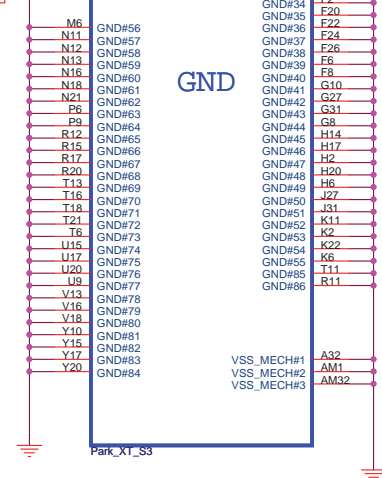
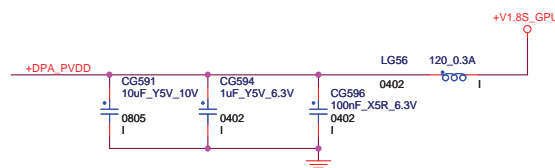
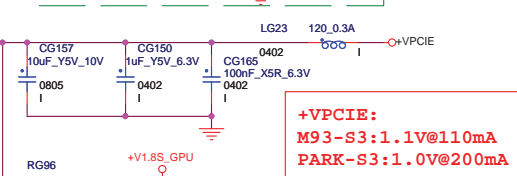
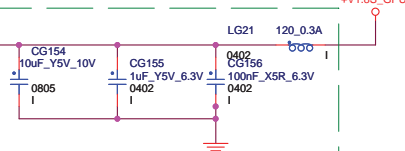
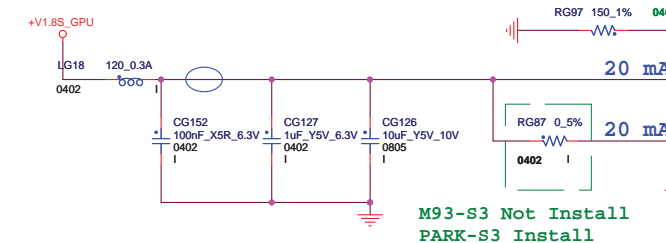
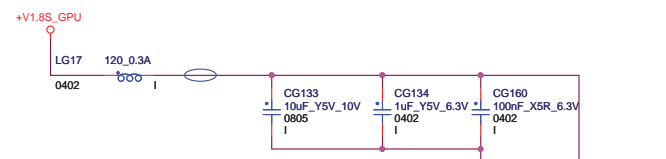


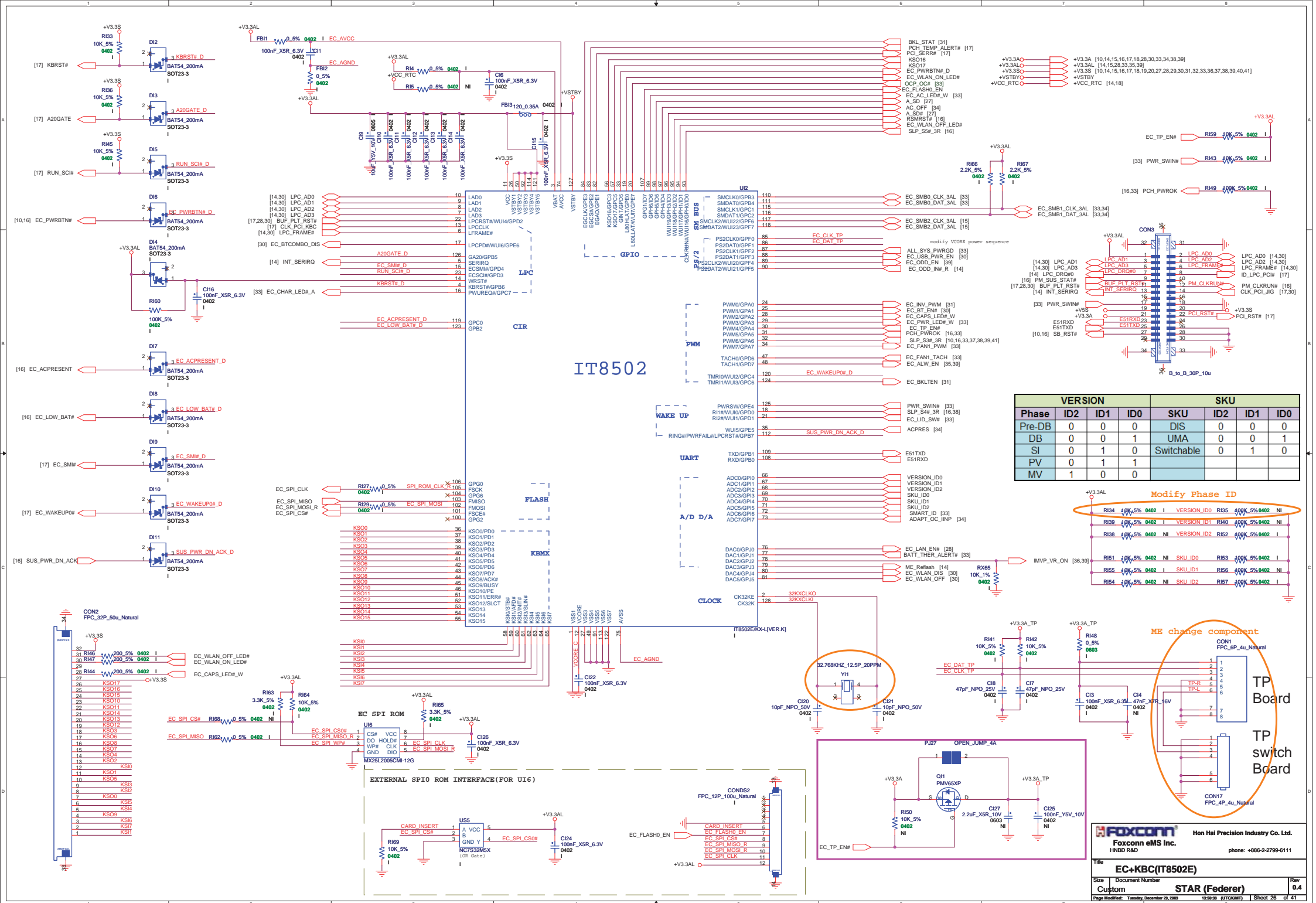


M93-S3:Not Install
PARK-S3:Install

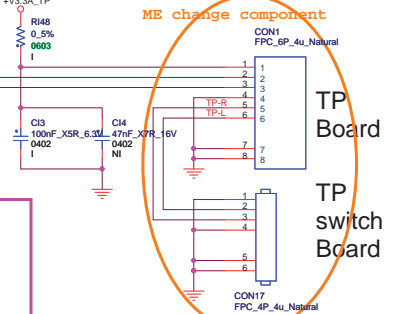
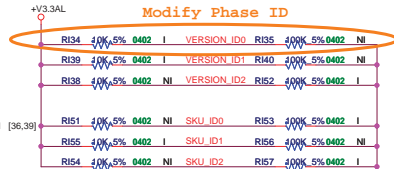
Del NorFlash parts

clock source change to clock gen.



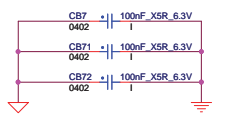
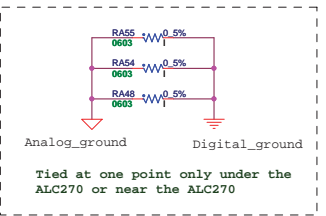
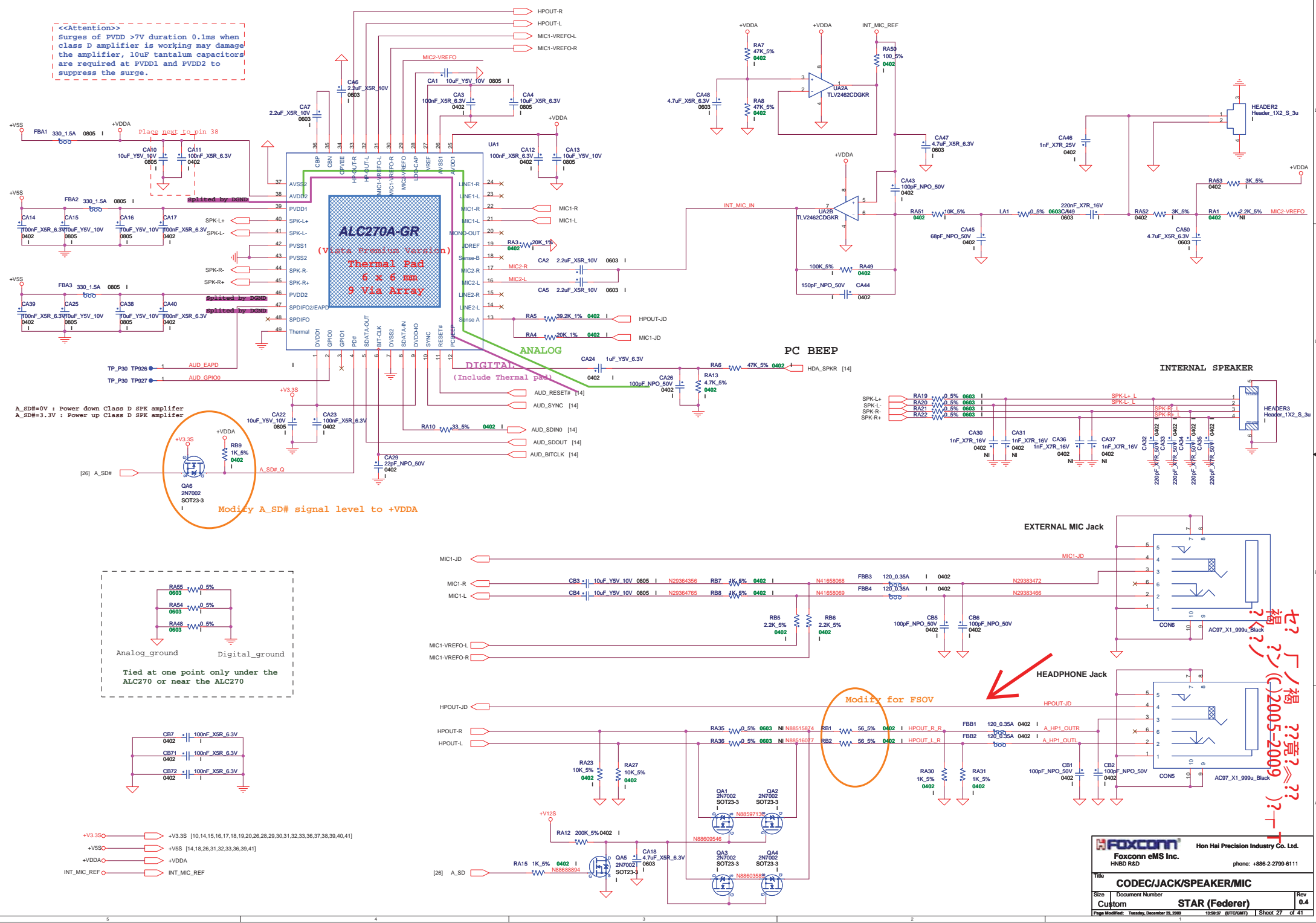


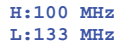
VERSION				SKU			
Phase	ID2	ID1	ID0	SKU	ID2	ID1	ID0
Pre-DB	0	0	0	DIS	0	0	0
DB	0	0	1	UMA	0	0	1
PI	0	1	0	Switchable	0	1	0
SV	0	1	1				
MV	1	0	0				



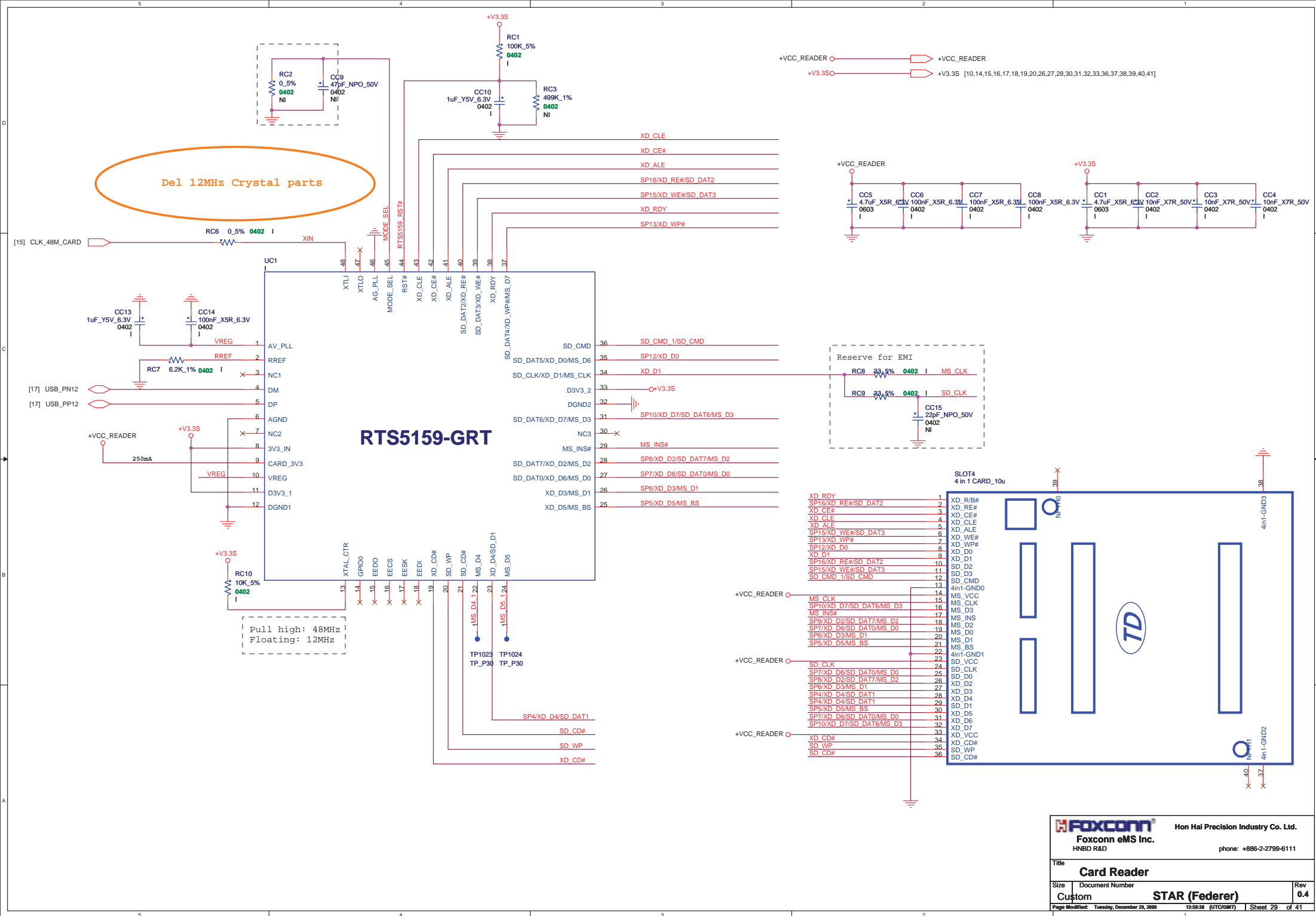
FOXCONN Hon Hai Precision Industry Co. Ltd.
Foxconn eMS Inc.
HNB D R&D phone: +886-2-2799-6111

<<Attention>>
Surges of PVDD >7V duration 0.1ms when class D amplifier is working may damage the amplifier, 10uF tantalum capacitors are required at PVDD1 and PVDD2 to suppress the surge.

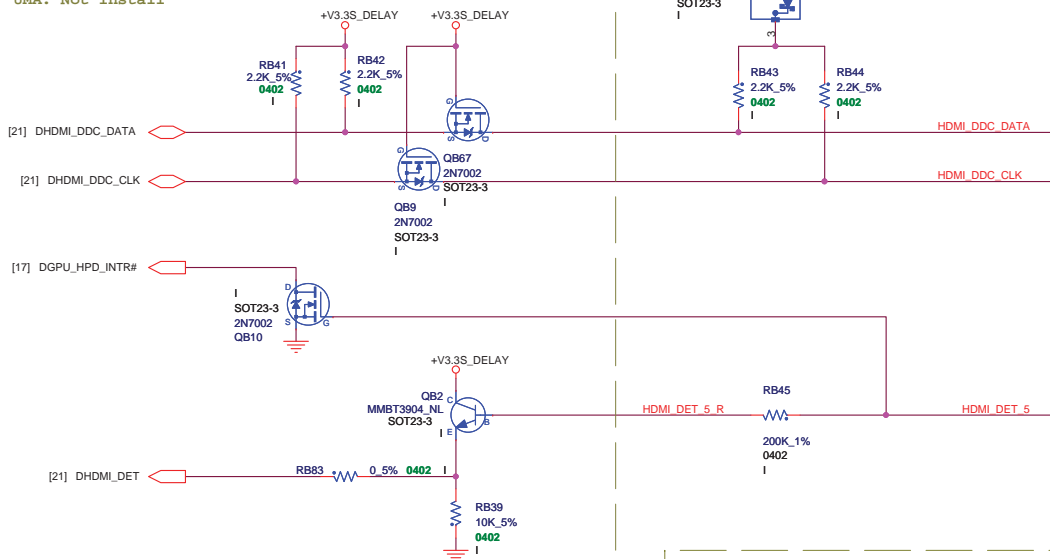




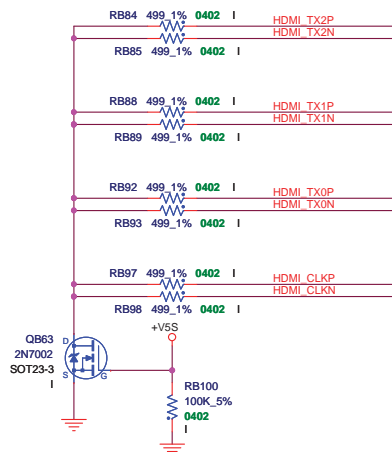
FS	CPU (PCH-->CPU)	Power On	SRC(DMI) (PCH-->CPU)	SATA (PCH)	DOT96 (PCH)	27MHz (GPU)	REF
0	133MHz	Default	100MHz	100MHz	96MHz	27MHz	14.318MHz
1	100MHz						



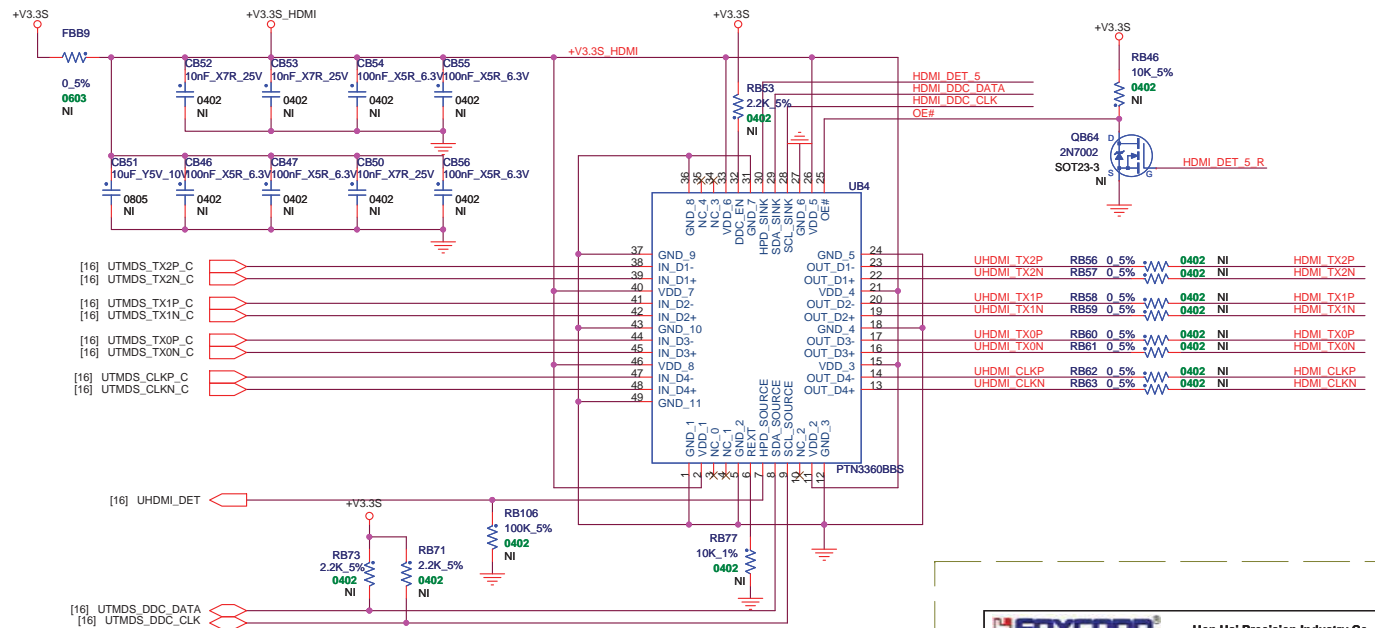
Discrete GPU: Install
UMA: Not Install



[21] DHDHMI_TX2P	CB63 0402	100nF X5R 6.3V	I	HDMI TX2P
[21] DHDHMI_TX2N	CB64 0402	100nF X5R 6.3V	I	HDMI TX2N
[21] DHDHMI_TX1P	CB65 0402	100nF X5R 6.3V	I	HDMI TX1P
[21] DHDHMI_TX1N	CB66 0402	100nF X5R 6.3V	I	HDMI TX1N
[21] DHDHMI_TX0P	CB67 0402	100nF X5R 6.3V	I	HDMI TX0P
[21] DHDHMI_TX0N	CB68 0402	100nF X5R 6.3V	I	HDMI TX0N
[21] DHDHMI_CLKP	CB69 0402	100nF X5R 6.3V	I	HDMI CLKP
[21] DHDHMI_CLKN	CB70 0402	100nF X5R 6.3V	I	HDMI CLKN



Discrete GPU:Not Install
UMA:Install



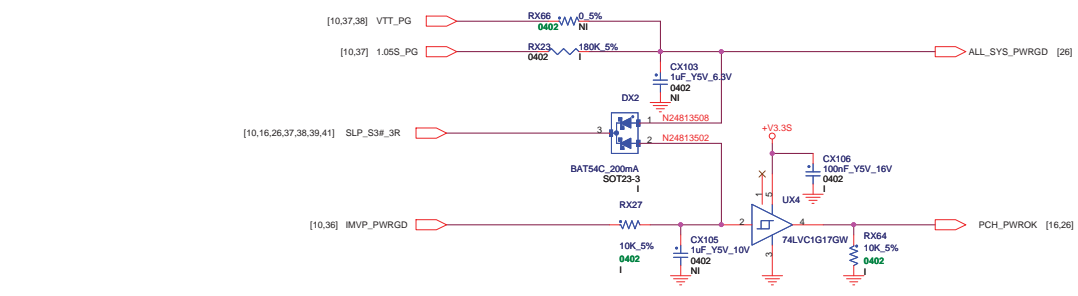
10uF --> 22uF +VSS Modify FAN control circuit



DC_JACK BT+ O DCIN O +V3.3AL O +V3.3AO +V3.3SO M31ALDOO

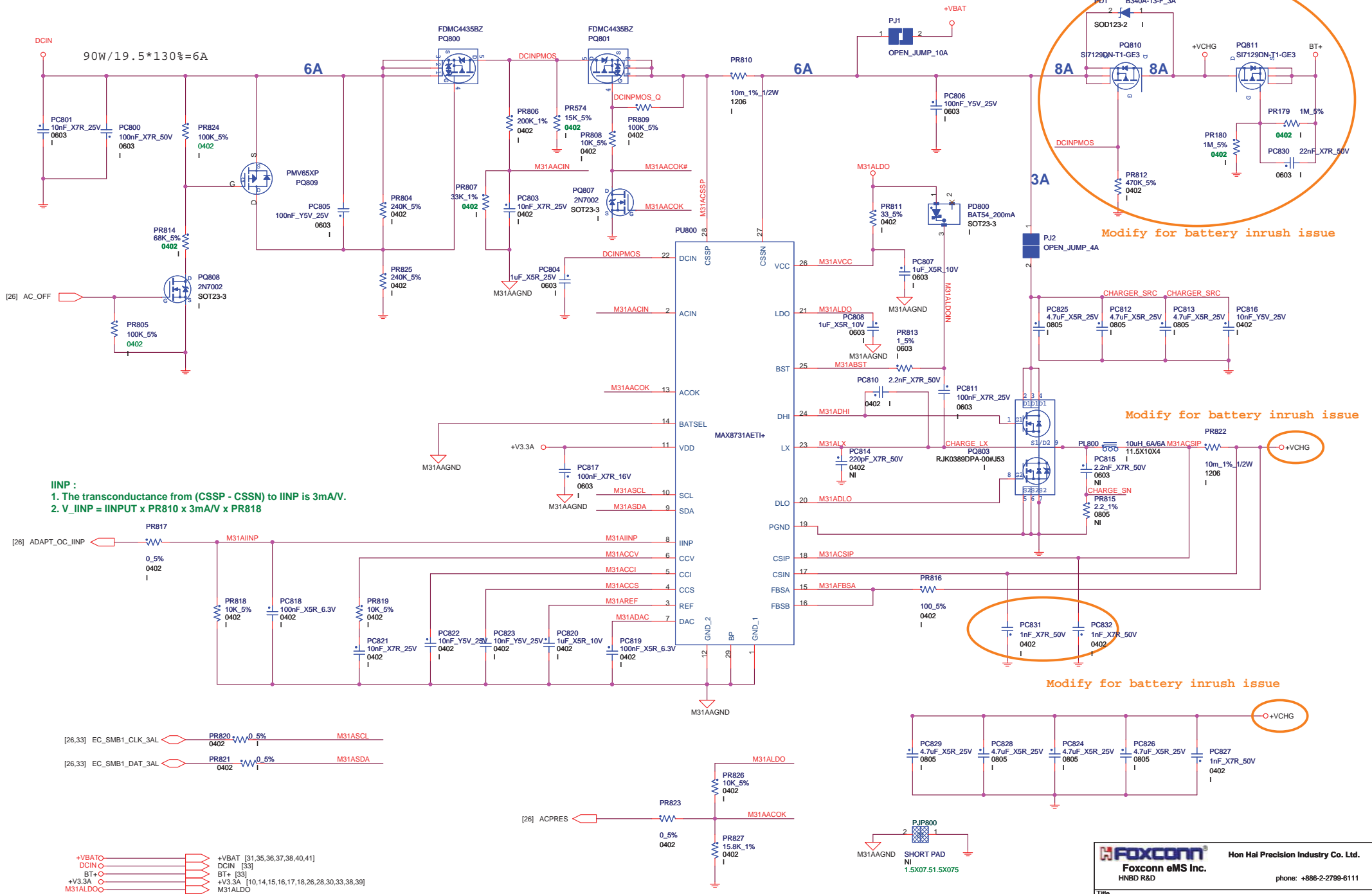
Wire to Board

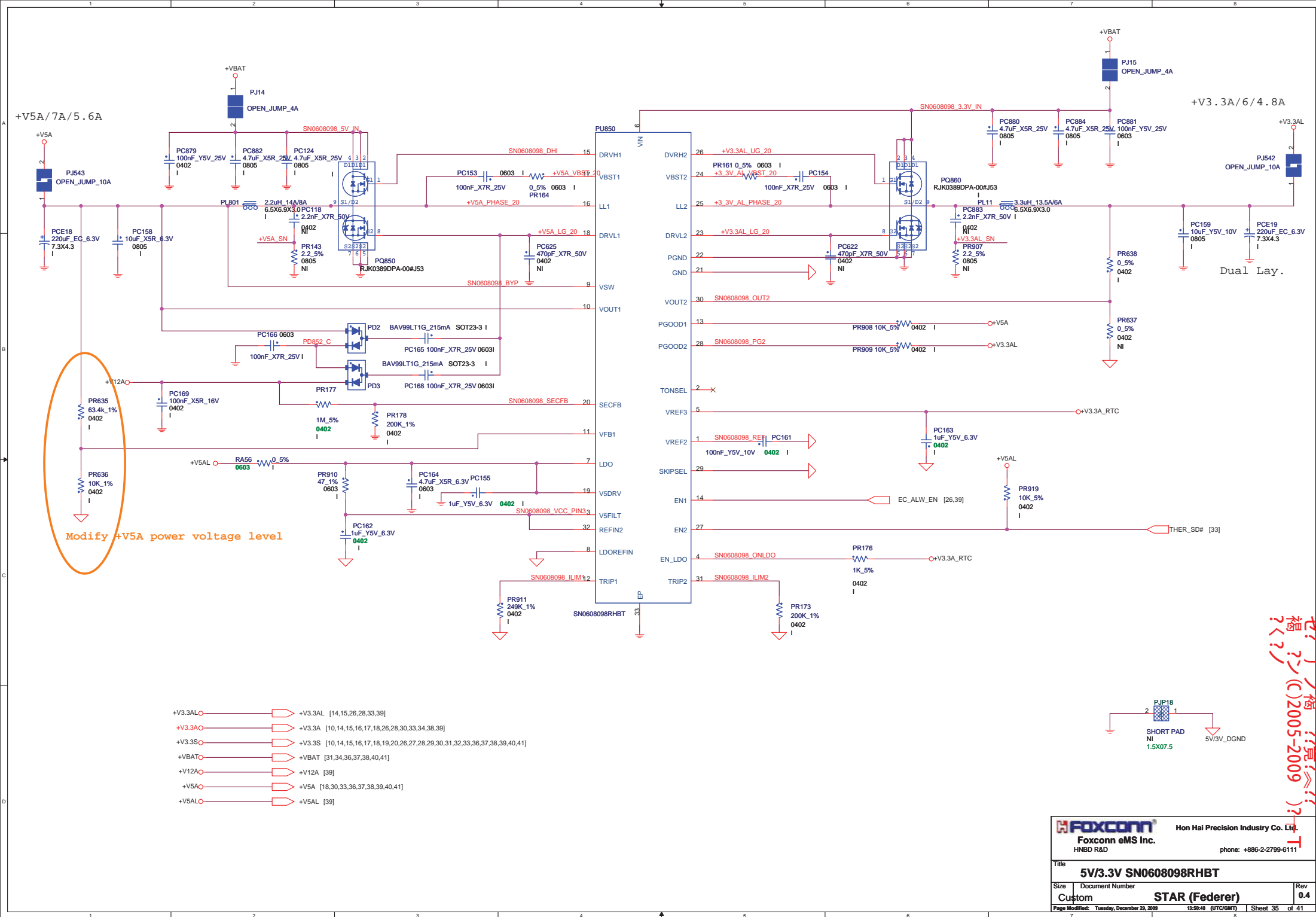
BT+ [34] DCIN [34] +V3.3AL [14,15,16,17,18,20,26,28,35,39] +V3.3AO [10,14,15,16,17,18,20,26,30,34,38,39] +V3.3SO [10,14,15,16,17,18,19,20,26,27,28,29,30,31,32,36,37,38,39,40,41] M31ALDO [34]



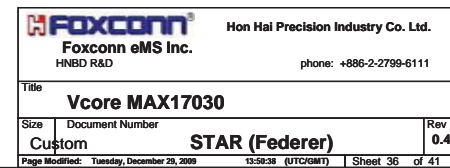
		S7S SMD Threshold Temperature					
		4.7K OHM 210%	6.8K OHM 210%	10K OHM 210%	15K OHM 210%	22K OHM 210%	33K OHM 210%
4.7K OHM 210%	Pick-Up	77°C	83°C	89°C	95°C	101°C	107°C
6.8K OHM 210%		79°C	84°C	90°C	96°C	102°C	108°C
10K OHM 210%		79°C	85°C	91°C	97°C	103°C	109°C
15K OHM 210%		80°C	86°C	92°C	98°C	104°C	110°C
22K OHM 210%		81°C	87°C	93°C	99°C	105°C	111°C
33K OHM 210%		82°C	88°C	94°C	100°C	106°C	112°C

Pin No.	Symbol	Comments
1	BATT+	Batt+, Battery Positive Terminal
2	BATT+	Batt+, Battery Positive Terminal
3	SMD	SMBus data interface I/O pin.
4	SMC	SMBus clock interface I/O pin
5	ID	Open
6	B/I	Connect to thermistor (103AT2 equivalent)
7	GND	Batt-, Battery Negative Terminal
8	GND	Batt-, Battery Negative Terminal

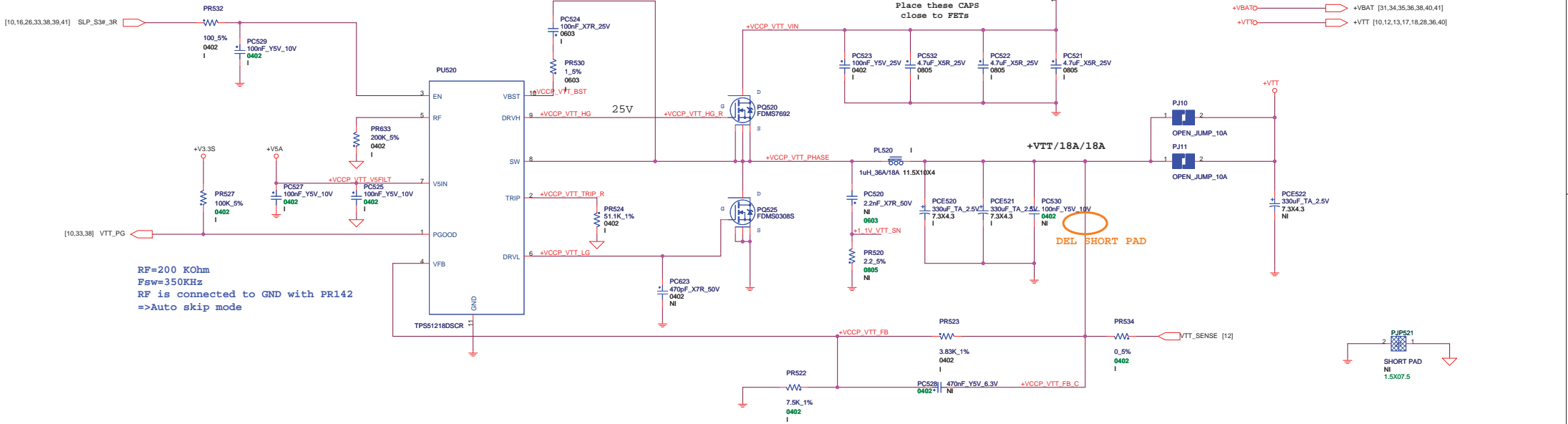




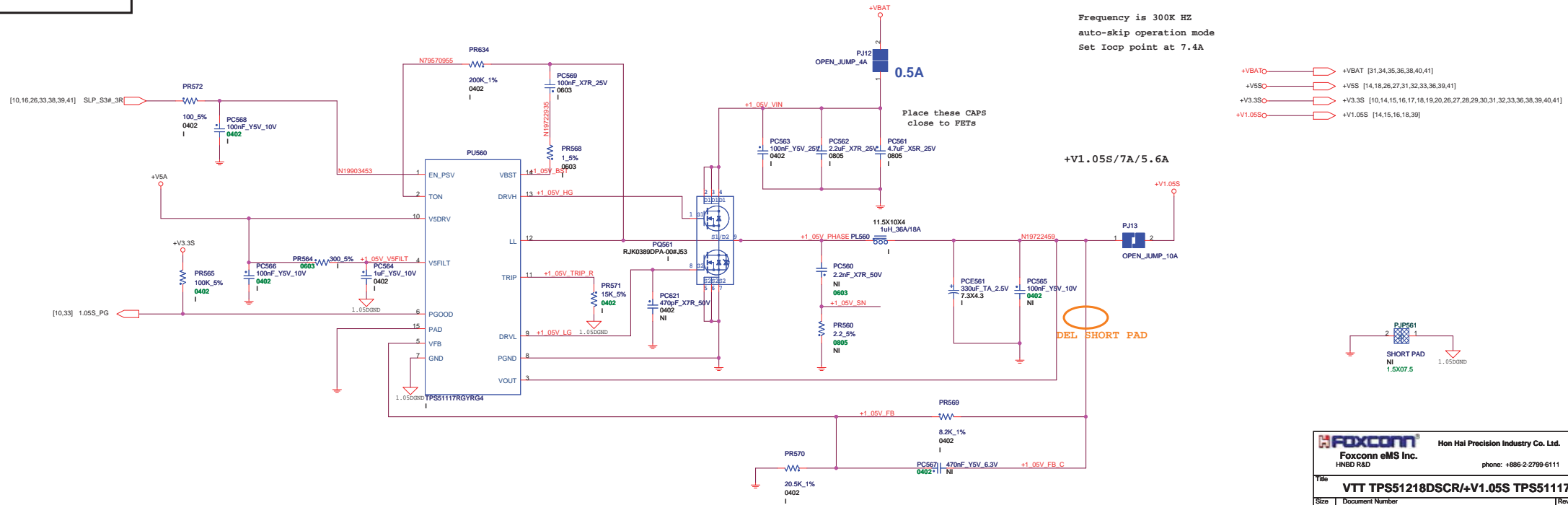
工厂
福 (C)2005-2009
?

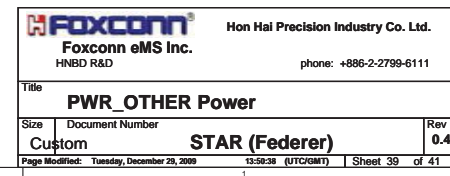


+VTT TPS51218

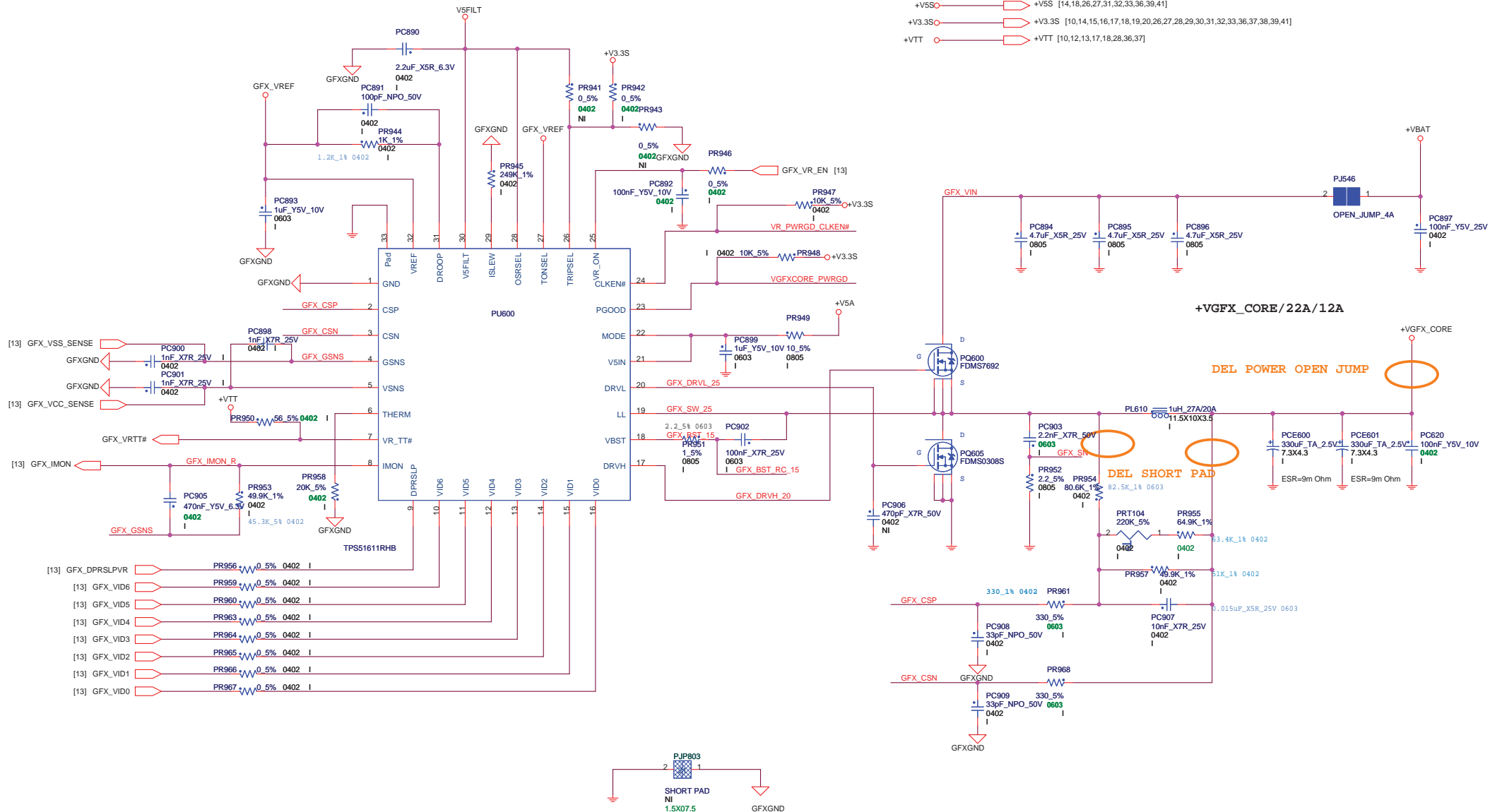


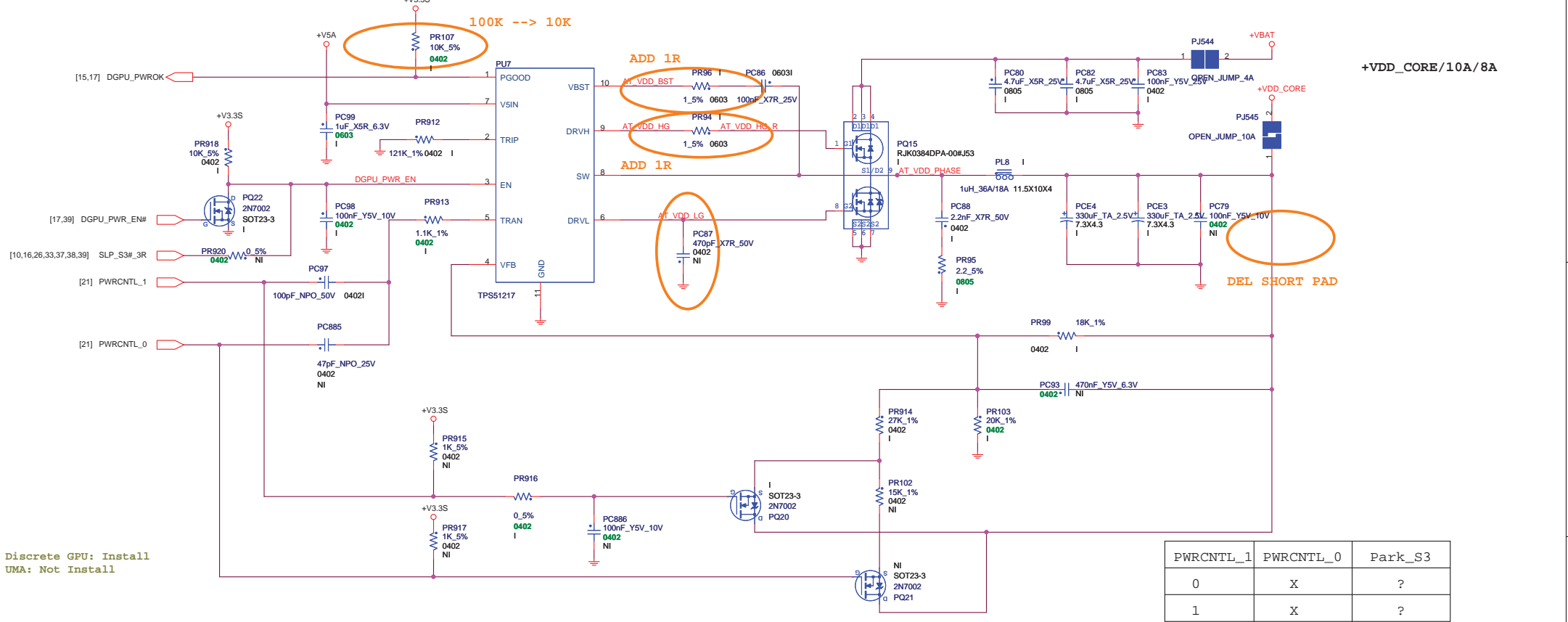
+V1.05S TPS51117



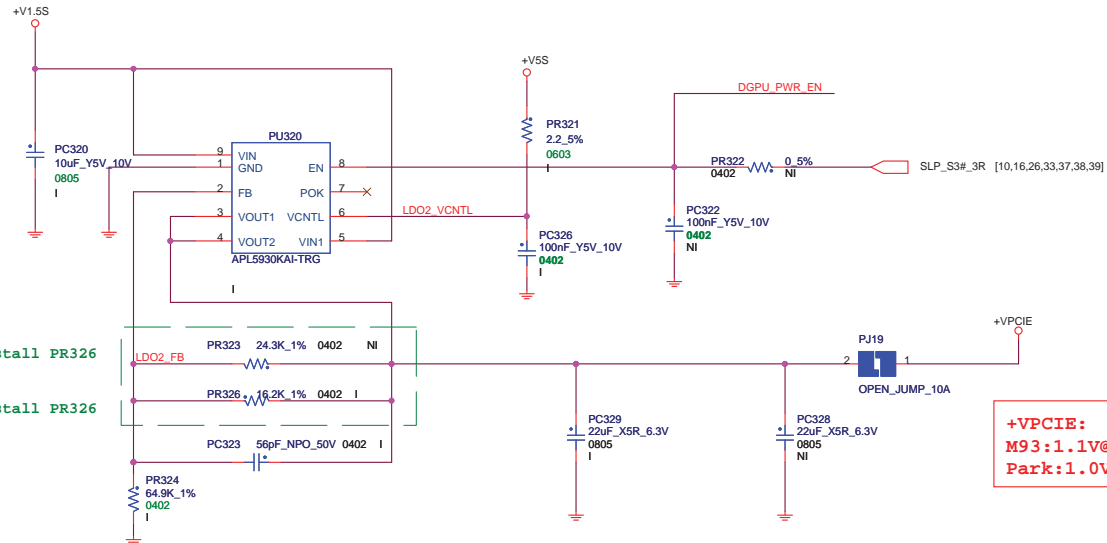


+VGFXCORE





Discrete GPU: Install
UMA: Not Install



- +VBAT → +VBAT [31,34,35,36,37,38,40]
- +V5A → +V5A [18,30,33,35,36,37,38,39,40]
- +V5S → +V5S [14,18,26,27,31,32,33,36,39]
- +V3.3S → +V3.3S [10,14,15,16,17,18,19,20,26,27,28,29,30,31,32,33,36,37,38,39,40]
- +V1.5S → +V1.5S [22,24,25,39]
- +VDD_CORE → +VDD_CORE [24]
- +VPCIE → +VPCIE [20,21,23,24]