

1	CPU P4-775(FSB)
2	CPU P4-775(PWR, GND)
3	Clock Generator
4	Power (CPU Vcore)
5	Power (DC to DC)
6	VDIMM & DDR VTT
7	NB P4M800pro (CPU)
8	NB P4M800pro (MEM)
9	NB P4M800pro (AGP, V-Link)
10	NB P4M800pro (VGA)
11	DDR II SLOT1
12	DDR II SLOT2
13	DDR I
14	DDR Terminator
15	AGP SLOT
16	SB 8237(PCI, USB)
17	SB 8237(IDE, GPIO, AC-Link)
18	SB 8237(V-Link, MII)
19	LAN PHY(VT6103L)
20	Super IO(ITE8705F GX)
21	PCI 1, 2
22	PCI 3
23	PCI LAN(RTL8100C)
24	USB, PS2, IDE
25	COM, LPT, VGA
26	Front Panel
27	AUDIO(ALC655), 6CH mute function
28	Cover Page
29	Block Diagram

# P4M800PRO-M

Rev : 2.0

Schematics	PCB Ver. 244*244*1.6 -2116	BOM	Schedule			
			Schematics	Layout	Gerber Out	M/B return
A	A	89-200-Q22000				
B	B	89-200-Q22010				
1.0	1.0	89-380-Q22100				
1.0A	1.0A	89-380-Q22110				
1.0A.	1.0A.	89-380-Q22110				

L2:PWR      DDR Area L2:GND  
L3:GND      DDR Area L3:PWR

Rev:A Initial version:

1. Base on P23G to modify placement and layout

Rev:B

1. Schematic modify for DDR2 clock input to buffer .. etc
2. Codec change to ALC655
3. Del 1394 function
4. Add RTL8100C PCI LAN optional

Rev:1.0

1. Modify component lib.
2. Modify LAN crystal placement

Rev:1.0A

1. Modify ATX 24pin power conn. placemant
2. Add SYS\_FAN smart FAN function

Rev:1.0A.

1. Support INTEL .65 nm CPU(ex. 661/940 etc.)

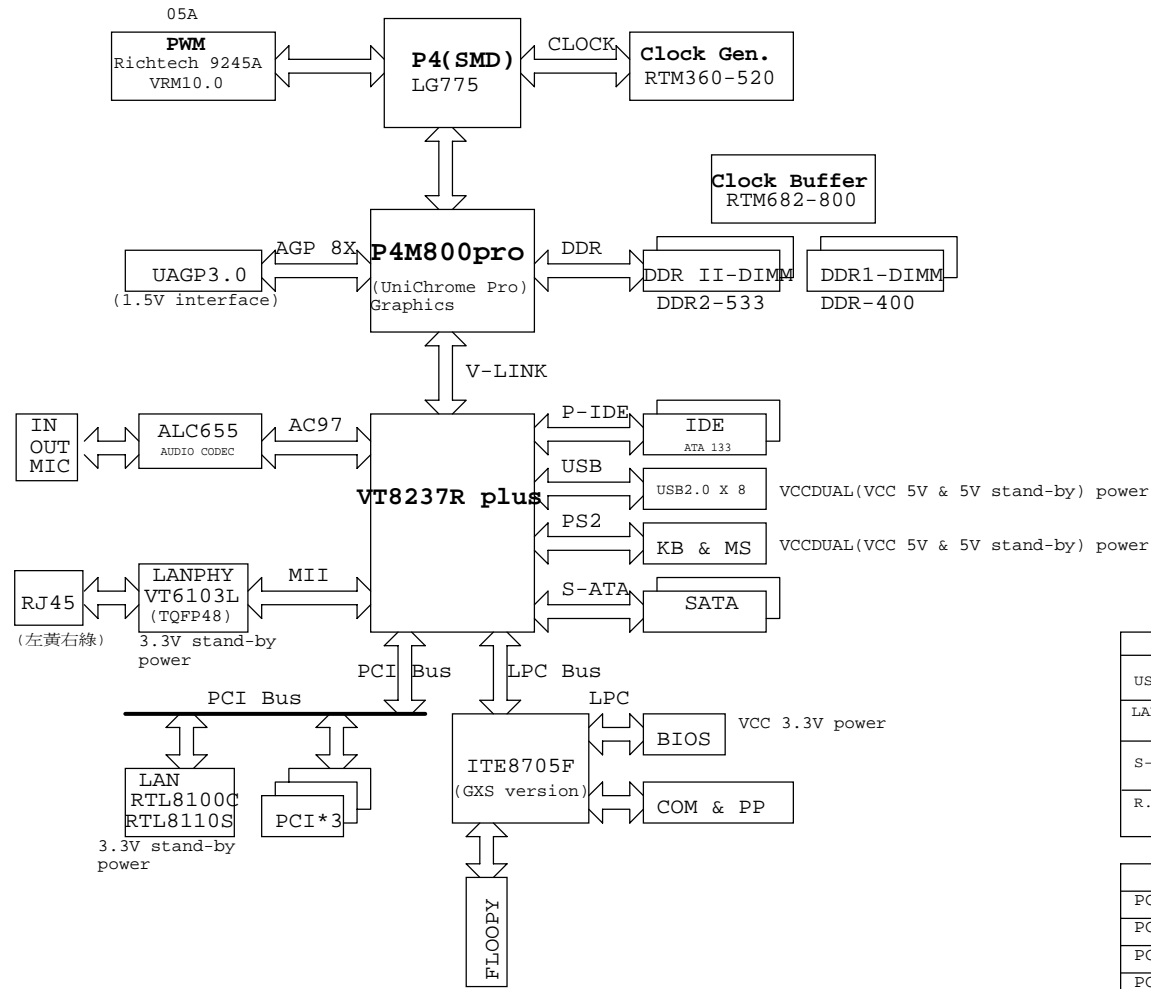
Rev:1.9

1. Support Intel(R) CONORE CPU
2. Modify IT8705 to IT8712 Co-Lay IT8718

Rev:2.0

1. Change R500,R506's value & remove C229 & add R589,C404,C405 for VRD11.
2. Remove R107 & add C406 & change C87's value for HW monitor.
3. Add 0.1uF(C403) CAP for waking up by ring question.

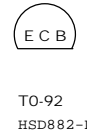
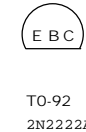
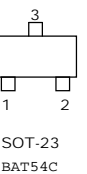
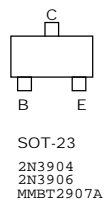
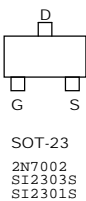
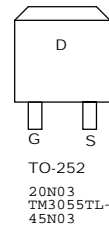
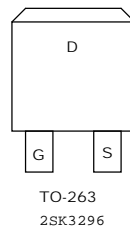
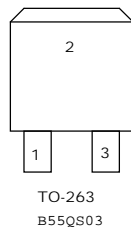
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Title Cover Page			
Size Custom	Document Number P4M800PRO-M		Rev 2.0
Date:	Thursday, June 29, 2006	Sheet	1 of 29



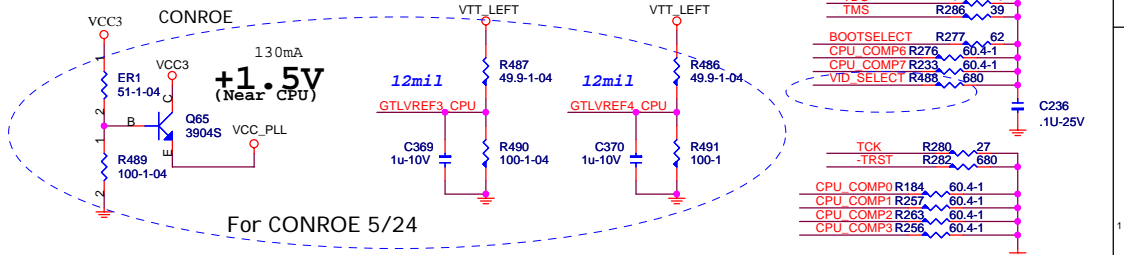
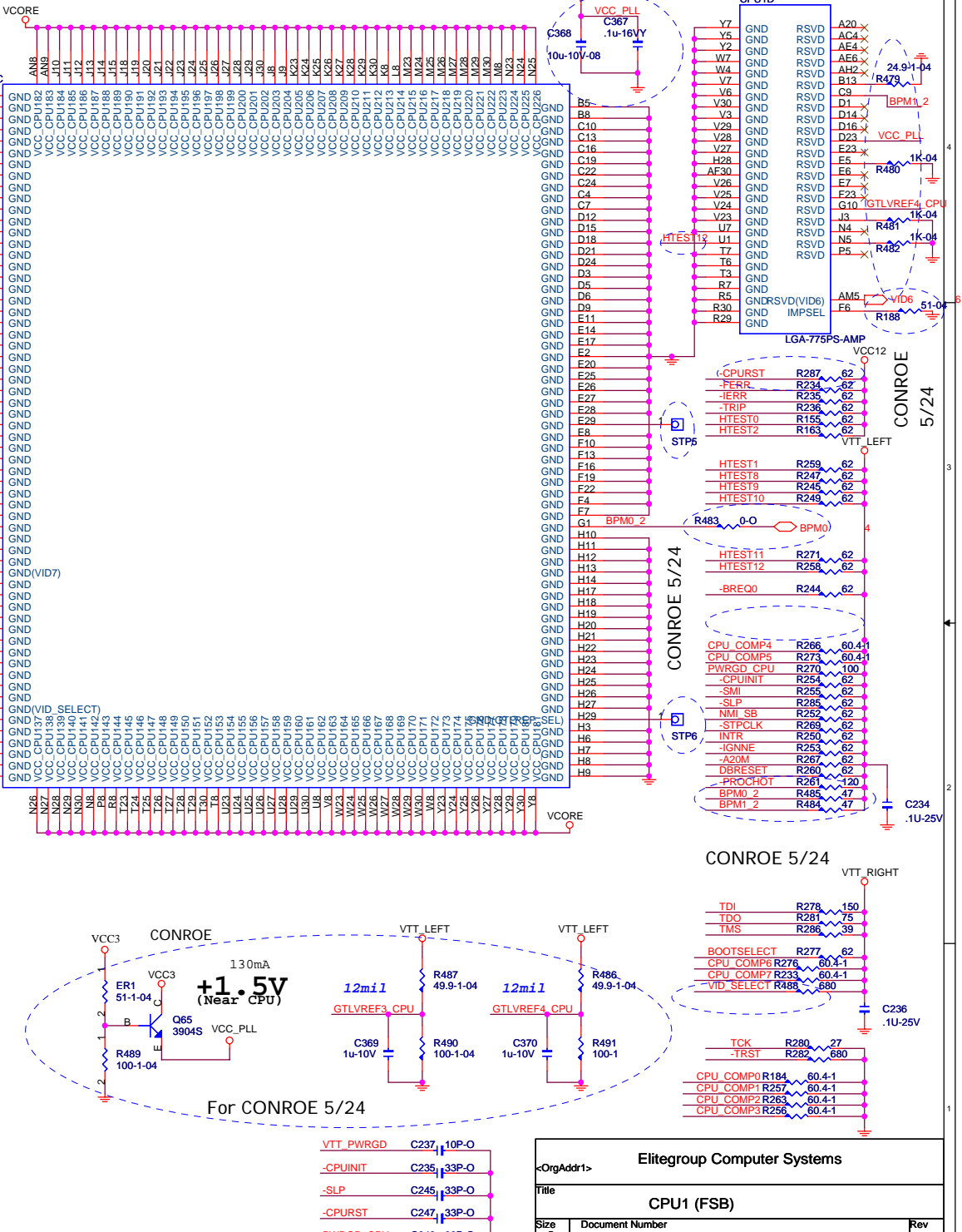
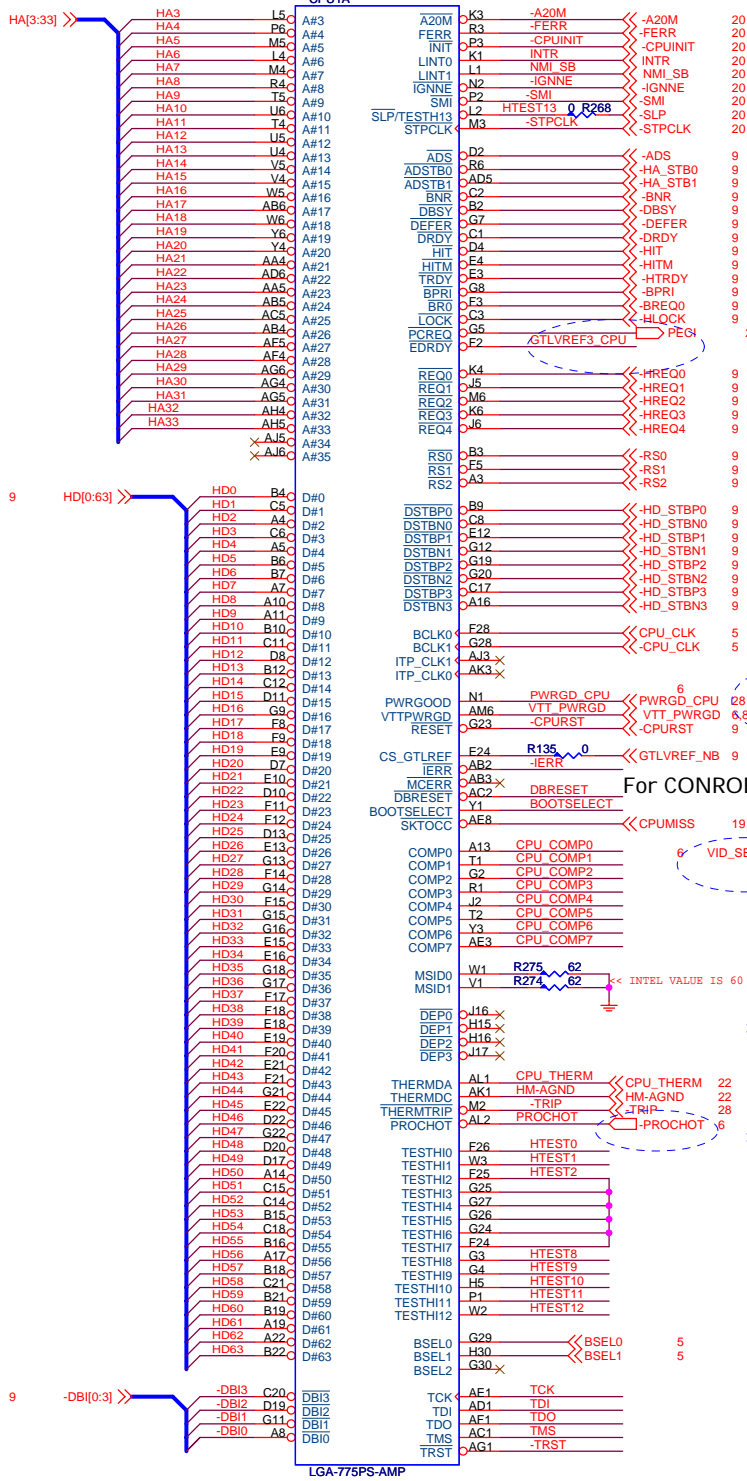
	Impedance	PCB 2116
USB_DT0+/-	(45/90)	8/8/8(47/87) 8/5/8(47/80 allegro) 7.5/7.5/7.5(50/90 guide)
LAN RX+/- TX+/-	(50/100)	8/8/8(47/87) 8/12/8(47/91 guide)
S-ATA	(50/100)	20/6/8/6/20(56/103) 17/6/8/6/17(guide) group mismatch 20 mil.
R.G.B	(37.5)	50/10/10/10/10/50 12/7/12/7/12(guide) Put 75 ohm on CON

PCI Bus Resource			
PCI1	AD19	INTA, BCD	REQ0
PCI2	AD20	INTB, CDA	REQ1
PCI3	AD21	INTC, DAB	REQ2
PCI LAN	AD22	INTB	REQ3

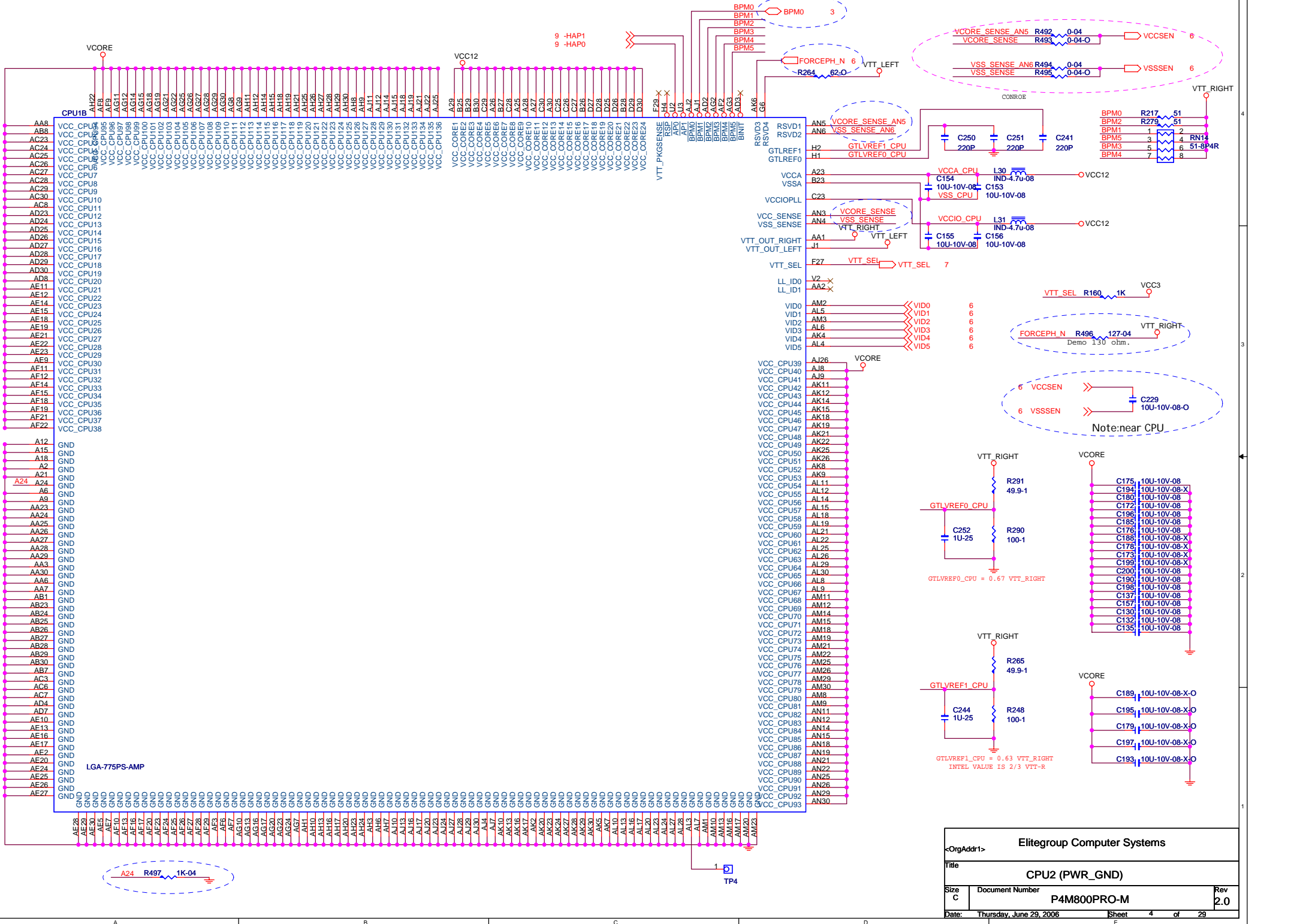
22U/25DE	5*7 mm
100U/16DE	6.3*11 mm
220U/10DE	6.3*11 mm
470U/16DE	8*11 mm
1000U/10DE	8*14 mm
1500U/16DE	10*25 mm
3300U/25DE	10*25 mm



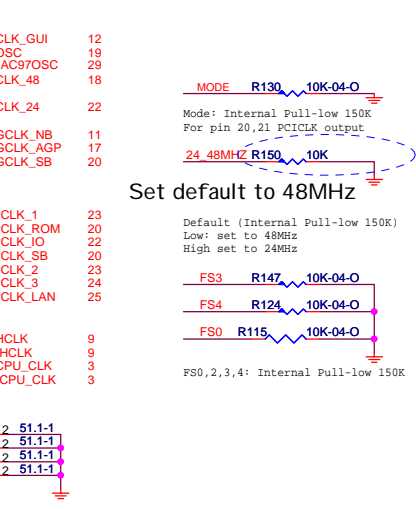
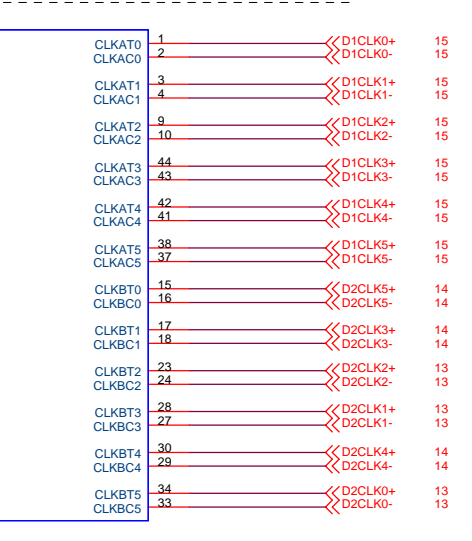
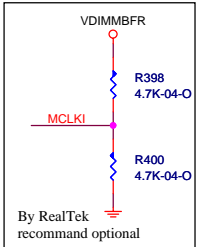
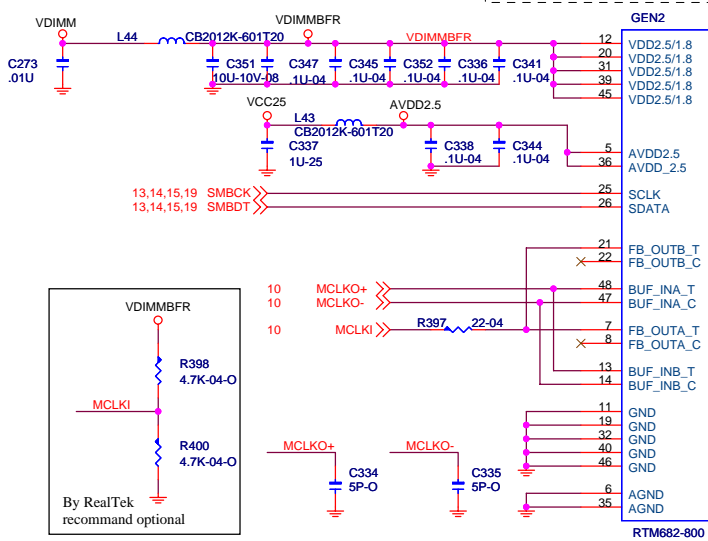
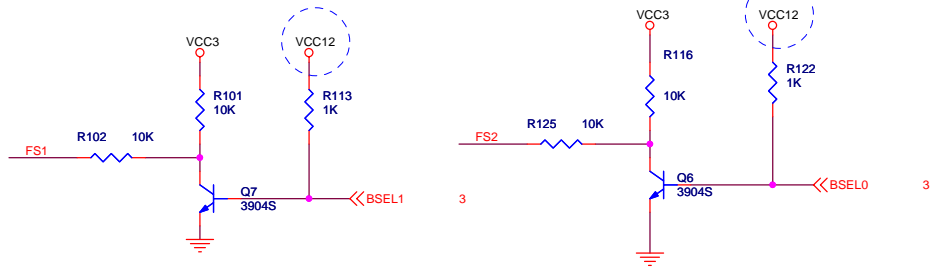
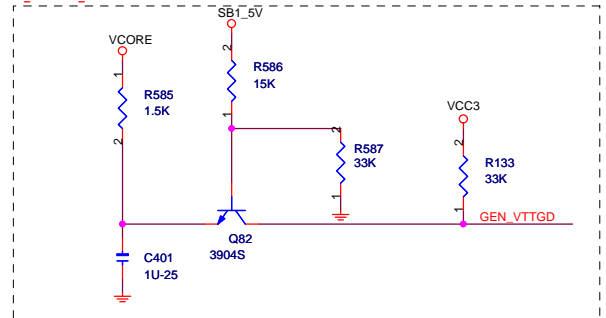
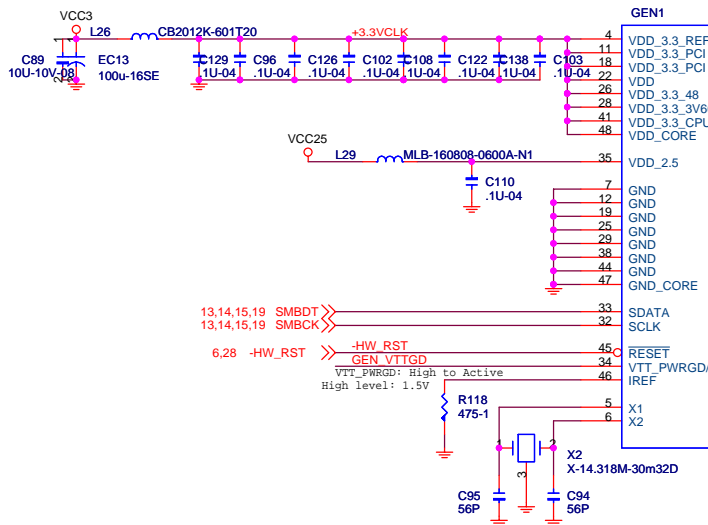
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Size: Custom	Document Number: <b>P4M800PRO-M</b>		Rev: <b>1.9</b>
Date: Friday, May 26, 2006	Sheet 2 of 29		



Elitegroup Computer Systems			
Title			
CPU1 (FSB)			
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Date:	Friday, June 30, 2006	Sheet	3 of 29



<b>Elitegroup Computer Systems</b>			
Title			
<b>CPU2 (PWR_GND)</b>			
Size	Document Number	Rev	
C	P4M800PRO-M	2.0	
Date:	Thursday, June 29, 2006	Sheet	4 of 29



**Set default to 48MHz**

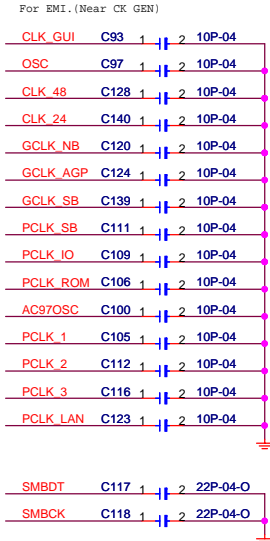
Mode: Internal Pull-low 150K  
For pin 20, 21 PCICLK output

24 48MHZ R150 10K

Default (Internal Pull-low 150K)  
Low: set to 48MHz  
High set to 24MHz

FS3 R147 10K-04-O  
FS4 R124 10K-04-O  
FS0 R115 10K-04-O

FS0,2,3,4: Internal Pull-low 150K

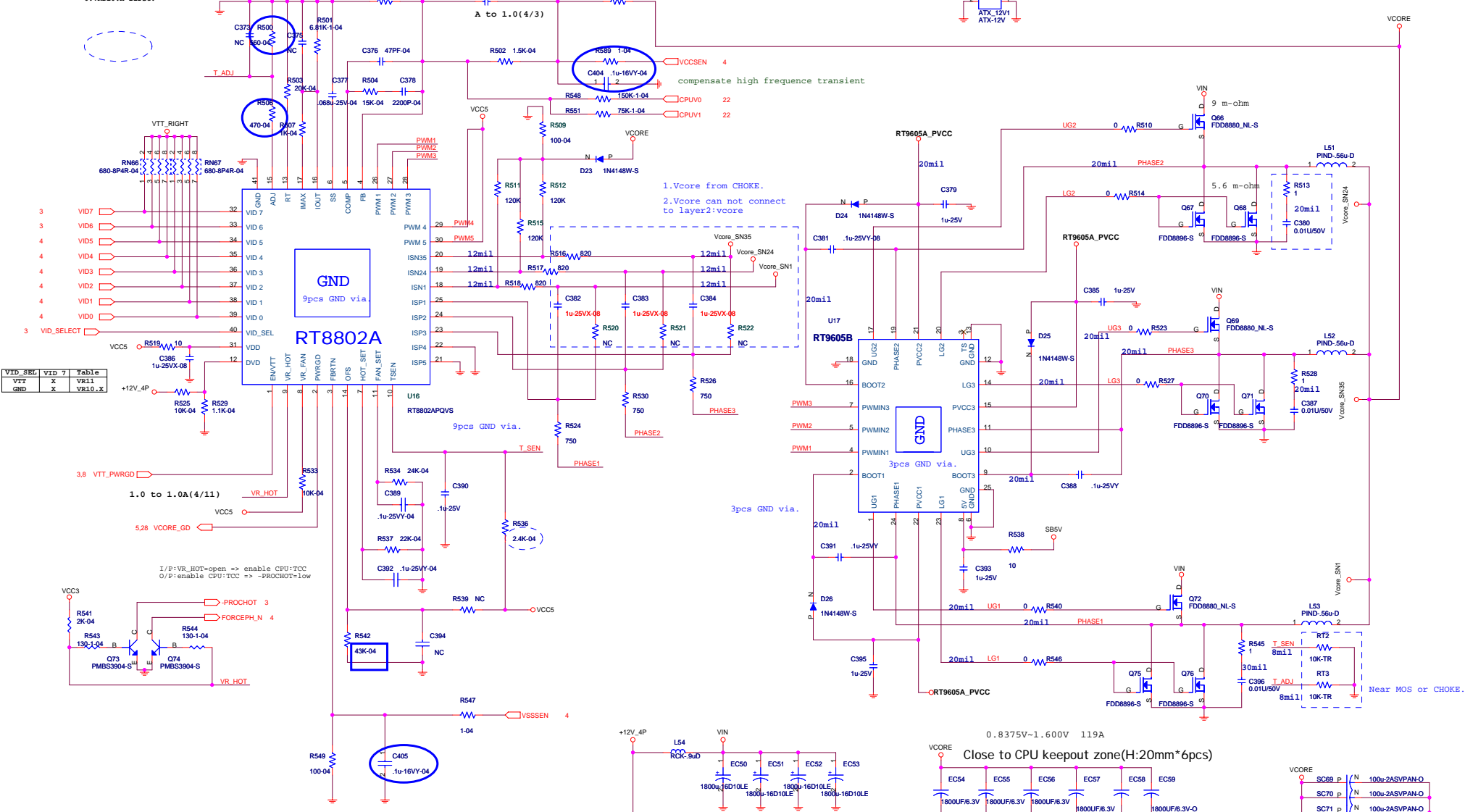


775CPU BESL				FS PIN			SB Strap
FSB	BSEL1	BSEL0		FS2	FS1	FS0	GPIOC
533	133	0	1	0	1	0	l=Auto
800	200	1	0	1	0	0	l=Auto
1066	266	0	0	1	1	0	l=Auto

FS0 = Low;  
FS1 = / BSEL1;  
FS2 = / BSEL0;

CPUV1D1	CPUV1D0	VCORE
1	1	Normal
1	0	1%
0	1	2%
0	0	3%

New RT8802A don't need it.  
Power on to latch  
0:VRD10.X first.



VID_SEL1	VID_7	Table
VTT	X	VR11
GND	X	VR10.X

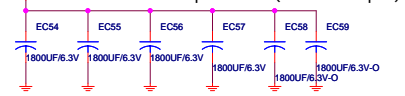
I/P:VR\_HOT=open => enable CPU:TCC  
O/P:enable CPU:TCC => -PROCHOT=low

**05A**  
C229:10UF-> NC  
R500:390 ohm-> 470 ohm  
R506:47 ohm-> 150 ohm  
R542:43K-> 18K  
OS-CON(560UF/2.5V): change to CT1,CT3,CT4,CT5,CT6  
POS-Cap(100UF/4V):add C397,C398,C399  
Remove(1800UF/6.3V):EC54,EC55,EC56,EC57

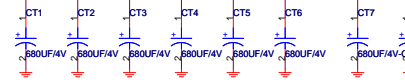
CPUV1D1	CPUV1D0	VCORE
0	0	Normal
0	1	0.025V
1	0	0.05V
1	1	0.075V

Patch RT9605A issue.  
5VSB first and then +12V.

0.8375V-1.600V 119A  
Close to CPU keepout zone(H:20mm\*6pcs)



Close to under CPU Heat-Sink(H:8mm\*9pcs)

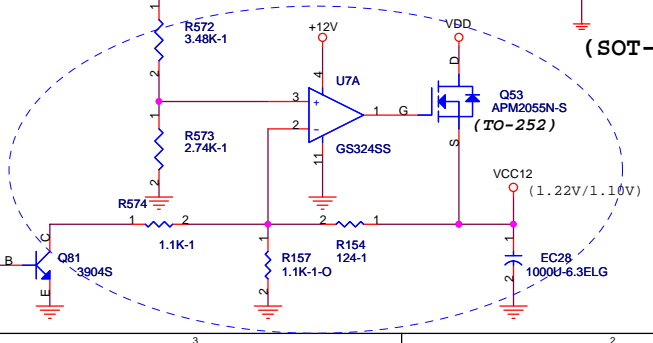
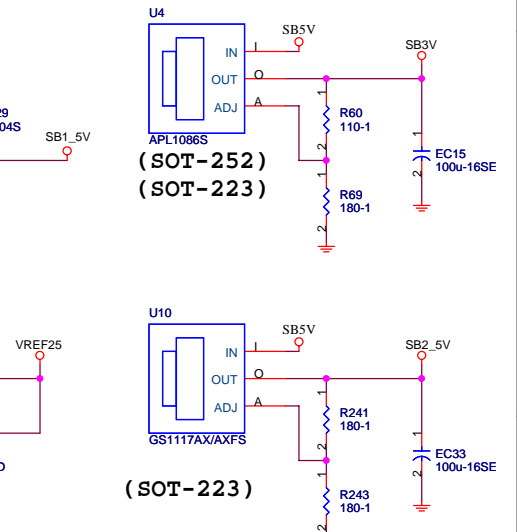
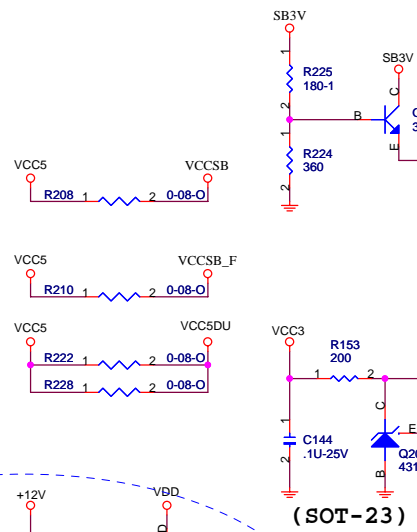
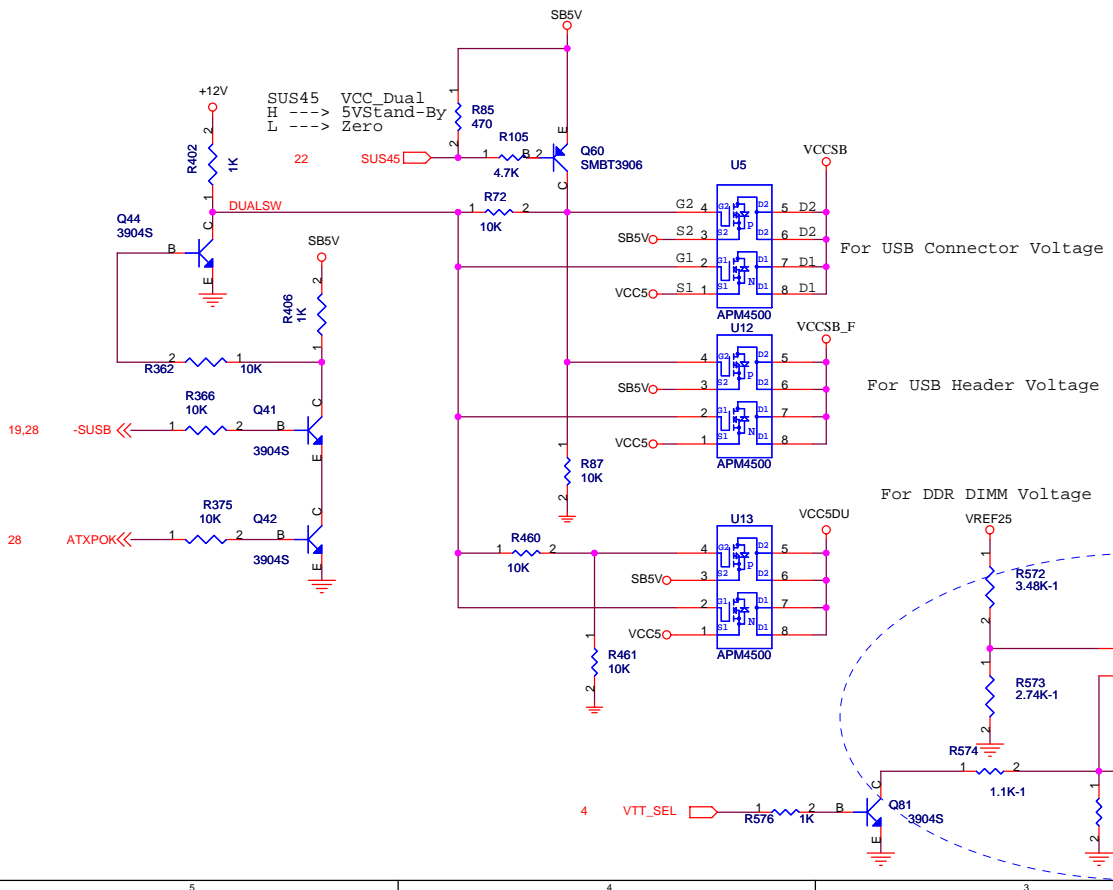
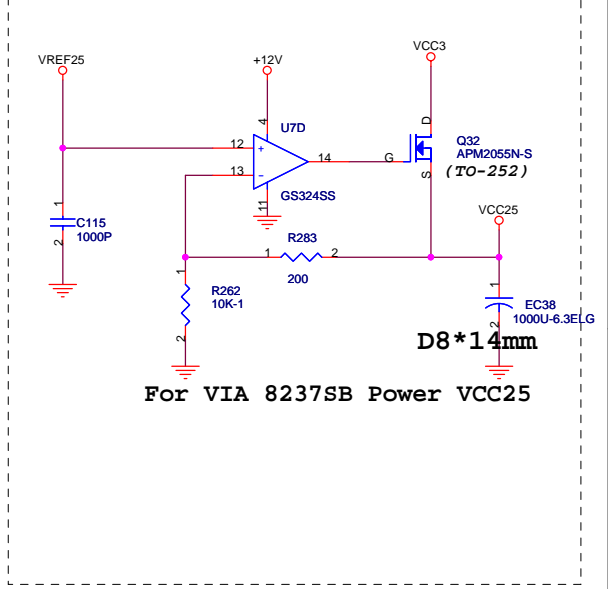
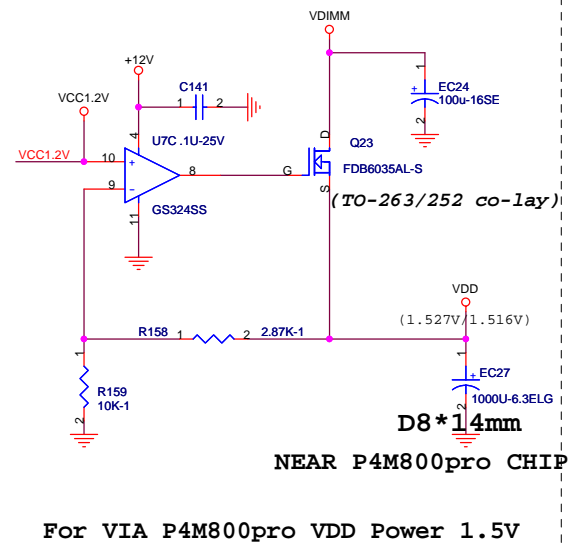
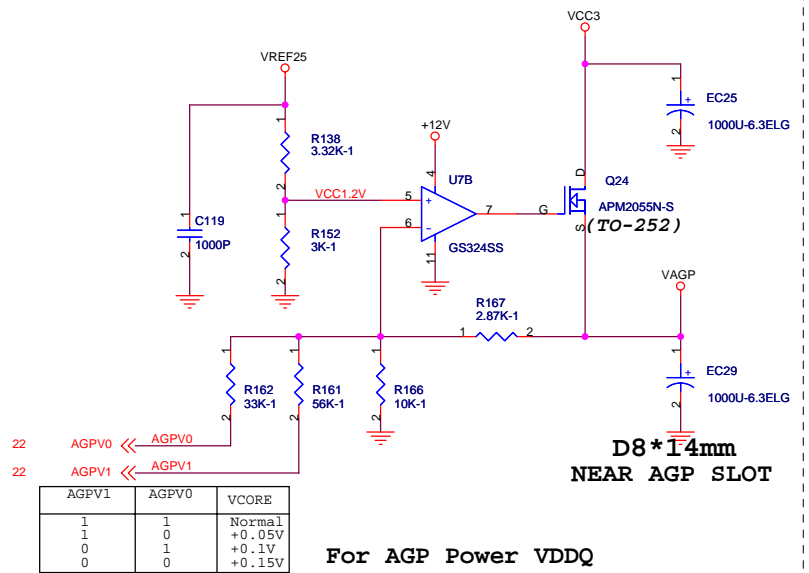


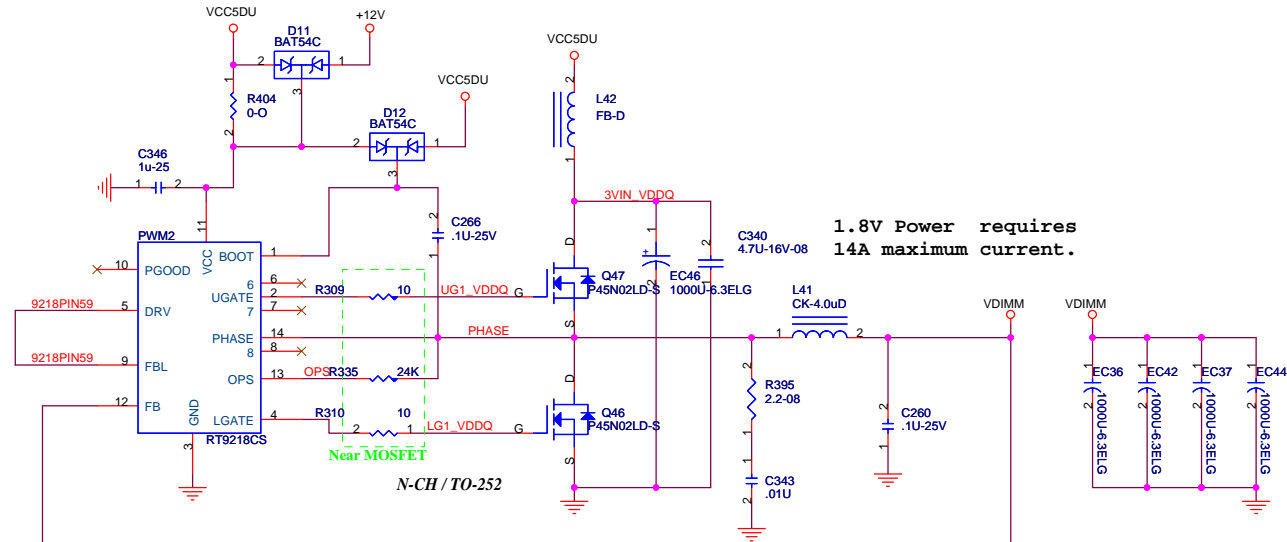
Elitegroup Computer Systems

File: **Vcore POWER**

Size C	Document Number	Rev
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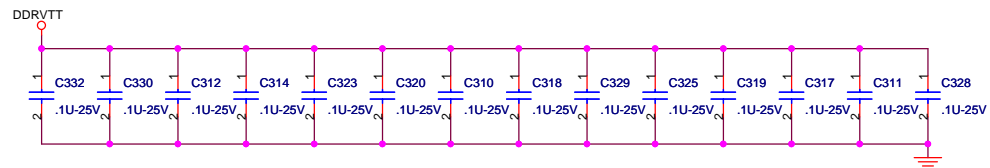




$$V_{OUT} = 0.8V(1 + R_t / R_b)$$

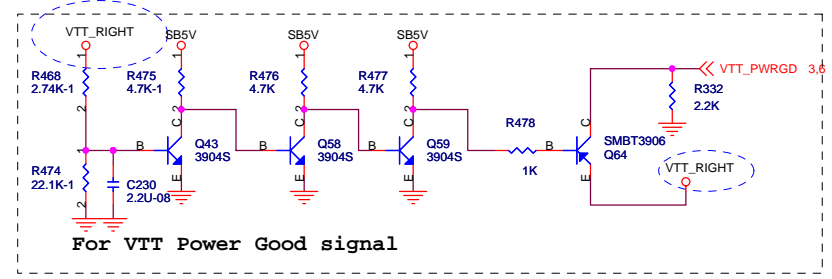
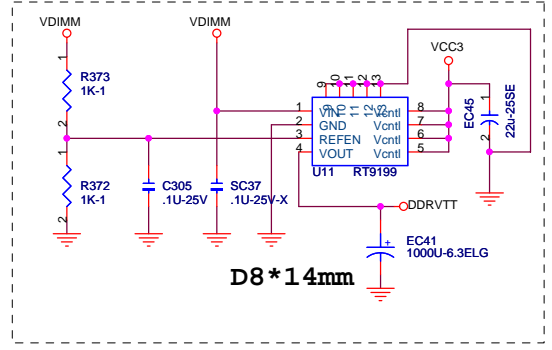
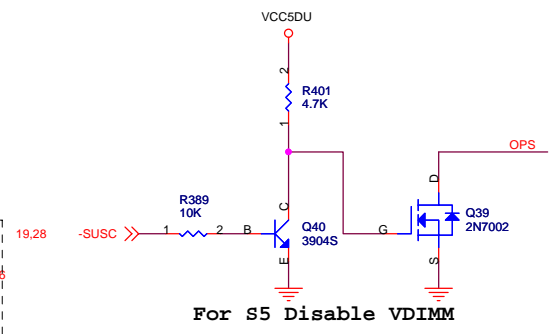
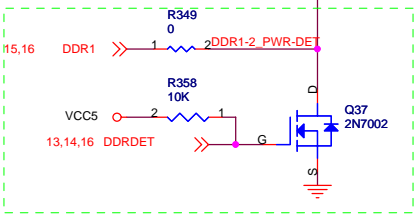
R15: OPEN=1.8V, LOW=2.5V

R15 => Low=2.5V ( DDR2\_DET\_L = Floating ), If don't install DDR1 & DDR2 .  
 R15 => Open=1.8V ( DDR2\_DET\_L = Low ), If install DDR1 & DDR2 at the same time .

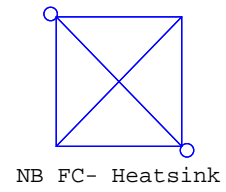
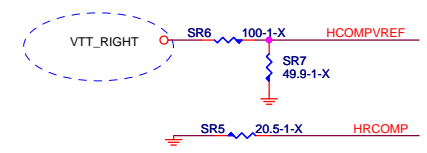
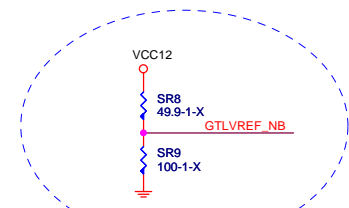
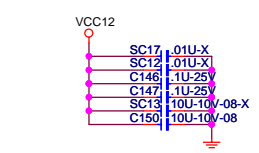
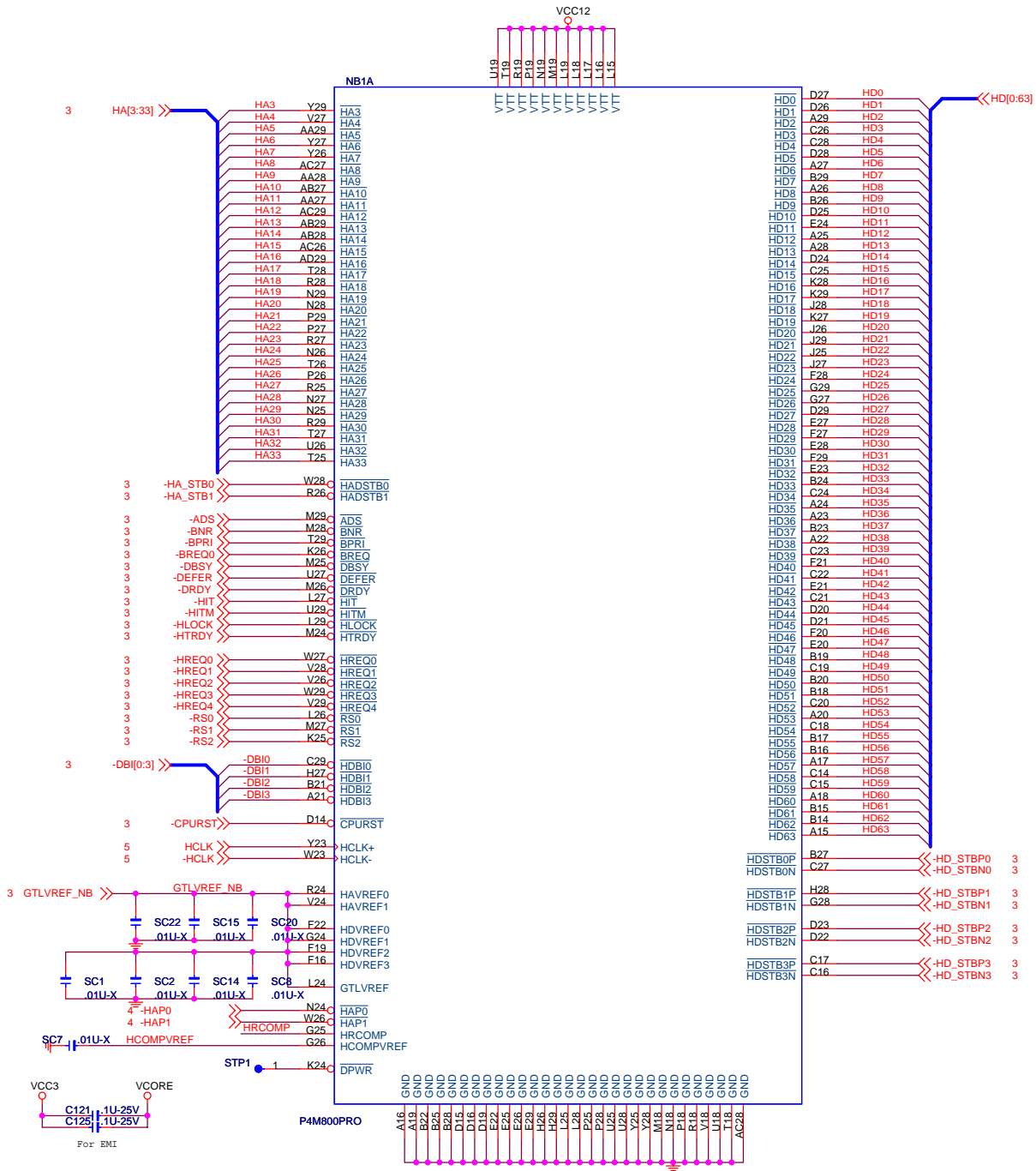


18 MEMVADJ2  
 18 MEMVADJ1  
 18 MEMVADJ0

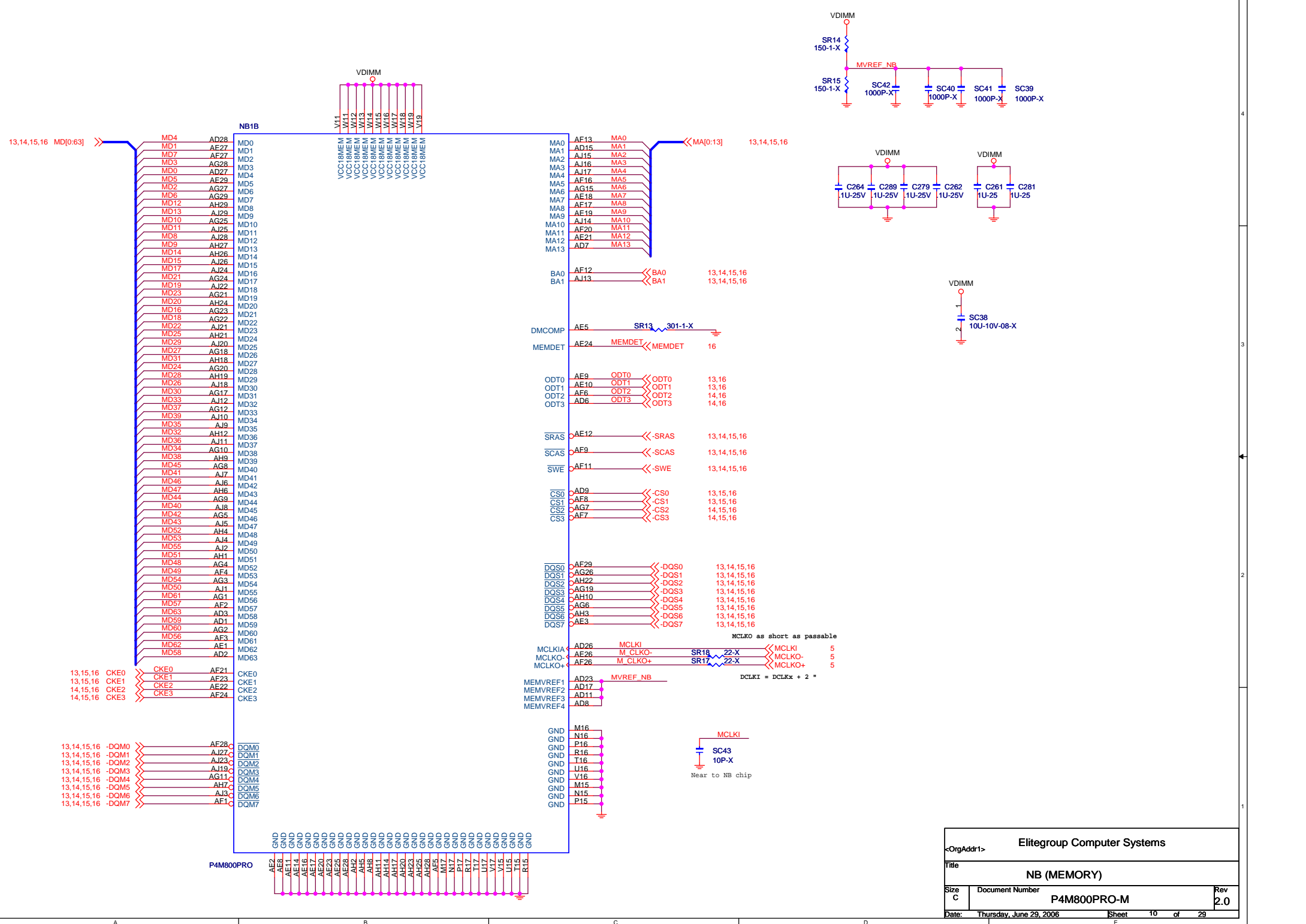
MEMV2	MEMV1	MEMV0	DDR Vltage
1	1	1	+0.35V (350mV)
1	1	0	+0.3V (300mV)
1	0	1	+0.25V (250mV)
1	0	0	+0.2V (200mV)
0	1	1	+0.15V (150mV)
0	1	0	+0.1V (100mV)
0	0	1	+0.05V (50mV)
0	0	0	Normal (1.8V or 2.5V)



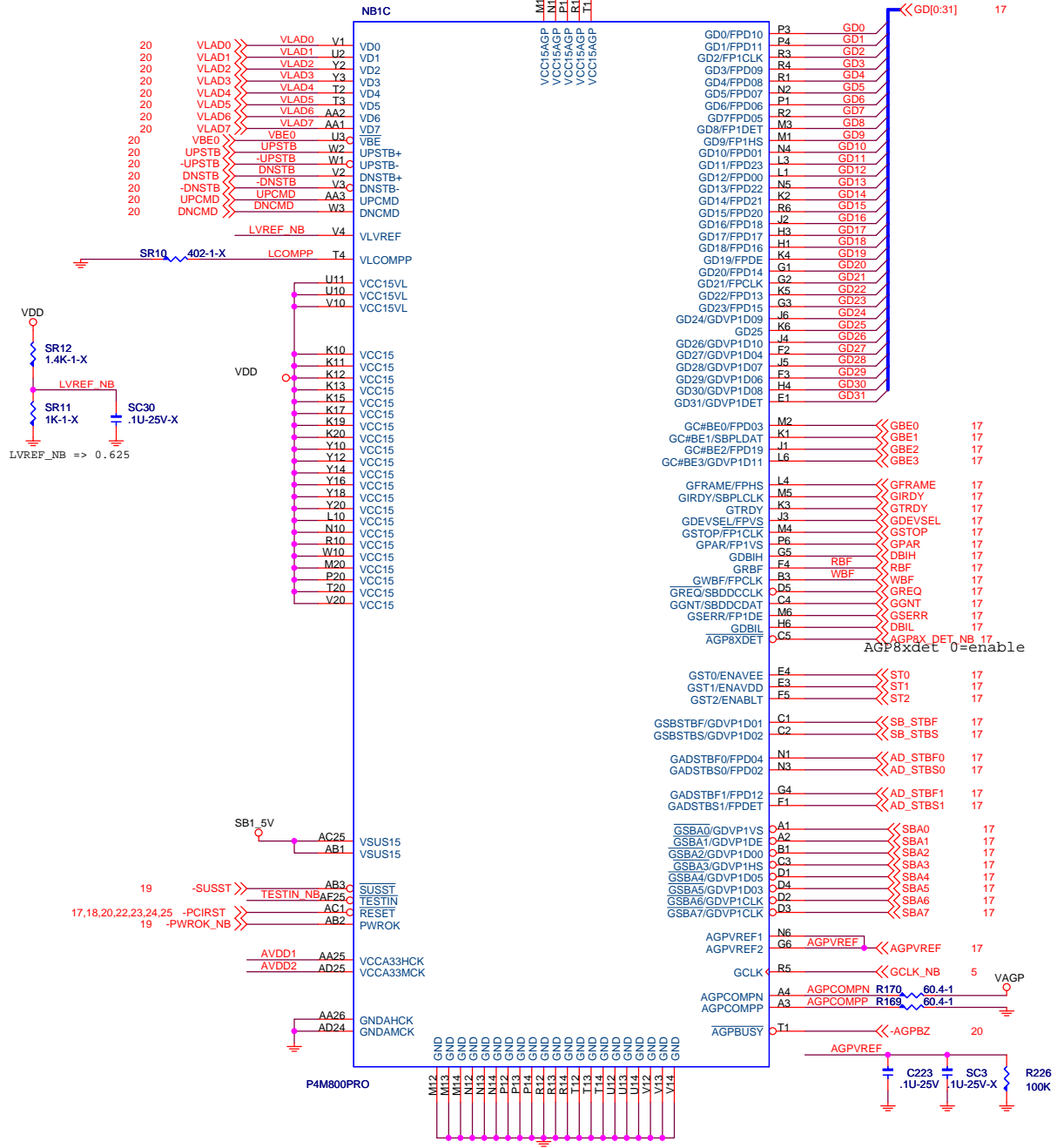
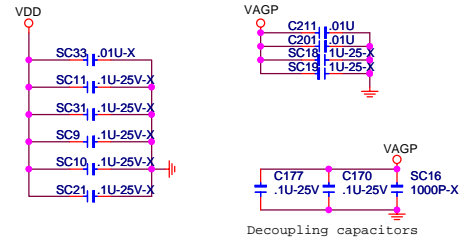
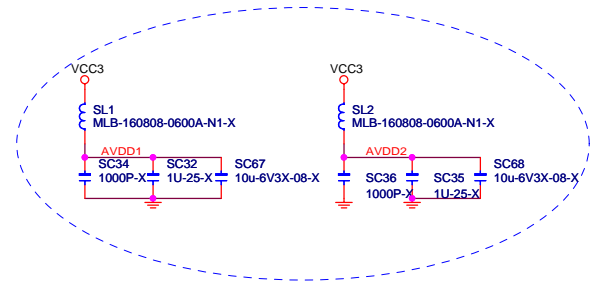
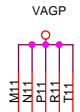
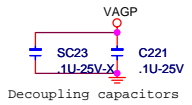




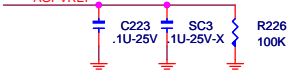
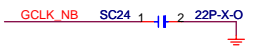
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Size C	Document Number	P4M800PRO-M	Rev 2.0
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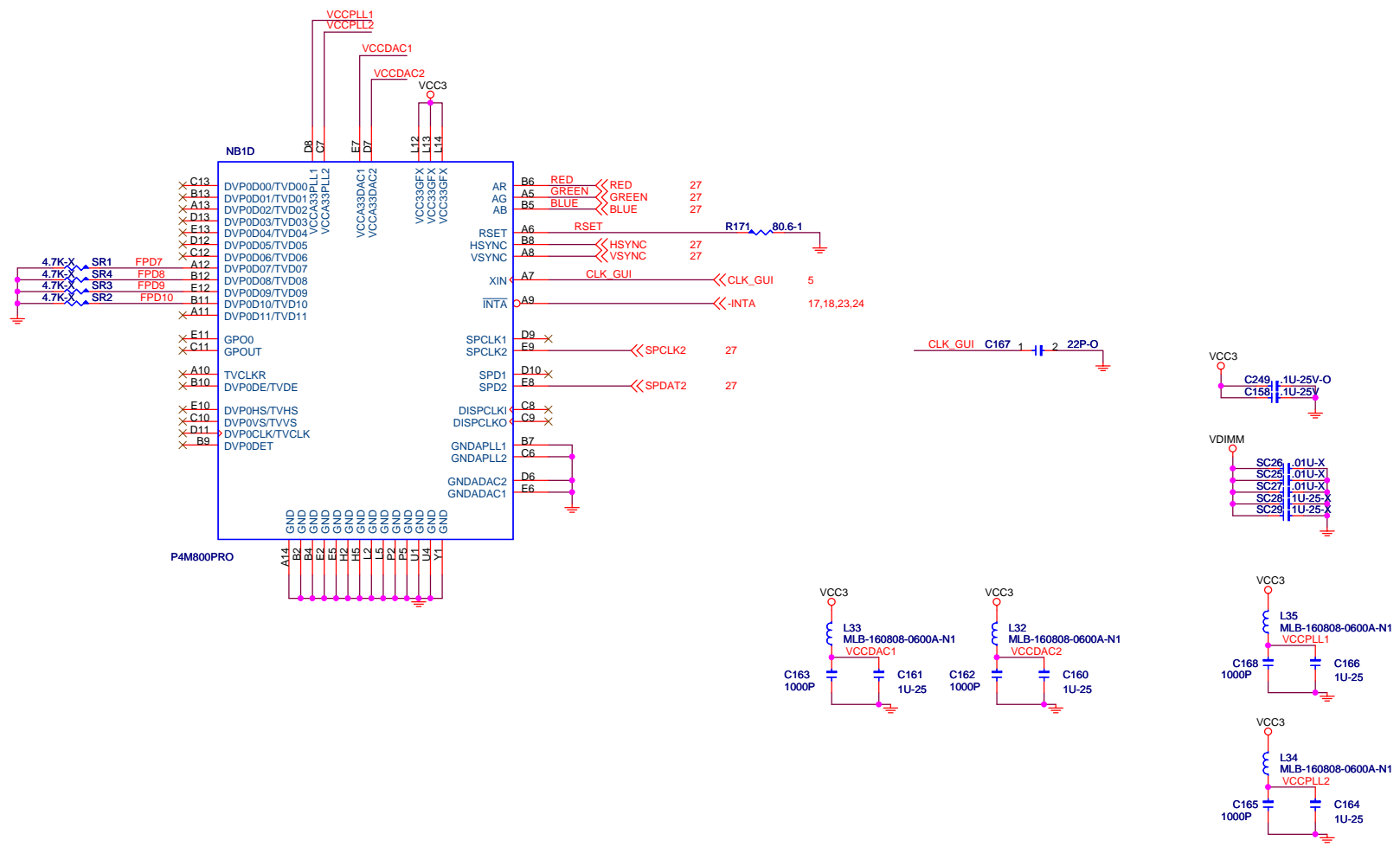
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<b>Title</b>			
<b>NB (MEMORY)</b>			
<b>Size</b>	<b>Document Number</b>	<b>P4M800PRO-M</b>	<b>Rev</b>
<b>C</b>			<b>2.0</b>
<b>Date:</b>	Thursday, June 29, 2006	<b>Sheet</b>	10 of 29



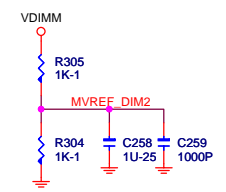
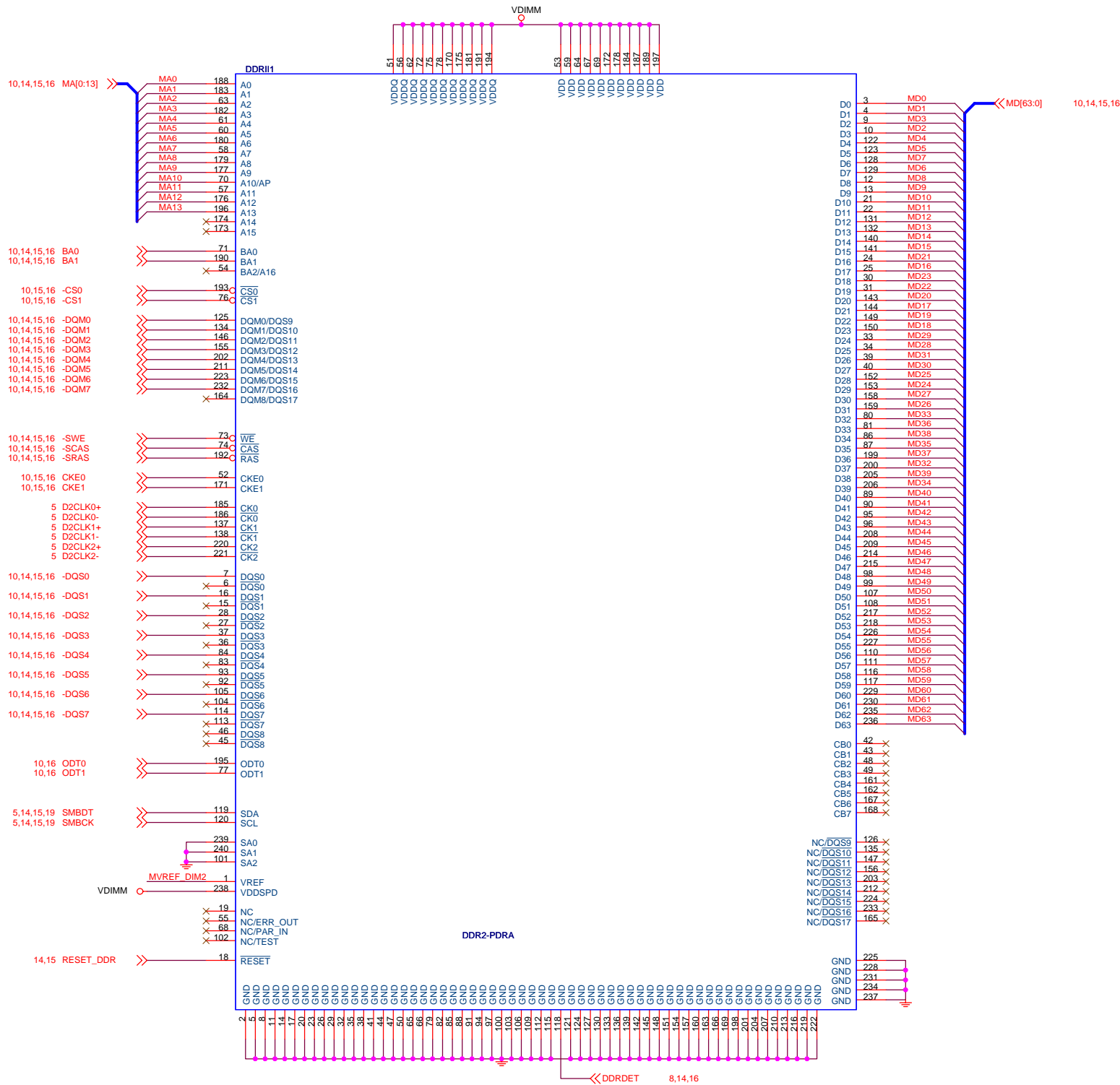
Strapping For NB\_TEST Mode  
 TESTIN RBF WBF  
 1 x x Disable all TEST mode



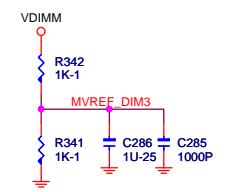
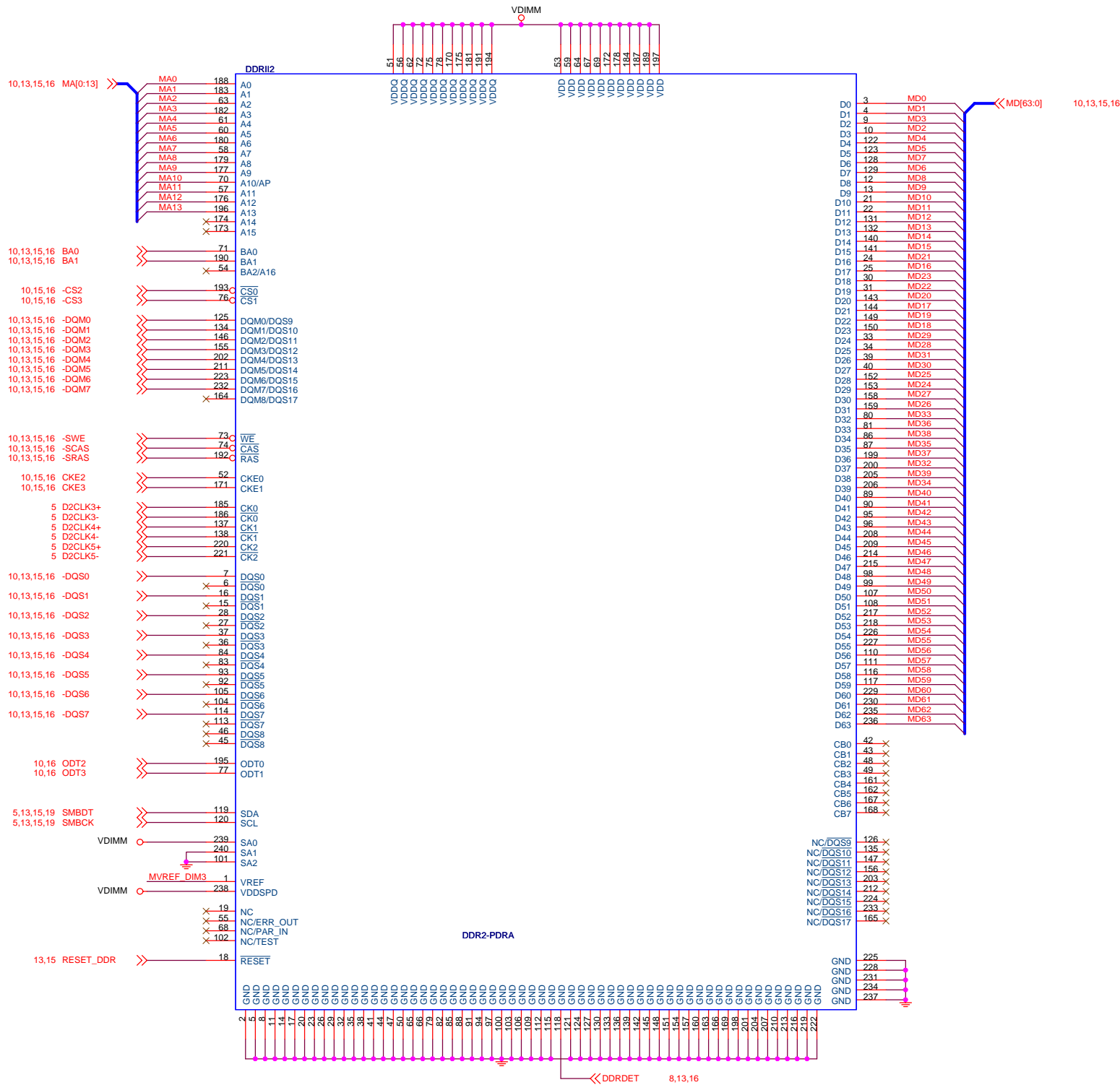
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NB (AGP_VLINK)			
Size	Document Number	Rev	
C	P4M800PRO-M	2.0	
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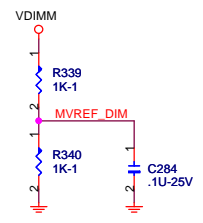
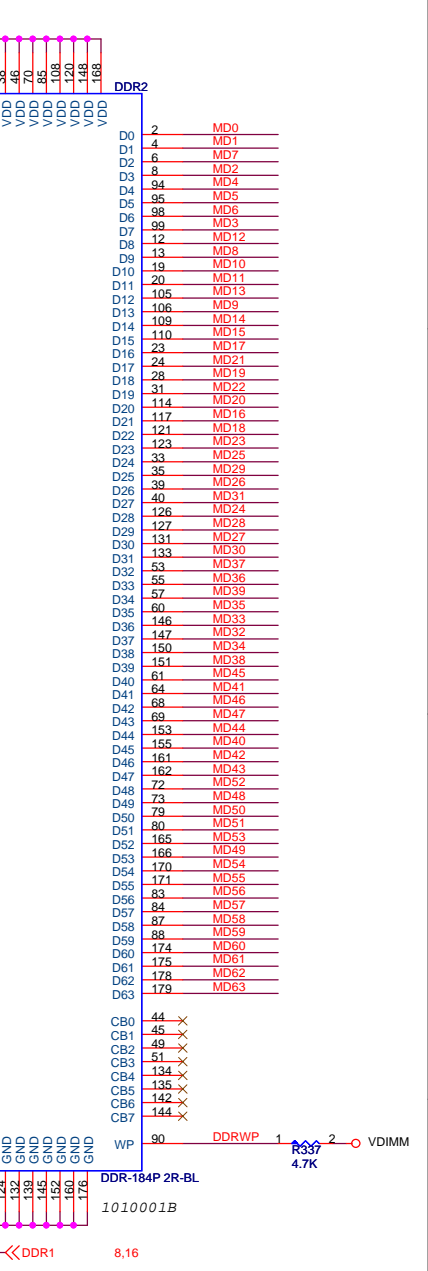
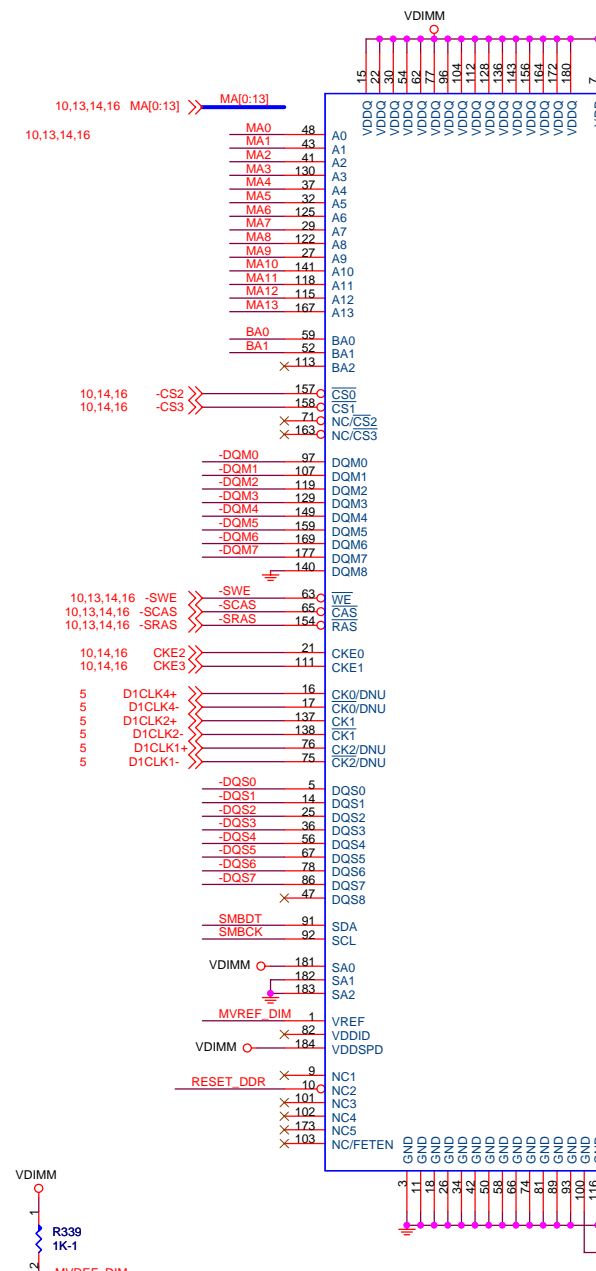
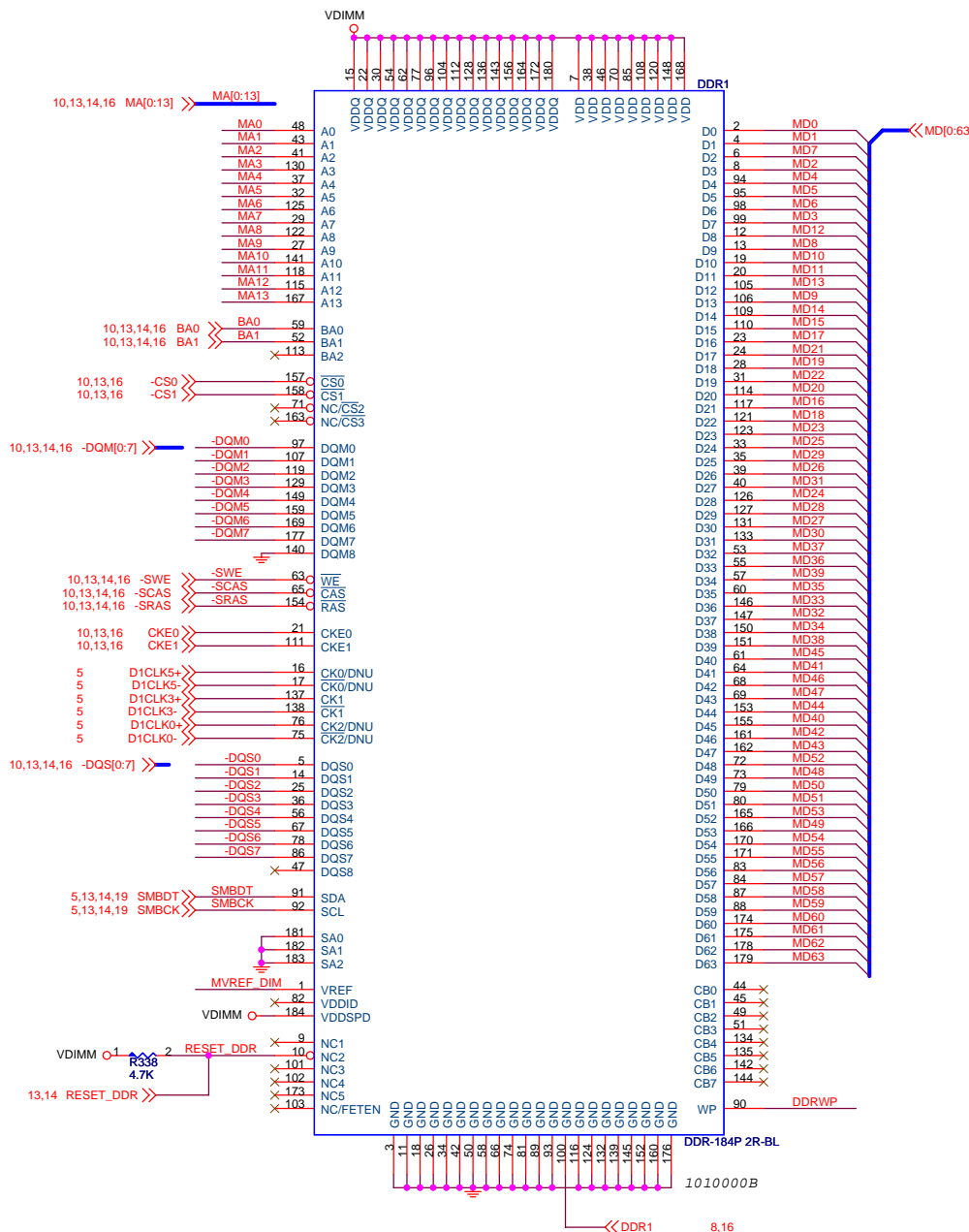
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<b>Title</b>			
<b>NB (VGA)</b>			
Size	Document Number		Rev
Custom	P4M800PRO-M		2.0
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<b>Elitegroup Computer Systems</b>	
<b>DDR2 SLOT1</b>	
Size	Document Number
Custom	P4M800PRO-M
Date:	Thursday, June 29, 2006
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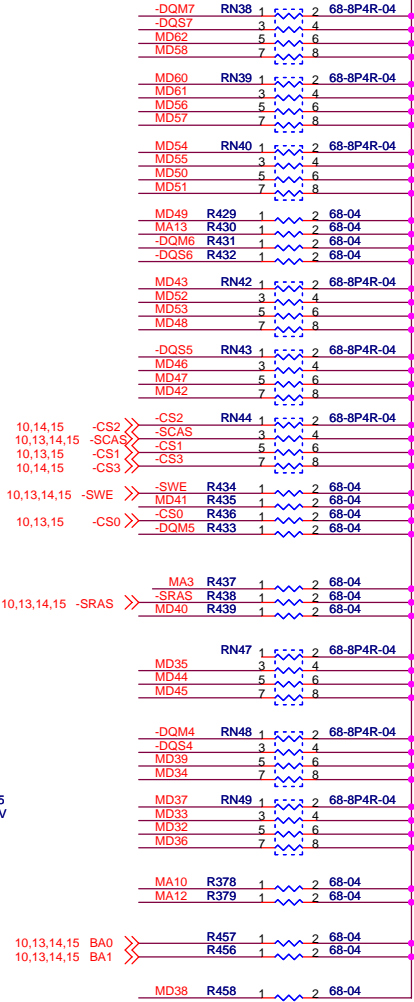
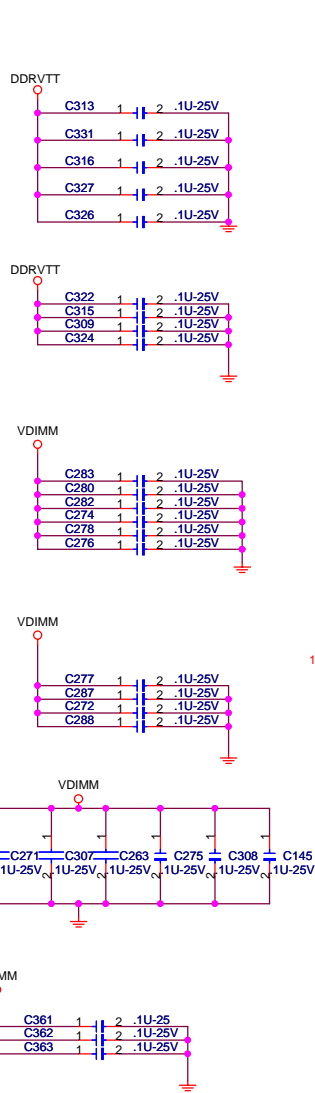


<b>Elitegroup Computer Systems</b>	
Title <b>DDR2 SLOT2</b>	
Size Custom	Document Number <b>P4M800PRO-M</b>
Date: Thursday, June 29, 2006	Rev <b>2.0</b>
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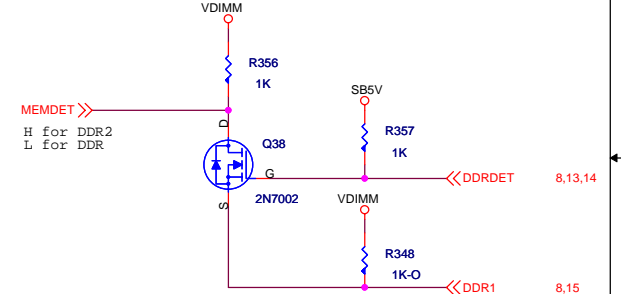
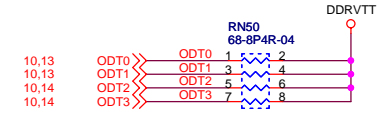
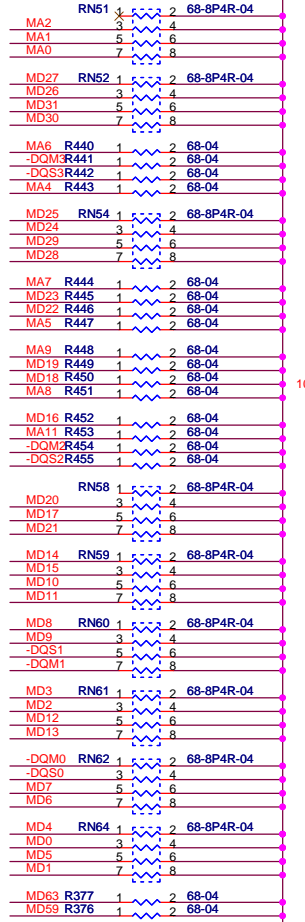


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Title: <b>DDR1</b>			
Size: Custom	Document Number: <b>P4M800PRO-M</b>		Rev: <b>2.0</b>
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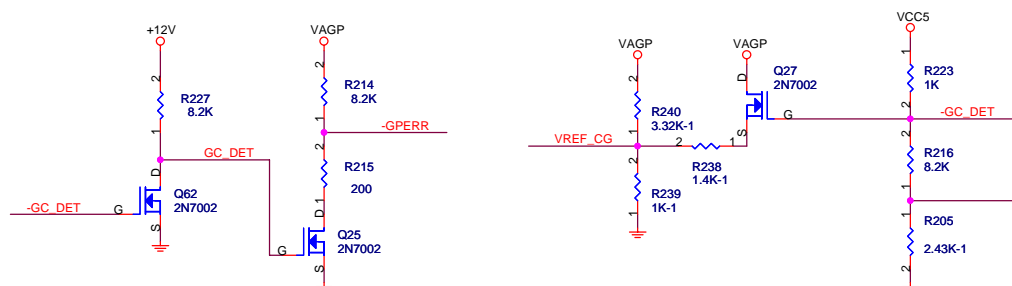
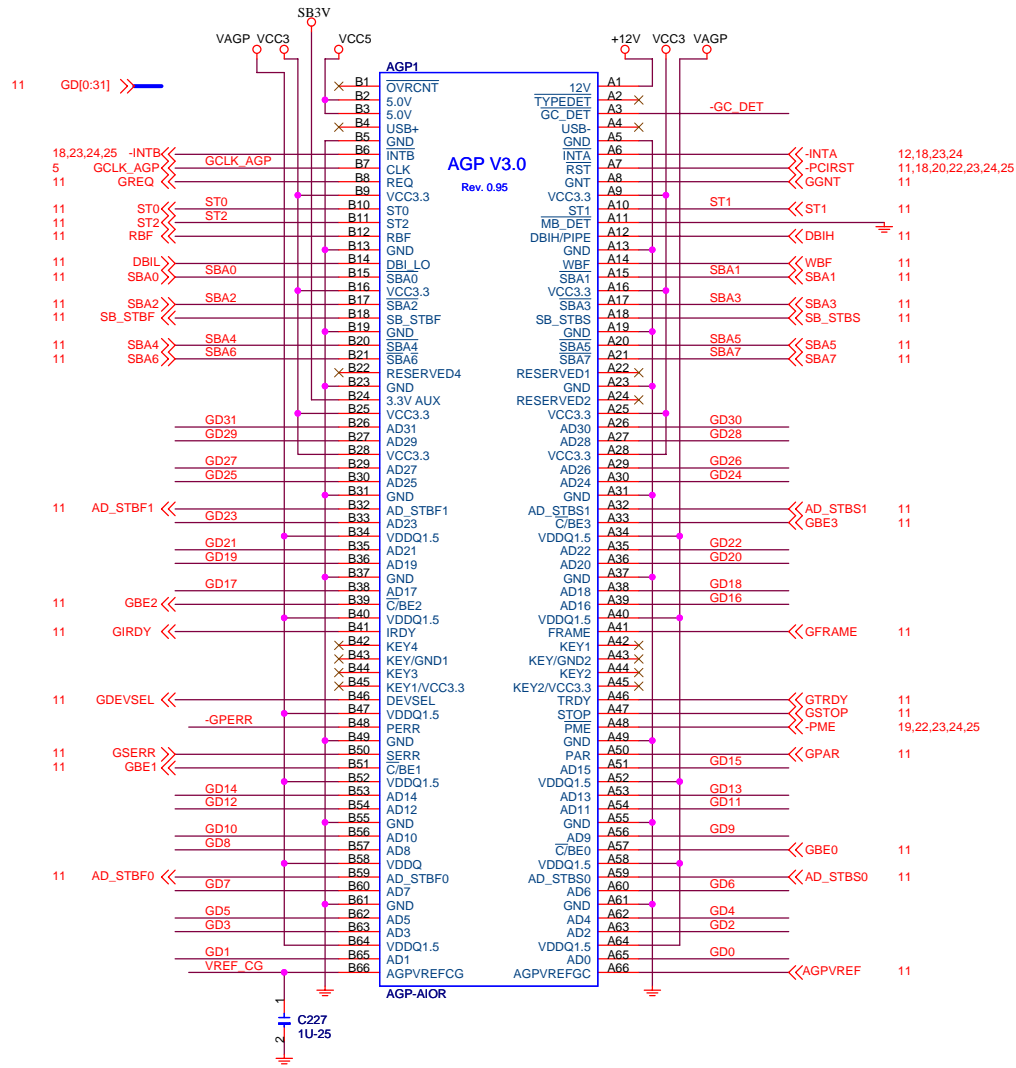
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 10,13,14,15 MA[0:13] >> MA[0:13]  
 10,13,14,15 -DQM[0:7] >> -DQM[0:7]  
 10,13,14,15 -DQS[0:7] >> -DQS[0:7]



10,14,15 CKE3 >> CKE3 RN65  
 10,13,15 CKE1 >> CKE1  
 10,14,15 CKE2 >> CKE2  
 10,13,15 CKE0 >> CKE0

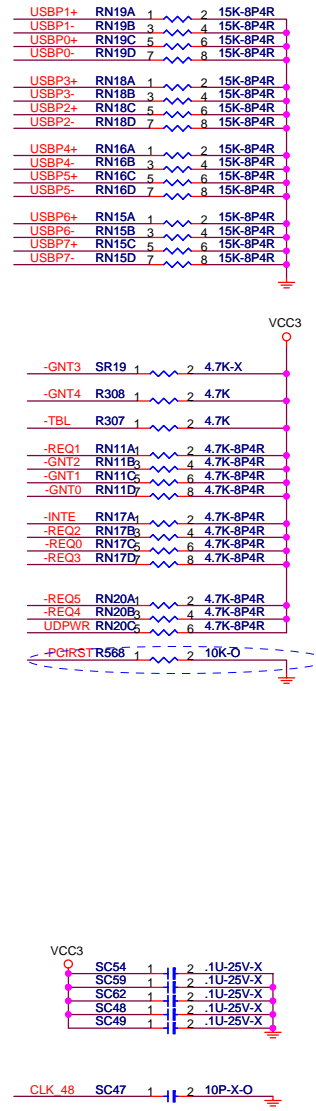
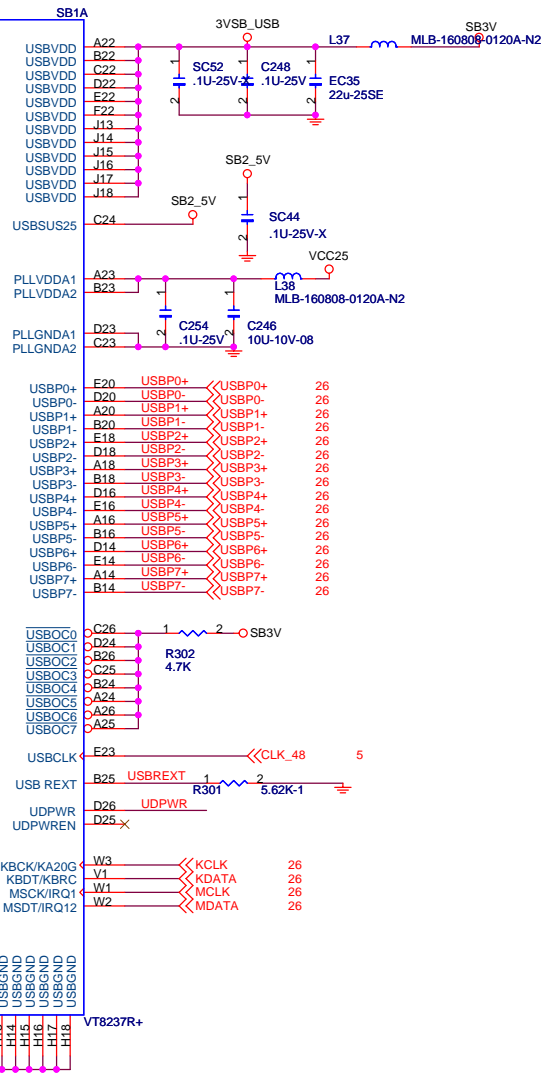
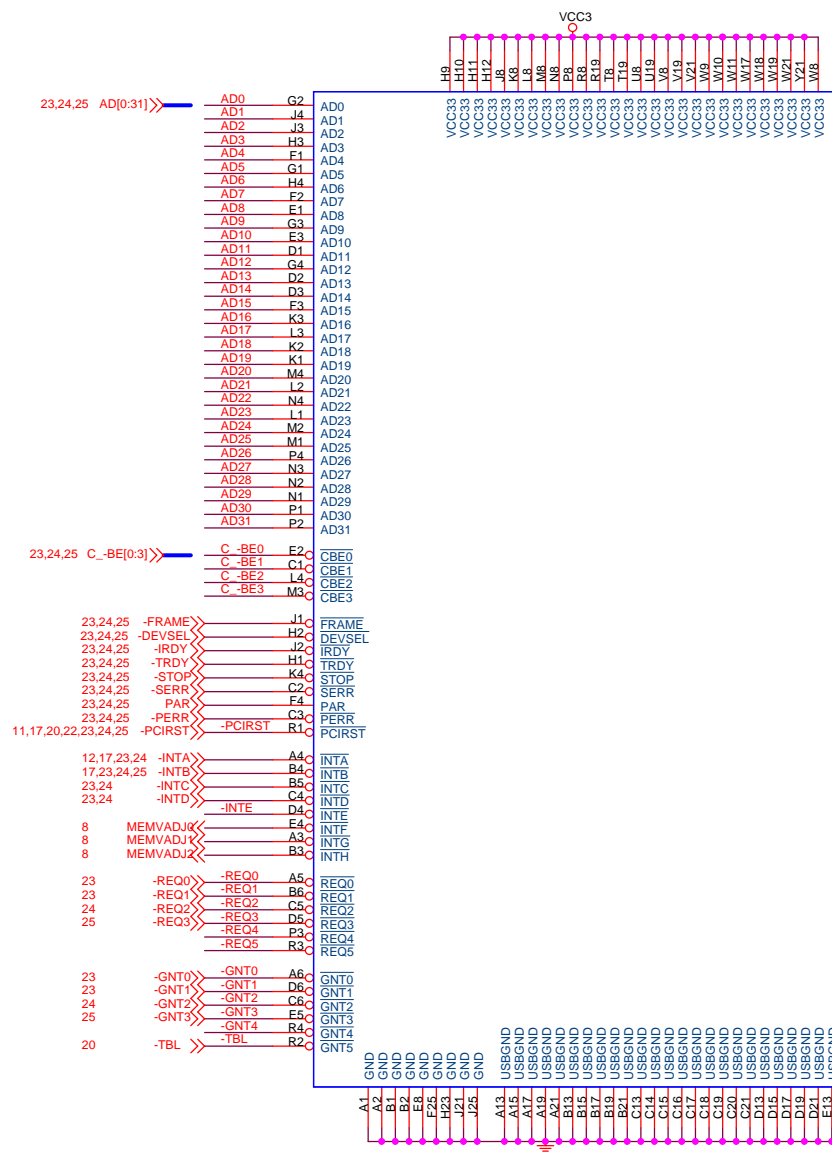


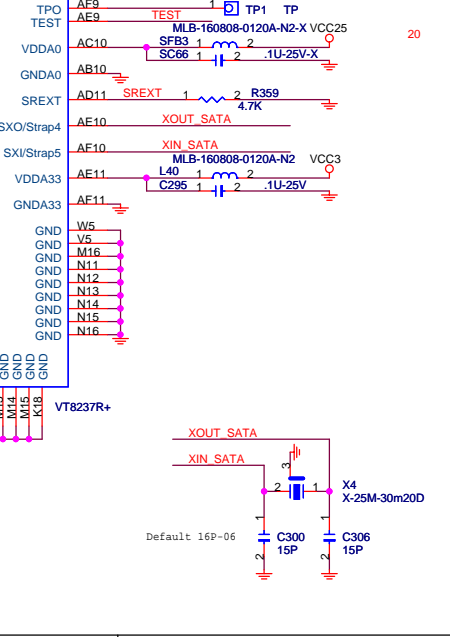
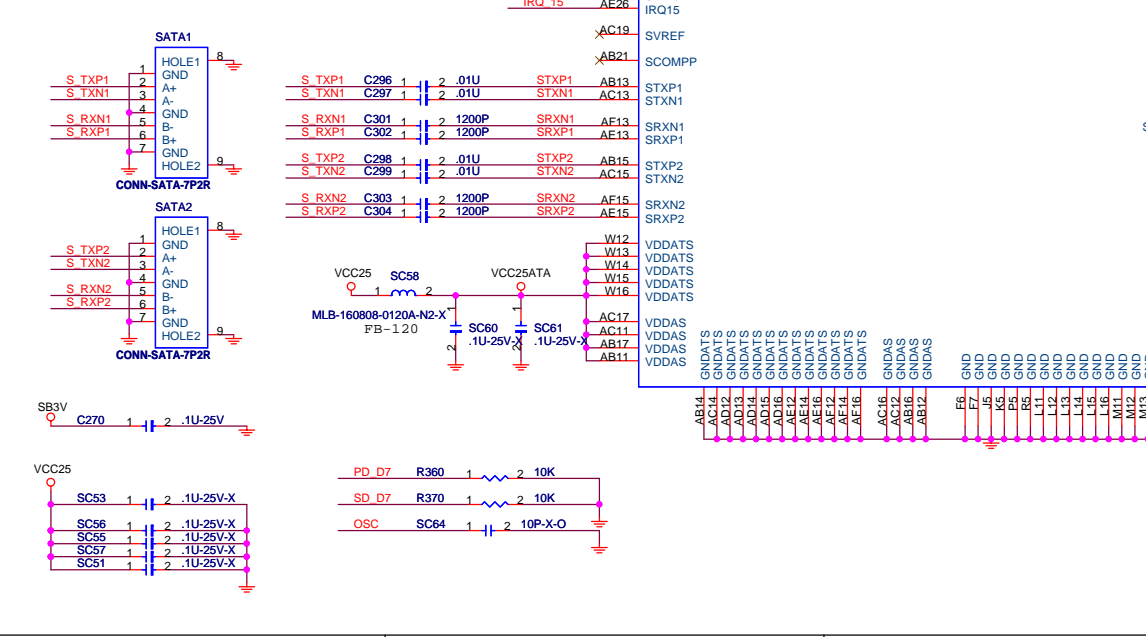
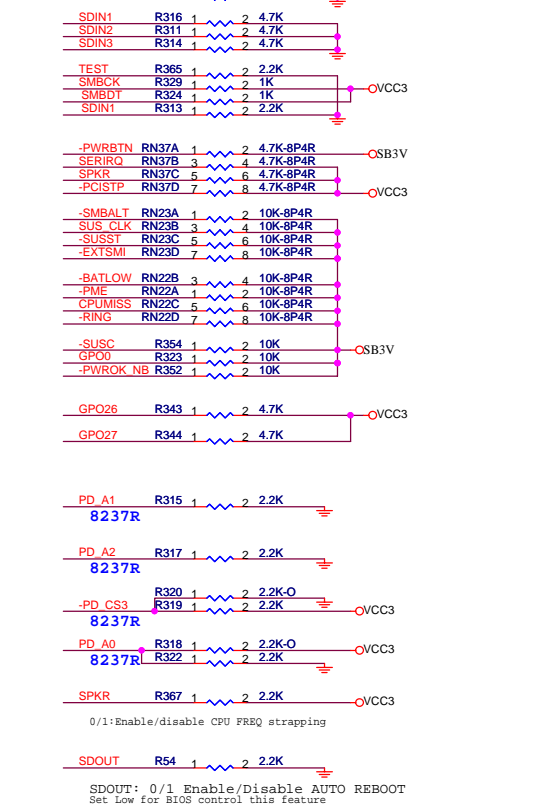
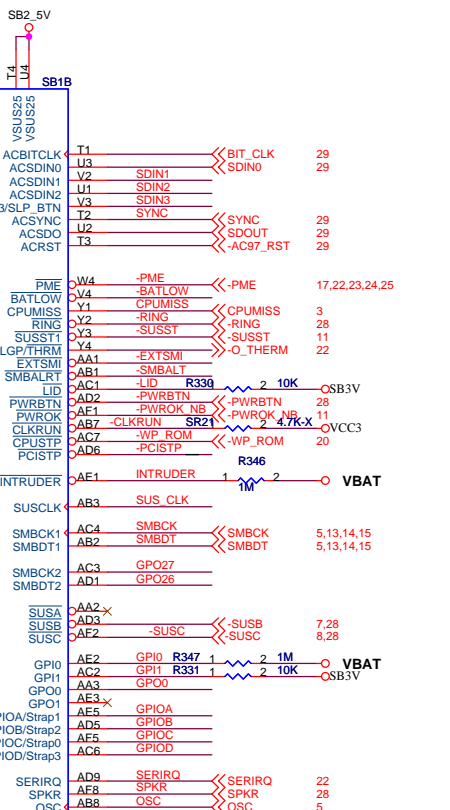
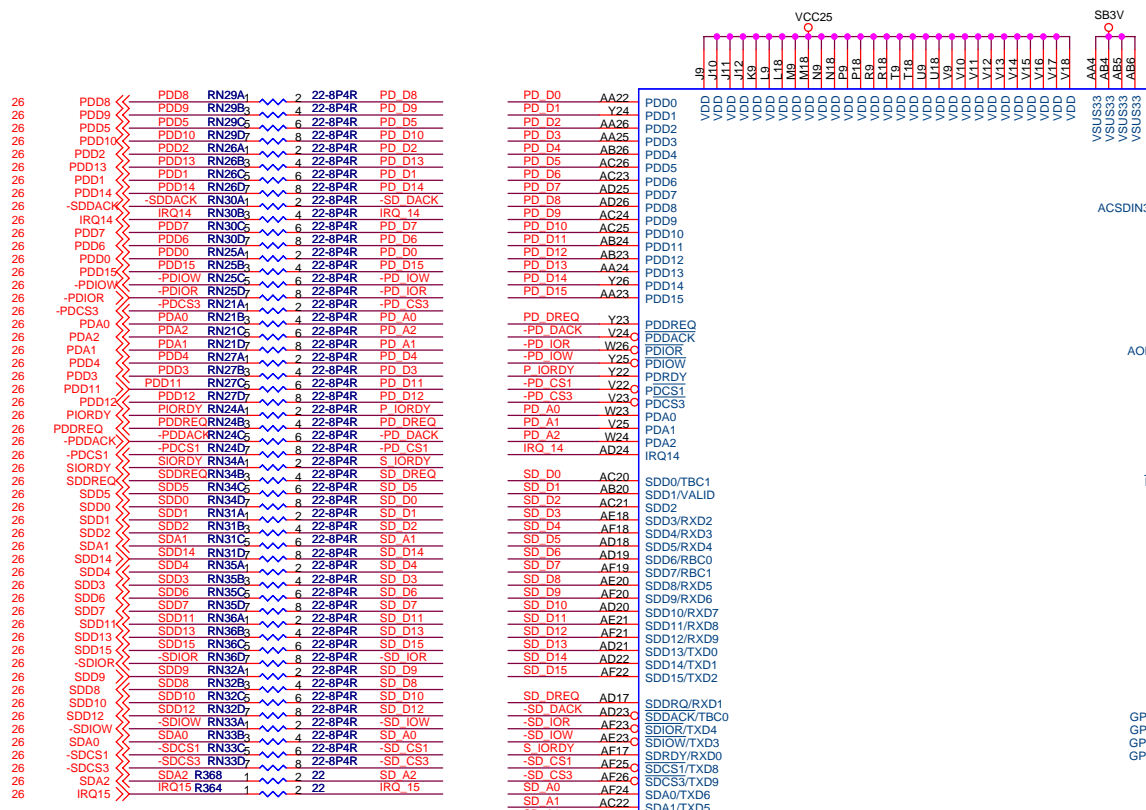




B to C(3/22)  
 AP note 307a  
 AGP 4X=1.0-1.1V  
 For boot random hang \*25\*

Elitegroup Computer Systems	
Title: AGP_SLOT	
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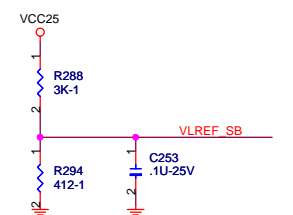
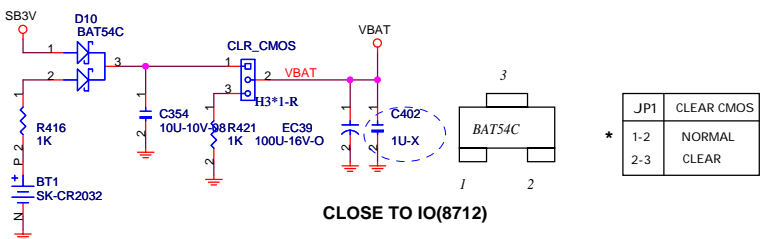
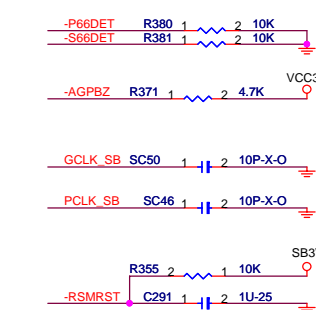
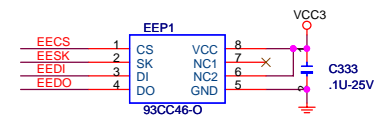
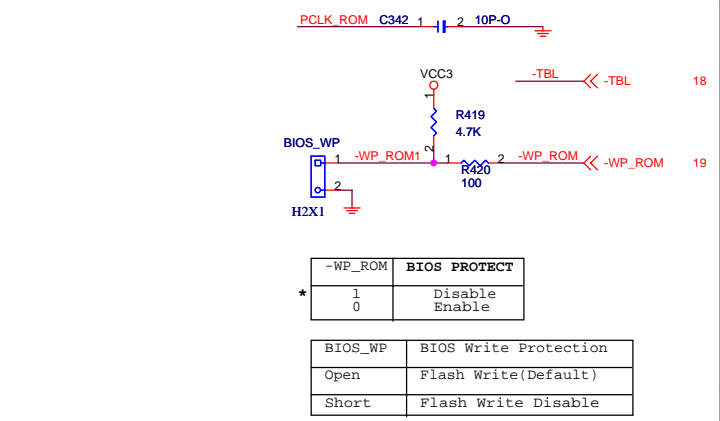
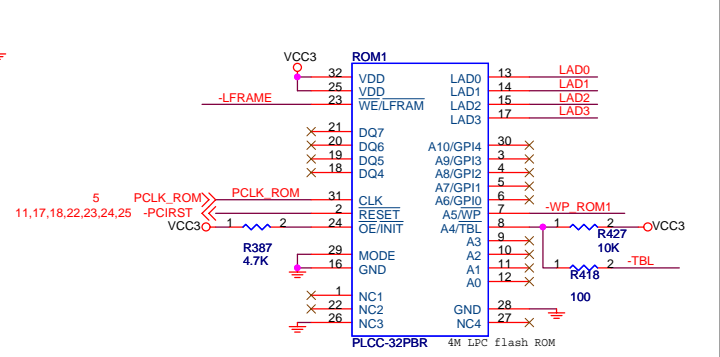
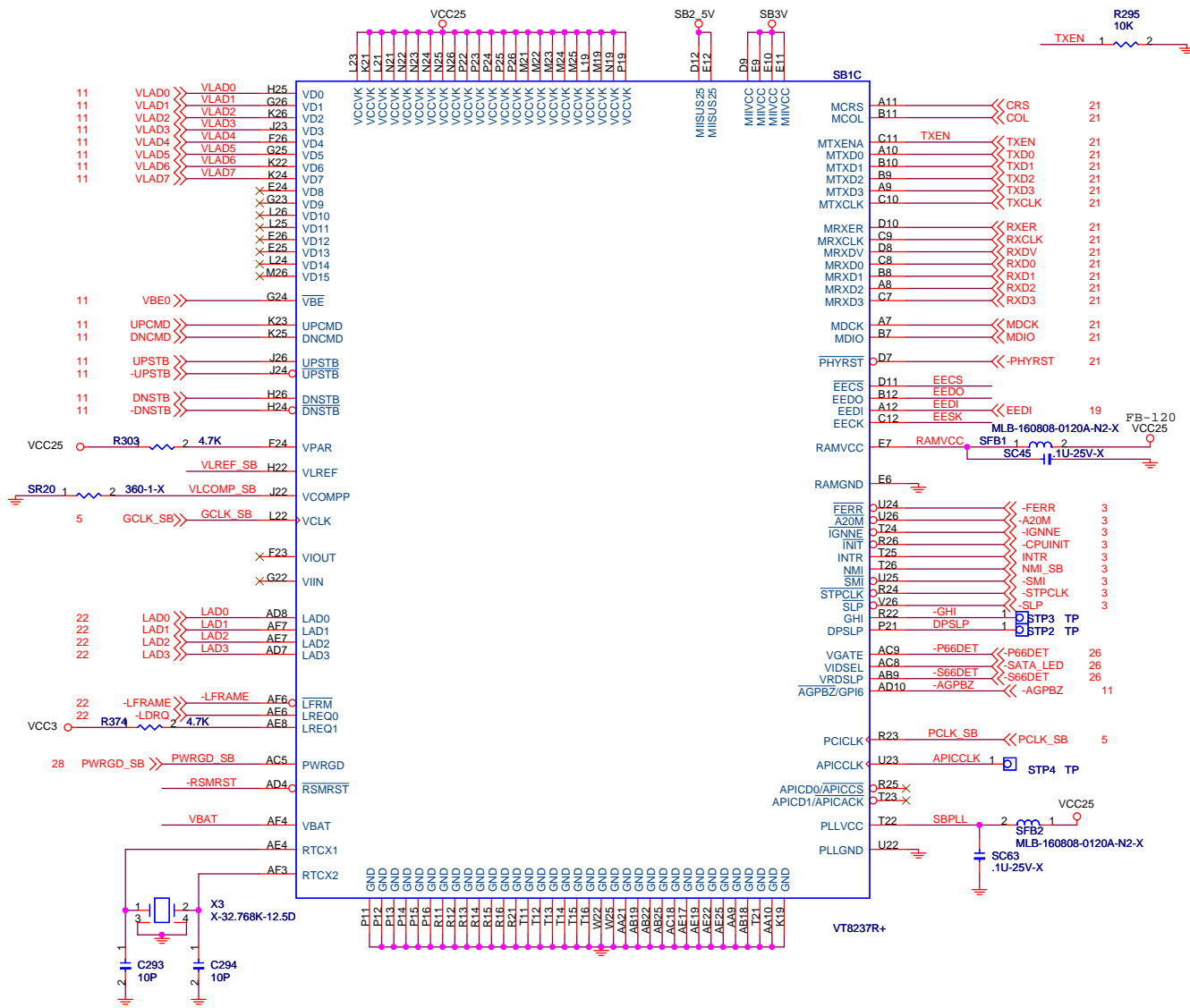
File: **SB (IDE\_GPIO\_AC-LICK)**

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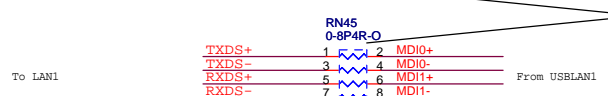
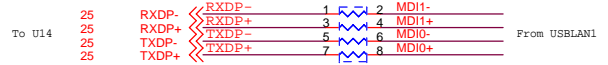
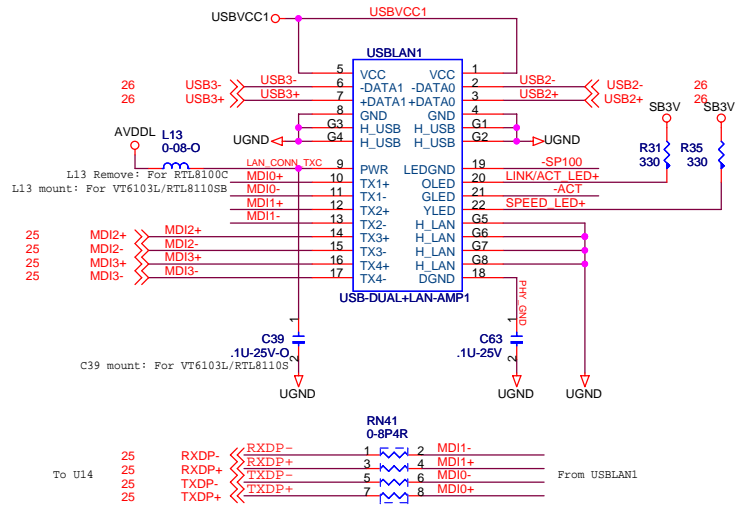
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* GPIOB I/OQ Depth	0 8 Level	* EEDI	Eliminate LAN EEPROM
1 1 Level		1	Enable
* GPIOD GTL pullup	0 Enable	* SPIOClock	Host Clock
1 Disable		0	200MHz
		1	Auto Mode
* PD CS3 WKCOMP for Vlink at 4X mode	0 Pull-down is 0.75V		
1 Pull-high is 0.9V			

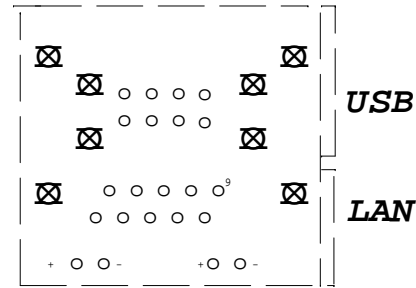
**8237R** : SYNC pull-up  
: PD\_CS1 pull-up  
: PD\_DACK pull-up



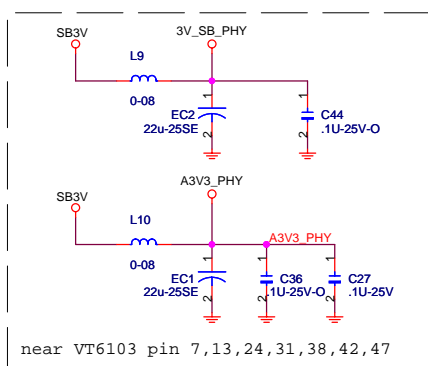
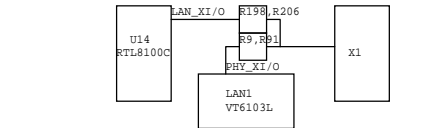
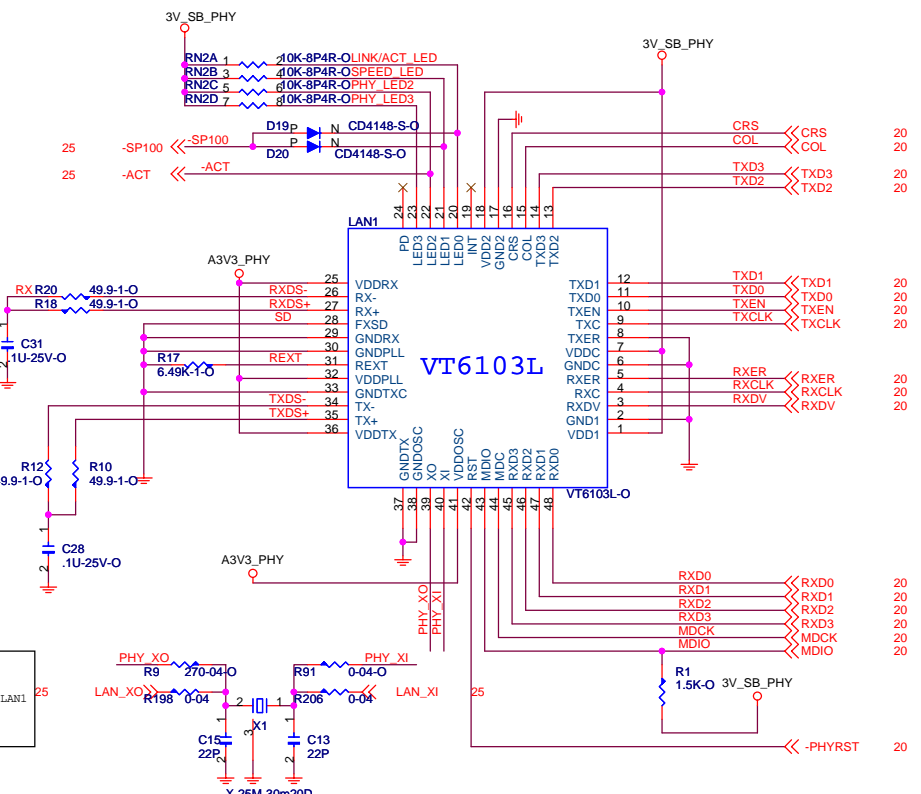
PT800CE: VLREF = 0.625  
 PM800/PT880/PM880: VLREF = 0.45  
 AP note 305: VLREF = 0.3



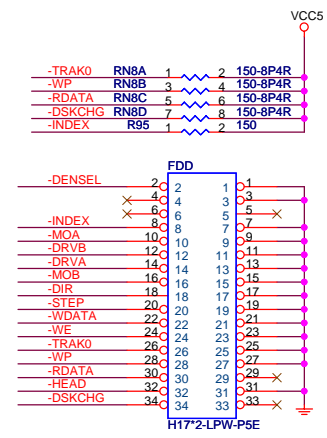
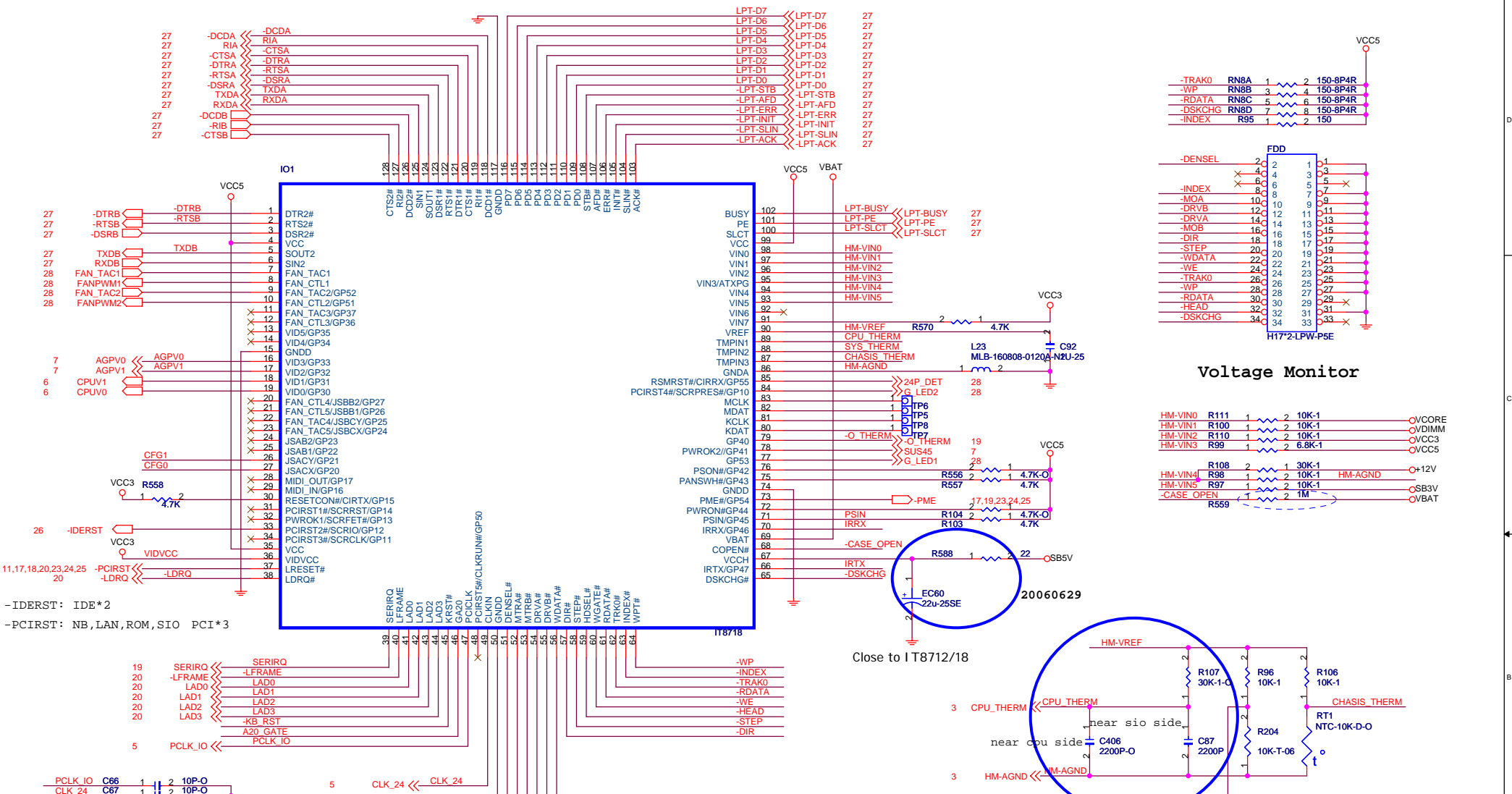
CONNECTOR Solder Side View



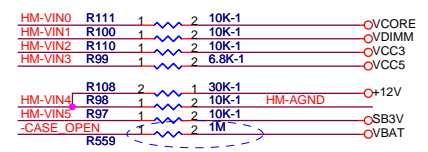
LNA CONN WITH TRSFORM  
LED L-Y / R-G  
**10-084-022627**  
CONN.USB DUAL PORT+LAN.22P  
90D.W/LED(LY-RG/O).10/100  
TRANS LJ-H51SU3-52.LANKOM.



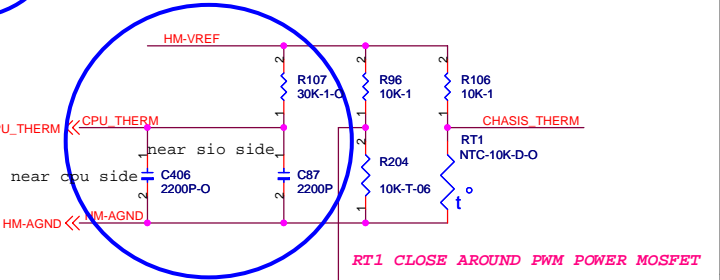
	LED0	LED1	LED2	LED3	
00	LINK/ACT	SPEED	DUPLEX	COL	
01	PWR/TXACT	LINK/RXACT	SPEED	DUPLEX	
10	SPEED100	SPEED10	ACT	DUPLEX	DEFAULT
11	PWR/TXACT	LINK/RXACT	SPEED	COL	



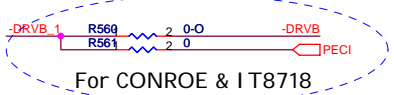
**Voltage Monitor**



Close to IT8712/18

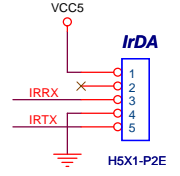
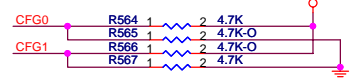
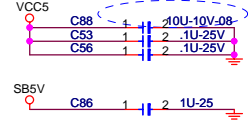


RT1 CLOSE AROUND PWM POWER MOSFET



CFG1	CFG0	Function description
1	1	W/S3 W/COM2
1	0	W/S3 W/O COM2
0	1	W/O S3 W/COM2
0	0	W/O S3 W/O COM2

CHANGE TO 10 uF, CLOSE TO IT8712/18



**ITE8712F/KX**

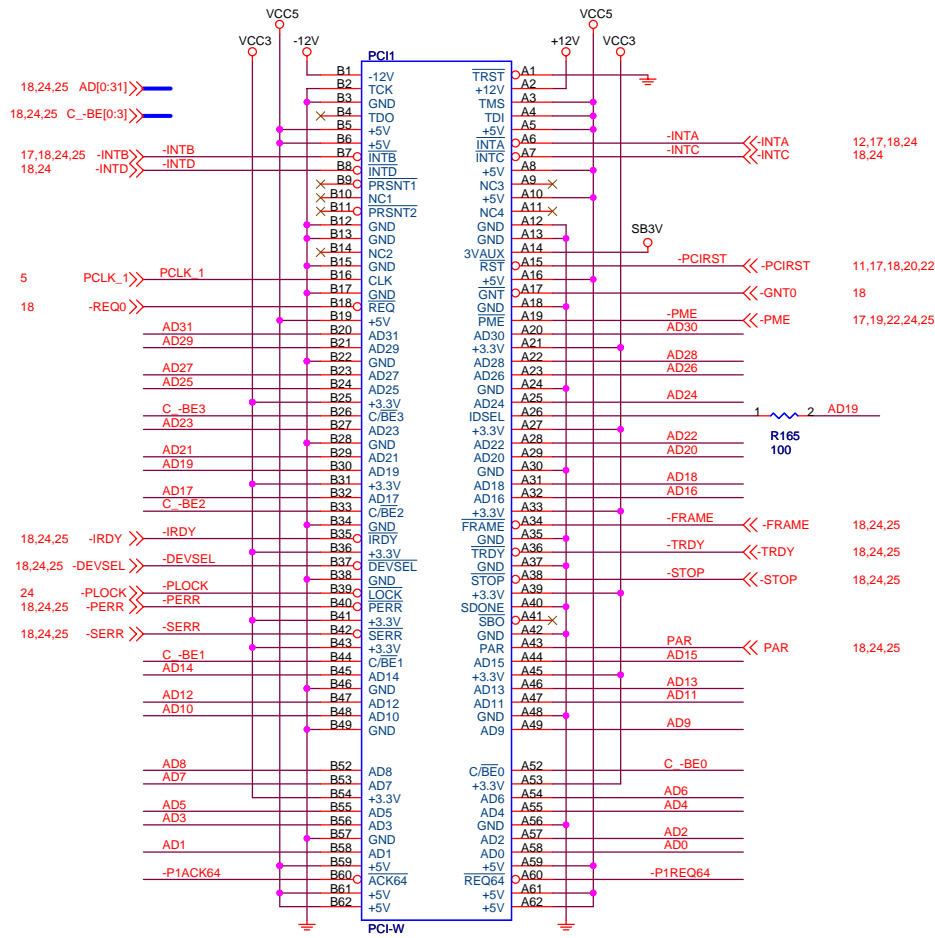
JP1	Flashseg1_EN(for SPI)	1:Disable
JP2	SerFlh_SO_SEL(S01/S02)	1:SEL FLH_SO2(don't care)
JP3	CHIP_SEL(for 2pcs ITE)	don't care(2 ITE,4 COMs)
JP4	BUF_SEL(OD/push pull)	1:PCIRST# O.D.
JP5	FAN_CTL_SEL	1:FAN full turn. 0:FAN mid turn.
JP6	VID_ISEL(CPU478/775)	Don't care.

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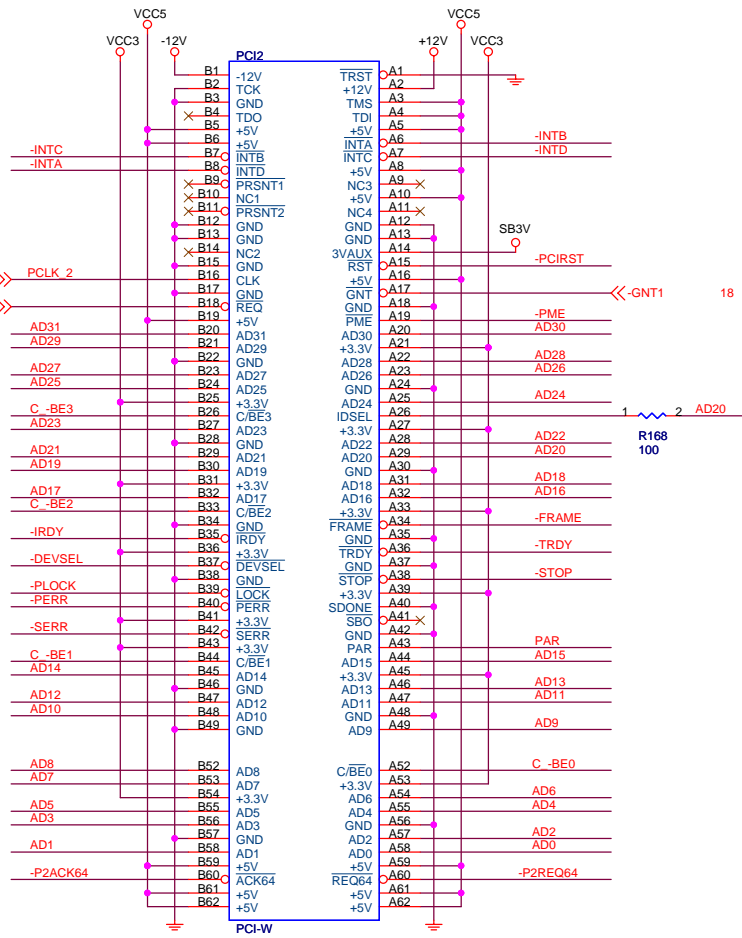
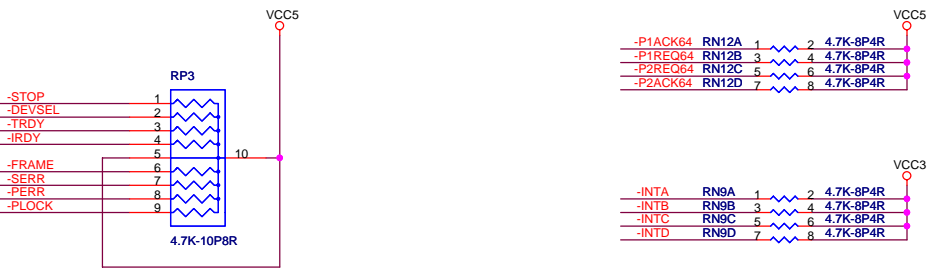
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Size: Custom Document Number: **P4M800PRO-M** Rev: **1.9**

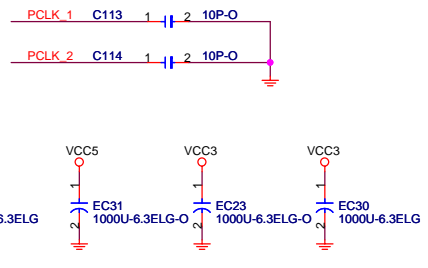
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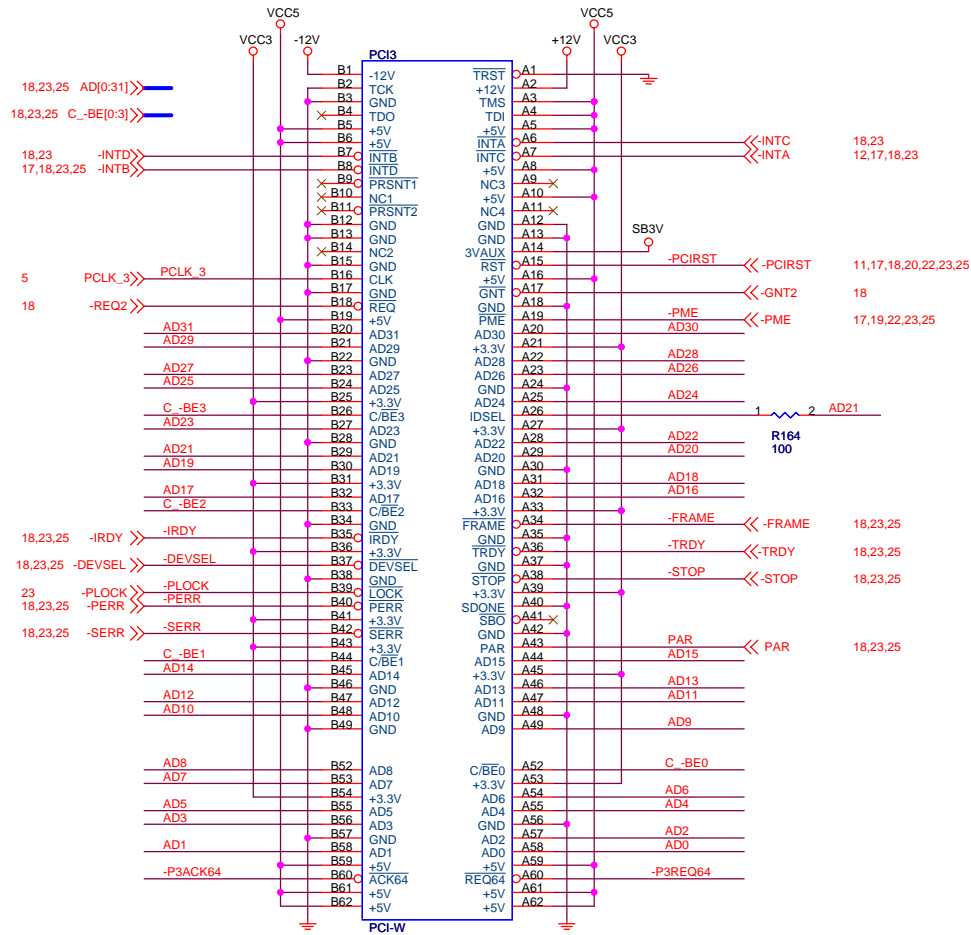


INT:A  
IDSEL:AD19

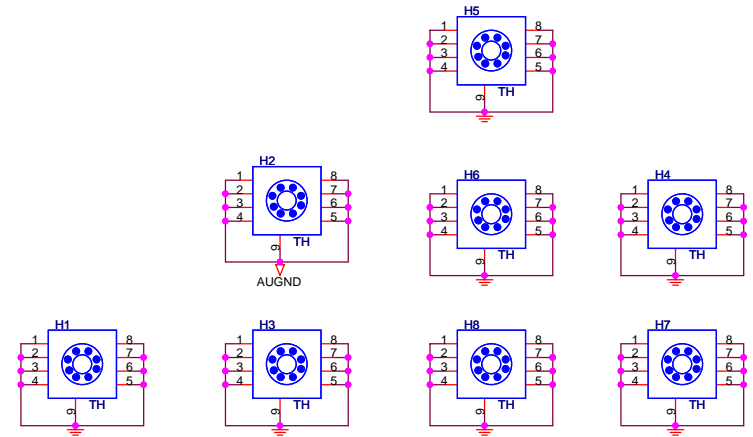
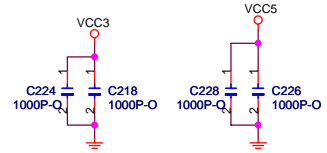
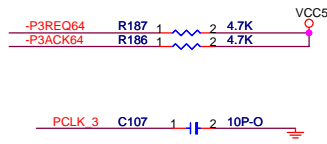


INT:B  
IDSEL:AD20



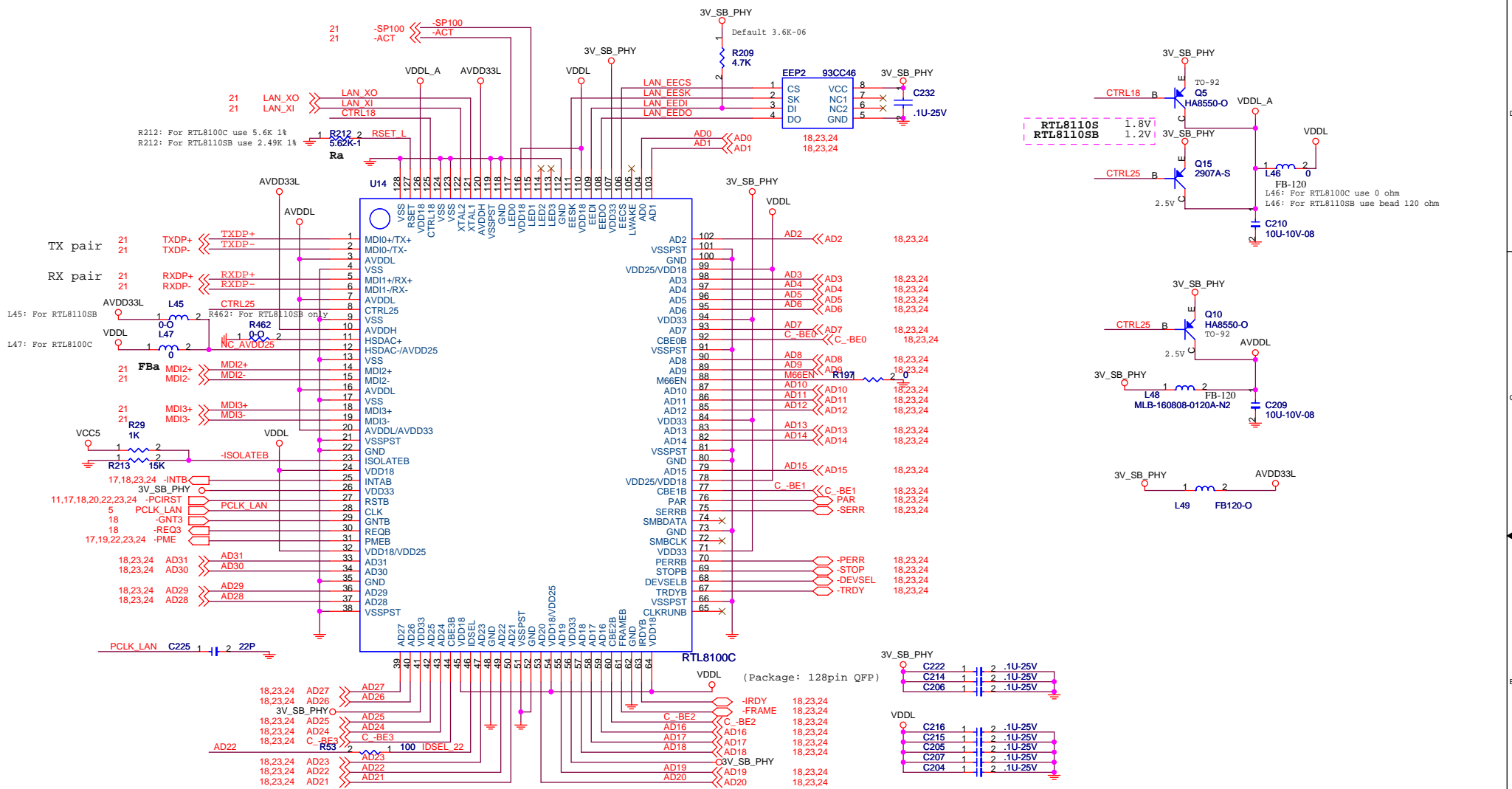


INT:C  
IDSEL:AD21



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R212: For RTL8100C use 5.6K 1%  
 R212: For RTL8110SB use 2.49K 1%

L45: For RTL8110SB  
 L47: For RTL8100C

L46: For RTL8100C use 0 ohm  
 L46: For RTL8110SB use bead 120 ohm

	VCC3_DUAL	V_DAC	pin12	VDDL	VDDL_A	AVDDL	AVDD33L
8100C	3.3V	NC	2.5VA	2.5V	2.5VA	3.3VA	NC
8110S	3.3V	2.5VA	NC	1.8V 500mA	1.8VA	2.5VA 650mA	3.3VA
* 8110SB	3.3V	2.5VA	3.3VA	<b>1.2V</b>	<b>1.2VA</b>	2.5VA	3.3VA

	U14	R212	L47	L45	L13	Q10	Q15	Q5	L46	L48	L49	R462	R463-R466	C359, C360	Connector+Tran
* 8100C	8100C	5.6K	0	NC	NC	X	V	X	V	V	X	X	X	X	10-084-022623
8110S	8110S	2.49K	NC	NC	NC	V	V	V	V	X	V	X	X	V	10-084-022624
8110SB	8110SB	2.49K	NC	0	0	V	X	V	V	X	V	V	V	V	10-084-022624

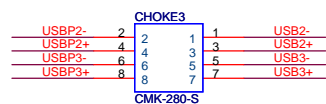
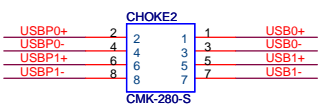
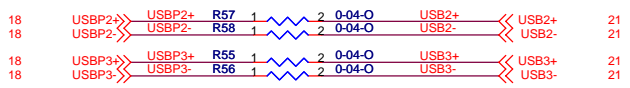
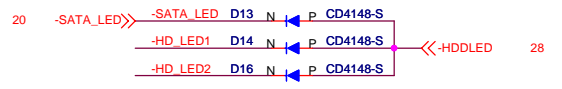
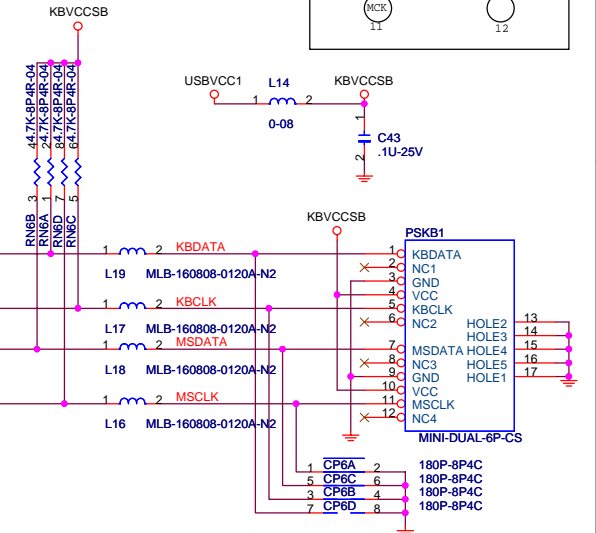
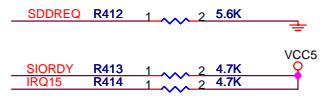
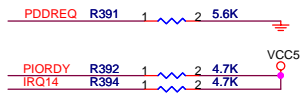
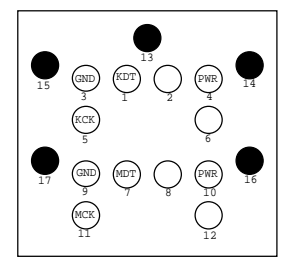
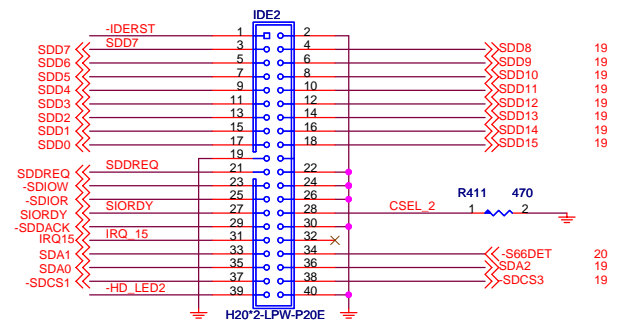
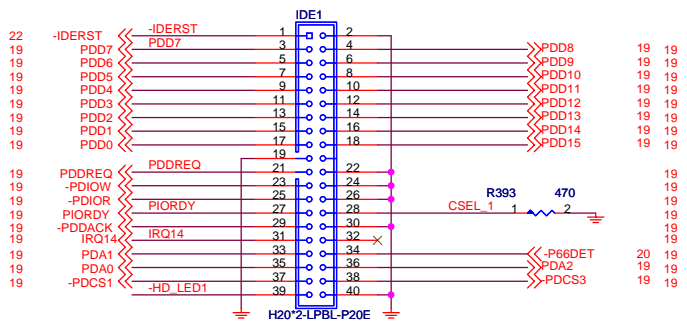
C8, C16, C359, C360:  
 For RTL8110SB use  
 0.01uF

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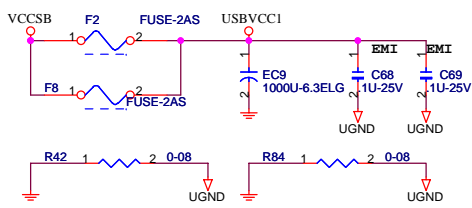
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Size: Custom Document Number: P4M800PRO-M Rev: 2.0

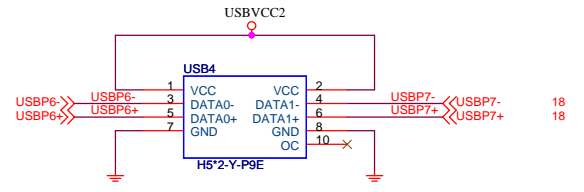
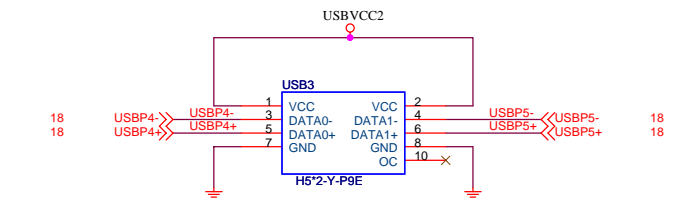
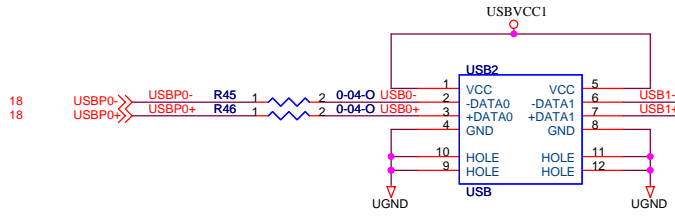
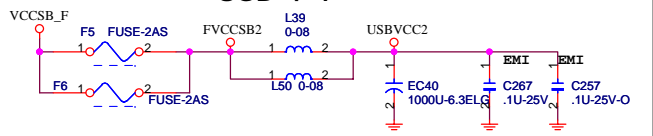
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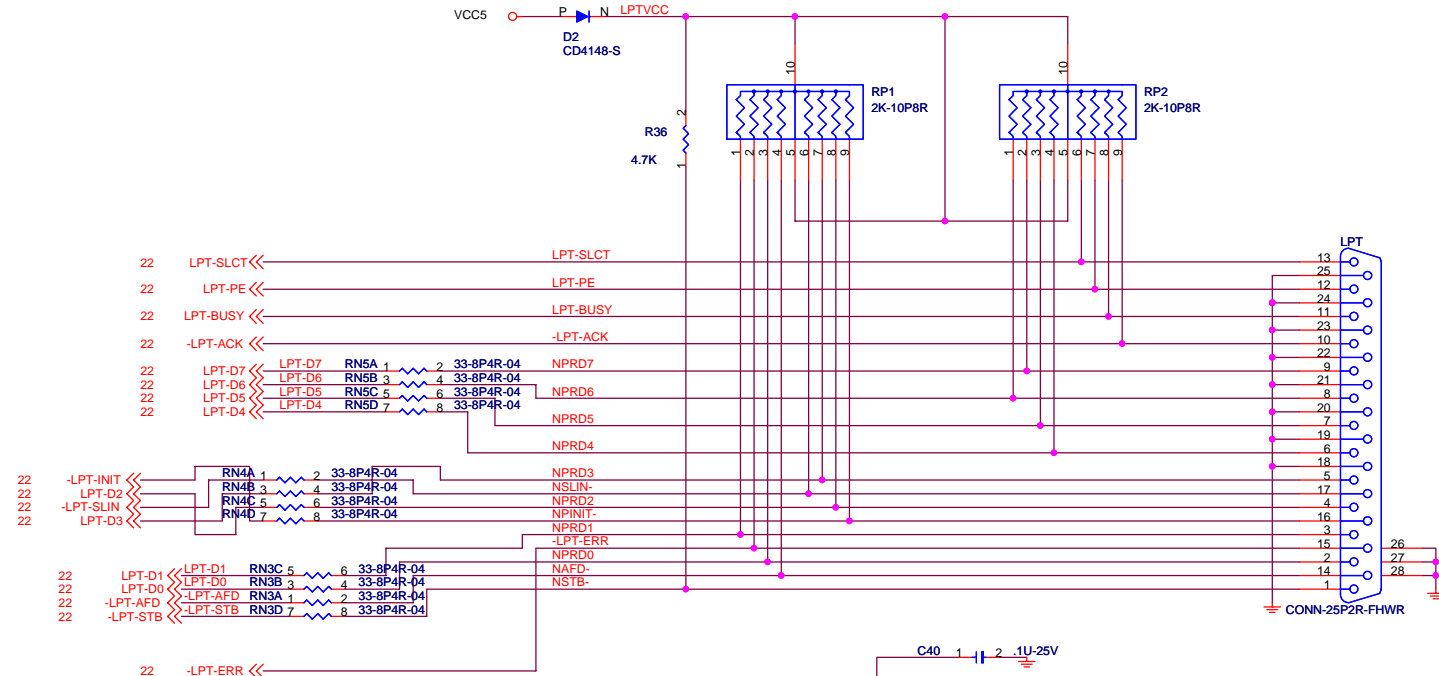
**USB 0-3**



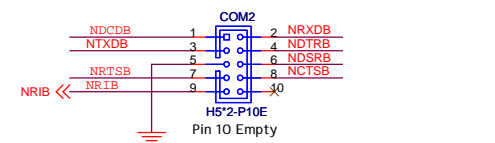
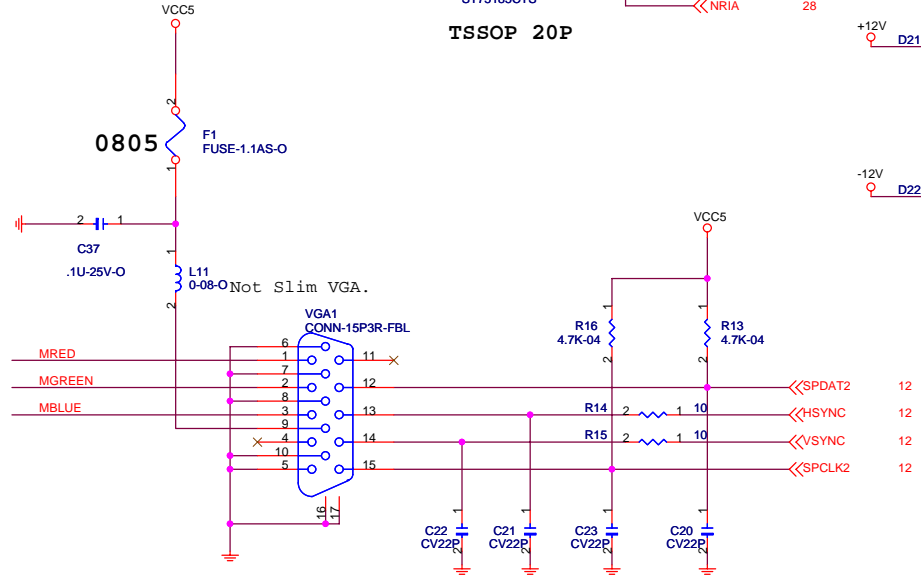
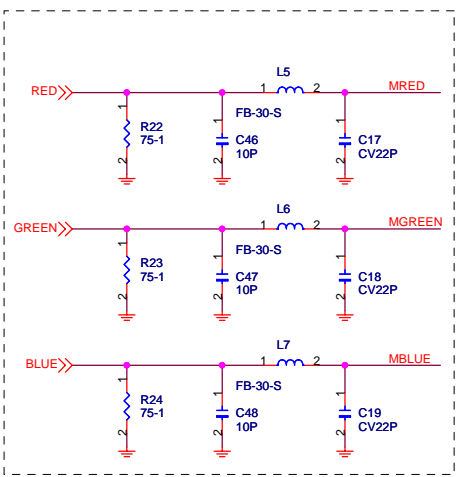
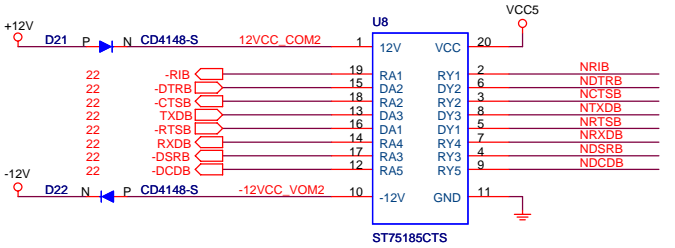
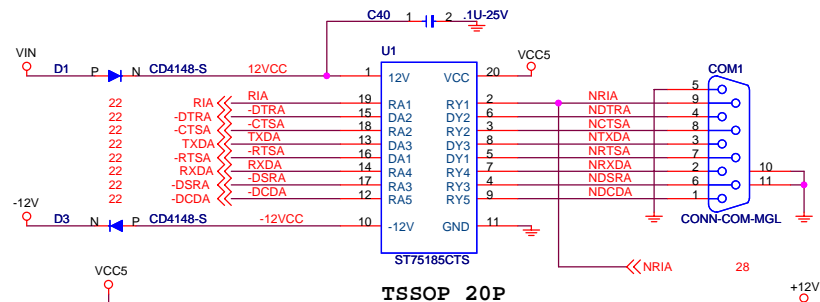
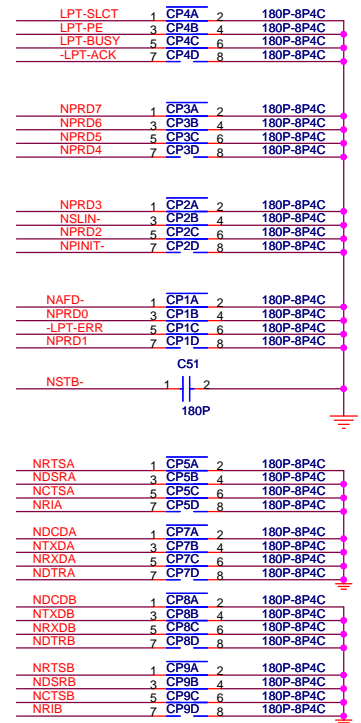
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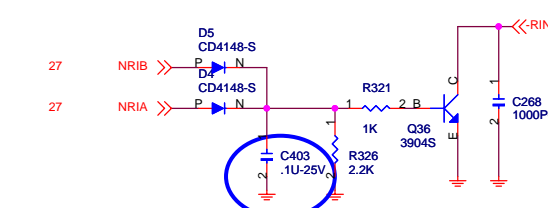
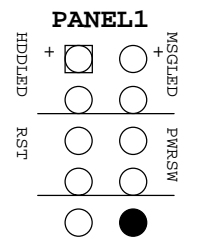
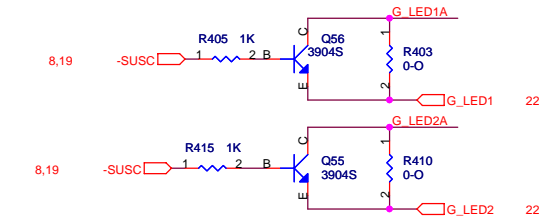
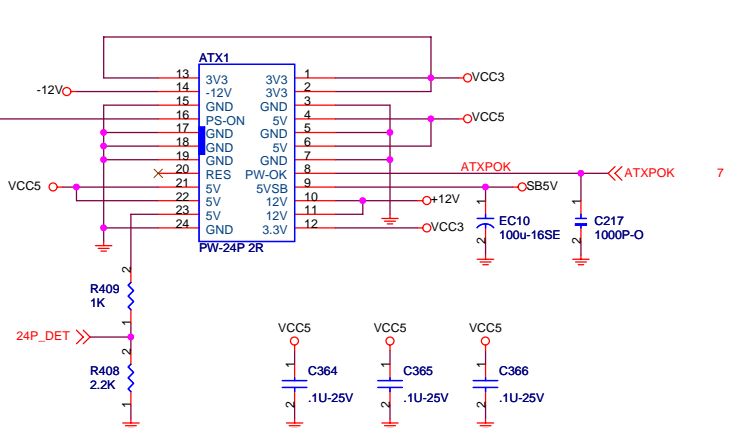
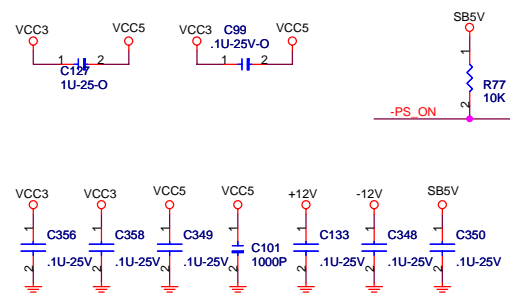
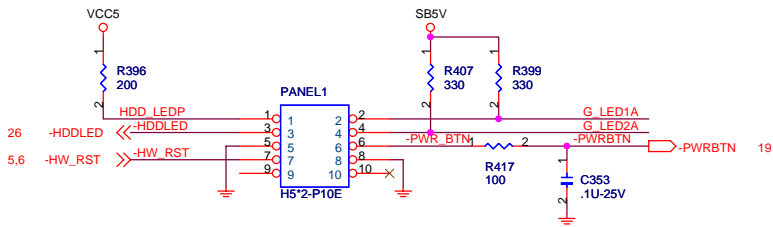


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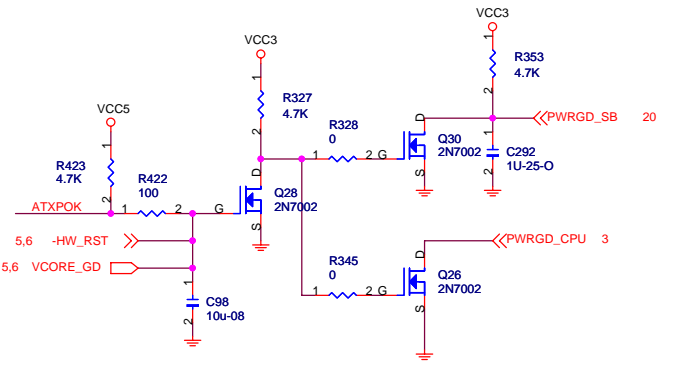
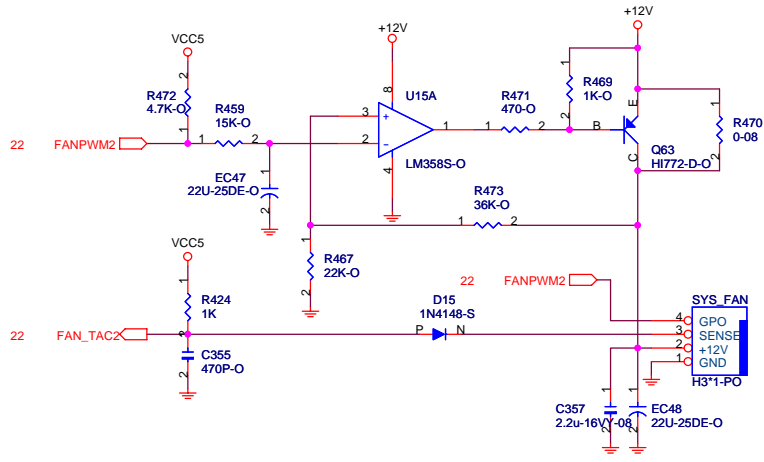
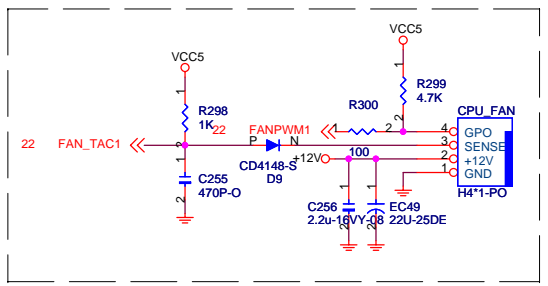
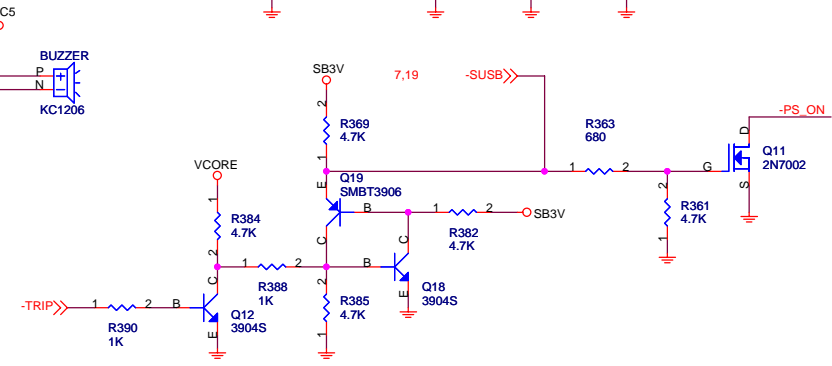
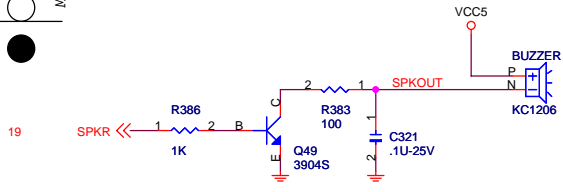
### CP1, CP2, CP3, CP4





SUSST1#	SUSA#	SUSB#	SUSC#	MODE
0	0	0	0	Mechanical off
1	0	0	0	S4/S5
1	0	0	1	S3
1	0	1	1	S1
1	0	1	1	S0 (ON)

	S0	S1	S3	S4,S5
PANEL1(4,2)	Green	G-blinking	Y-blinking	Dark
LPANEL1(3,5,7)	Green	G-blinking	G-blinking yellow	Dark
LSJ1(1,2)	Dark	Dark Blinking	Light	Dark
SJ1(1,3)(2,3)	Light		Blinking	Dark
GLE1	HIGH	HIGH	LOW	HIGH
GLE2	LOW	SWITCH	SWITCH	HIGH



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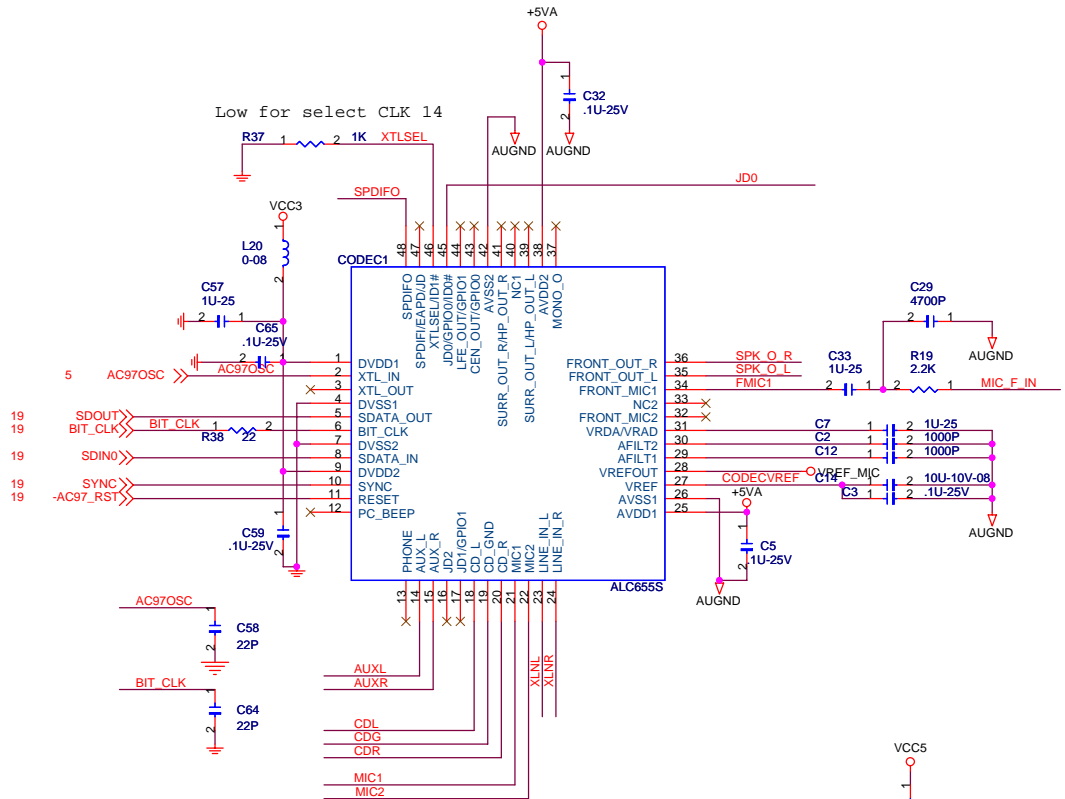
Title: FRONT\_PANEL\_FAN

Size: Custom Document Number: P4M800PRO-M

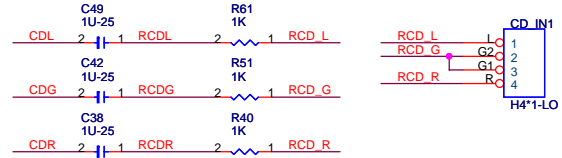
Date: Thursday, June 29, 2006

Sheet: 28 of 29

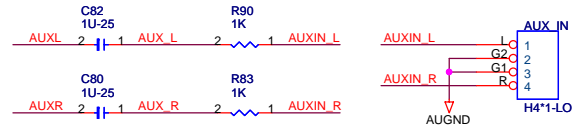
Rev: 1.9



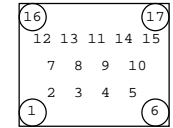
**CD-IN**



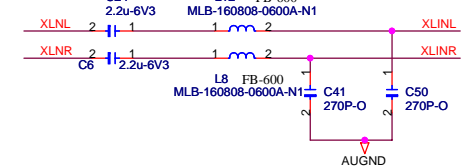
**AUX-IN**



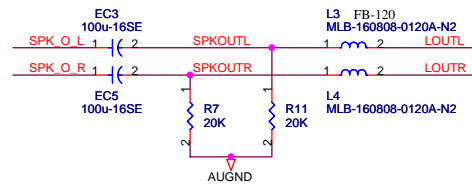
Top View



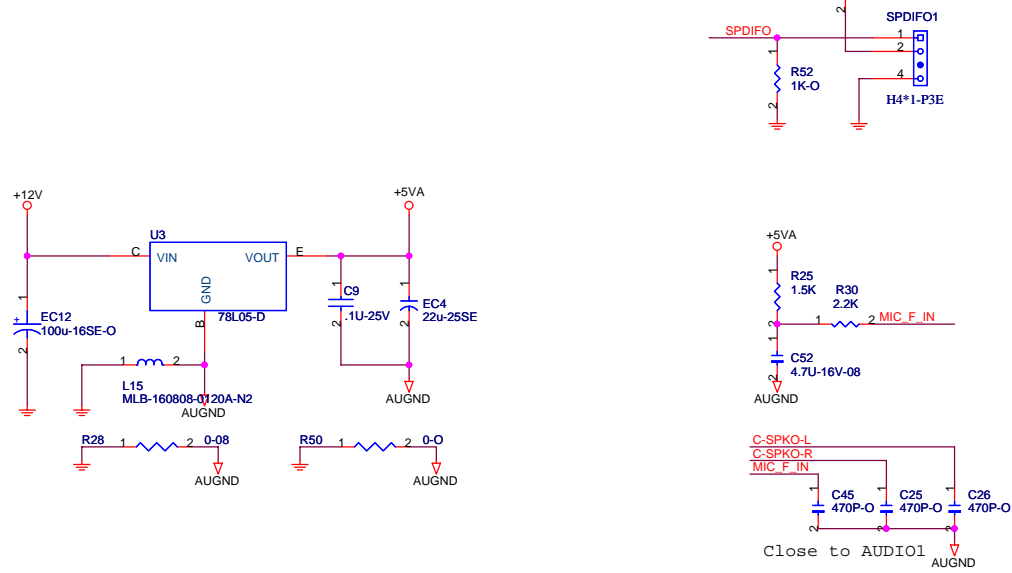
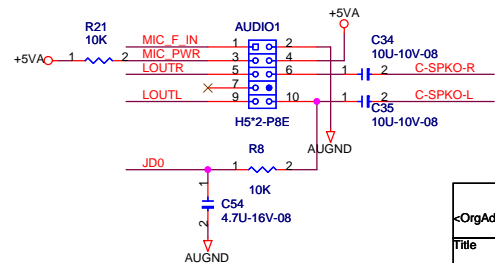
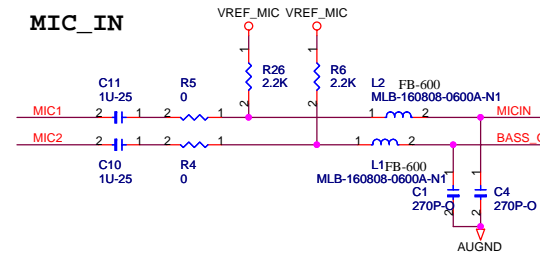
**LINE\_IN**



**LINE\_OUT**



**MIC\_IN**



<b>Elitegroup Computer Systems</b>	
Title: <b>AUDIO</b>	
Size: Custom	Document Number: <b>P4M800PRO-M</b>
Date: Thursday, June 29, 2006	Rev: <b>2.0</b>
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