

# Compal Confidential

## PAWGC/D Schematics Document

**AMD APU Ontario-FT1 + FCH Hudson-M1 + GPU Roberson XT**

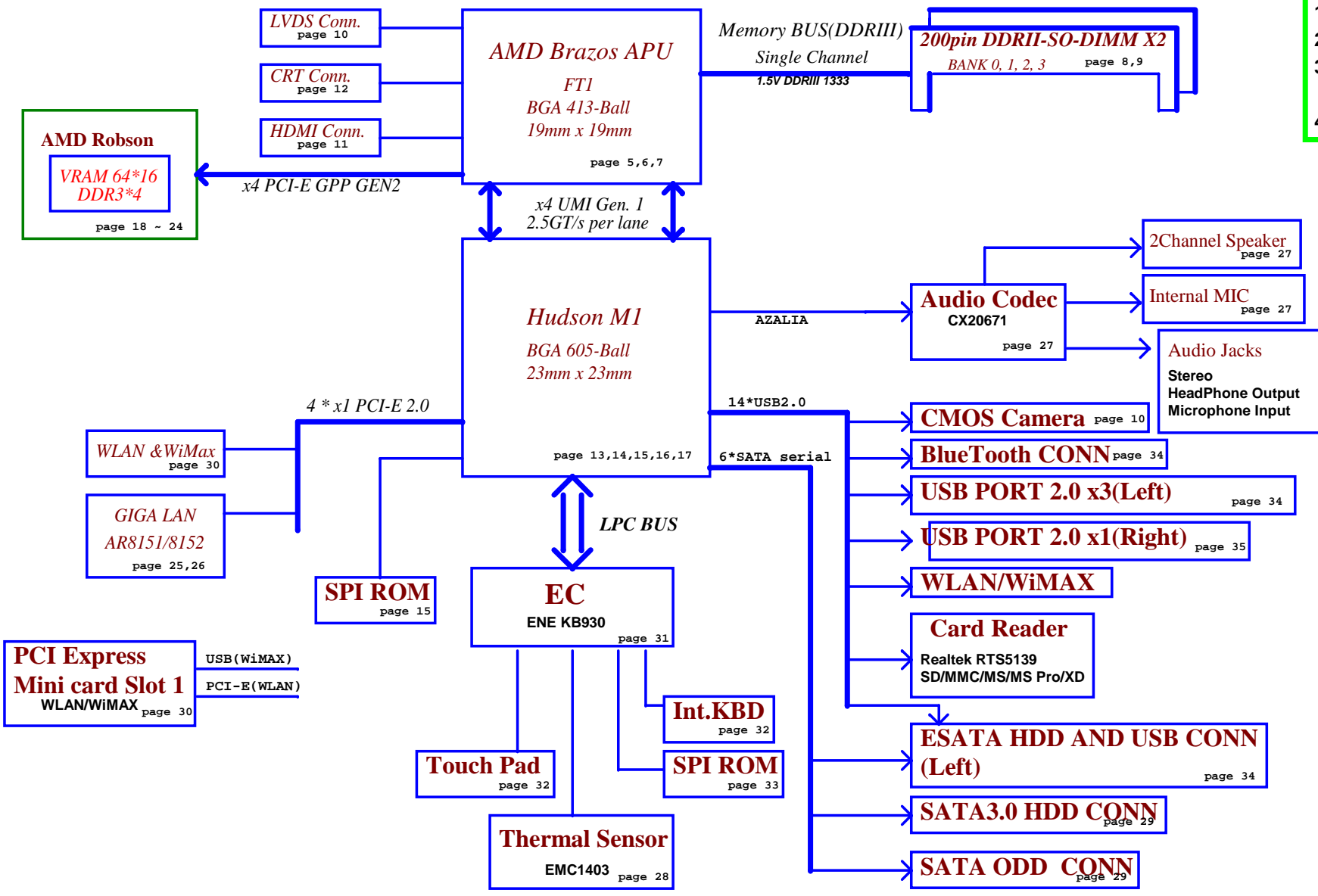
**2010-11-10**

**REV:1.0**

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**For PAWGC**  
 1. POWER BOARD  
 2. Card Reader BOARD

**For PAWGD**  
 1. POWER BOARD  
 2. Card reader BOARD  
 3. 4\*LED+SW(3pin)  
 +SW(4pin) BOARD  
 4. ODD BOARD



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## Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+APU_CORE	Core voltage for CPU (0.7-1.2V)	ON	OFF	OFF
+APU_CORE_NB	1.0V switched power rail	ON	OFF	OFF
+1.5V	1.5V power rail for CPU VDDIO and DDRIII	ON	ON	OFF
+0.75VS	0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.0VS	1.0V switched power rail for NB VDDC & VGA	ON	OFF	OFF
+1.1VS	1.1VS switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V_LAN	3.3V power rail for LAN	ON	ON(WOL)	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON
+1.1VALW	1.1V always on power rail	ON	ON	ON*

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

## EC SM Bus1 address

## EC SM Bus2 address

Device	Address	HEX	Device	Address	HEX
Smart Battery	0001-011xb	15H	EMC1412-2 (dGPU)	1111-100xb	F8H
			EMC1403-2(DDR,WLAN)	1001-101xb	9AH
			SB-TSI	1001-100xb	98H

## SM Bus Controller 0

(FCH\_SMB1 ~ FCH\_SMB4, SMB\_ALERT#)

Device	Address	HEX
APU SIC/SID (FCH_SMB3)		
H_THERMTRIP# (FCH_ALERT#)		

## SM Bus Controller 1

(FCH\_SMB0)

Device	Address	HEX
DDR DIMM1 (FCH_SMB0)	1001-000xb	90
DDR DIMM2 (FCH_SMB0)	1001-001xb	92
WLAN (FCH_SMB0)		

## FCH Hudson-M1 USB Port List

USB1.1	
Port0	NC
Port1	NC
USB2.0	
Port0	Left USB1
Port1	USB Camera
Port2	Left (Combo)
Port3	Left USB2
Port4	Right USB
Port5	BT
Port6	CardReader
Port7	Mini-PCIE
Port8	NC
Port9	NC
Port10	NC
Port11	NC
Port12	NC
Port13	NC

## Brazos PCIE Port List

APU	PCIE0	GPU PCIE x4
	PCIE1	
	PCIE2	
	PCIE3	
FCH	PCIE0	LAN
	PCIE1	WLAN
	PCIE2	NC
	PCIE3	NC

## FCH Hudson-M1 SATA Port List

SATA0	HDD
SATA1	ODD
SATA2	eSATA
SATA3	NC
SATA4	NC
SATA5	NC

## BOM Structure

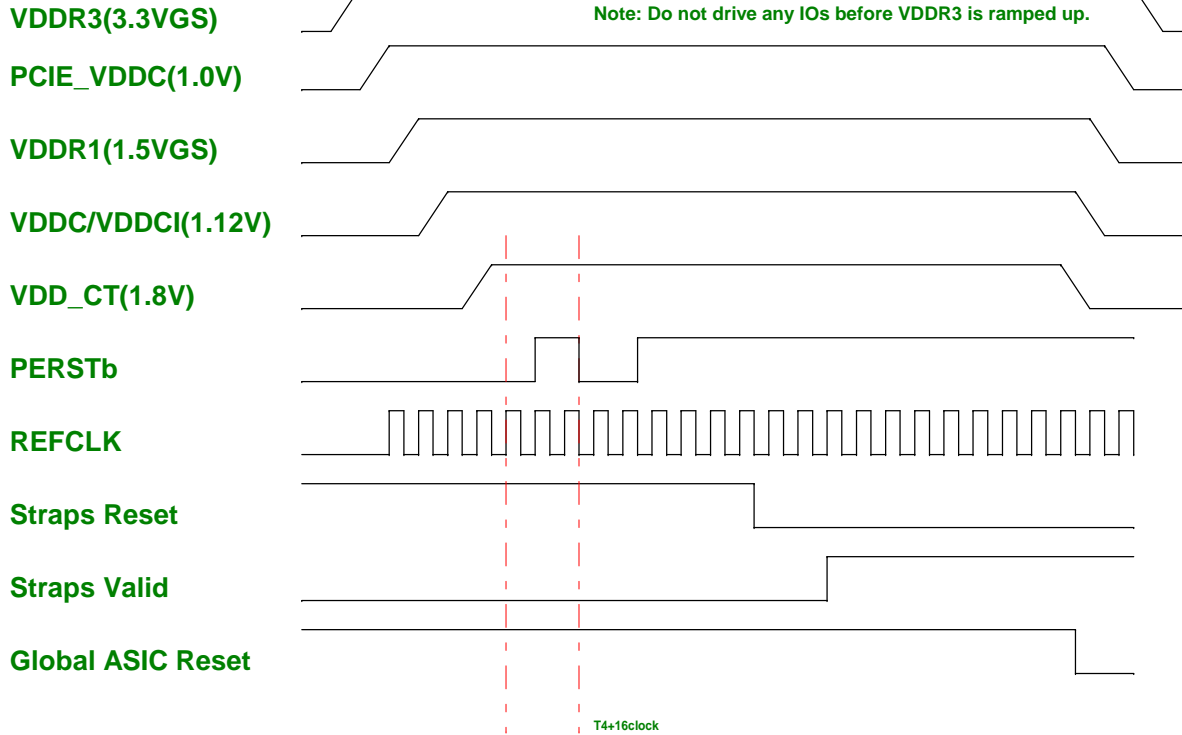
UMA@ : UMA only  
 PX@ : DIS muxluss  
     - PX3@ : PX3.0 only  
     - BACO@ : Baco only

GIGA@ : AR8151  
 8152@ : AR8152  
 CMOS@ : USB camera  
 HDMI@ : HDMI function  
 nonHDMI@ : w/o HDMI function  
 ESATA@ : eSATA function  
 BT@ : BT function  
 ME@ : ME components  
 X76@, H1G@, H512@, S1G@, S512@ : VRAM  
 45@ : 45 Level  
 HWM@ : hardware monitor function  
 nonHWM@ : w/o hardware monitor function

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## Power-Up/Down Sequence

- All the ASIC supplies must fully reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred.
- VDDR3 should ramp-up before or simultaneously with VDDC.
- For LVDS, DPx\_VDD10 should ramp-up before DPx\_VDD18 and the PCIe Reference clock should begin before DPx\_VDD18. For power-down, DPx\_VDD18 should ramp-down before DPx\_VDD10.
- The external pull-ups on the DDC/AUX signals (if applicable) should ramp-up before or after both VDDC and VDD\_CT have ramped up.
- VDDC and VDD\_CT should not ramp-up simultaneously. (e.g., VDDC should reach 90% before VDD\_CT starts to ramp-up (or vice versa).)



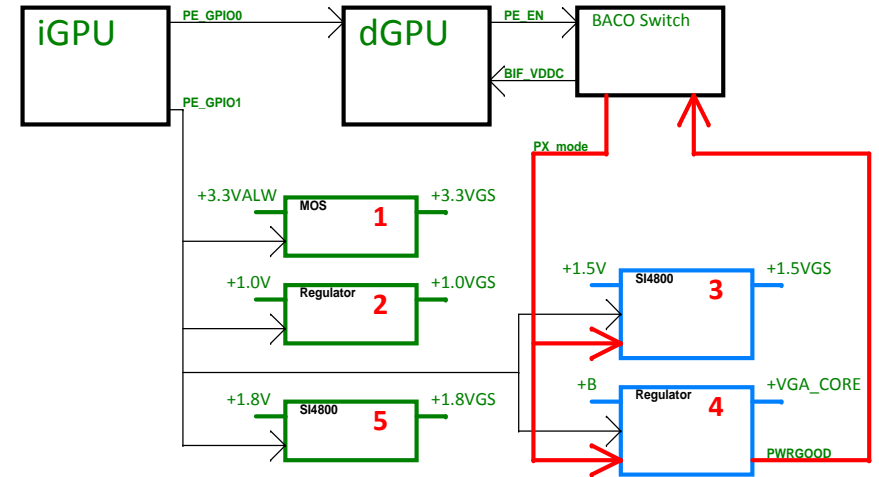
## Without BACO option :

PE\_GPIO0 : Low -> Reset dGPU ; High ->Normal operation  
 PE\_GPIO1 : Low -> dGPU Power OFF ; High -> dGPU Power ON

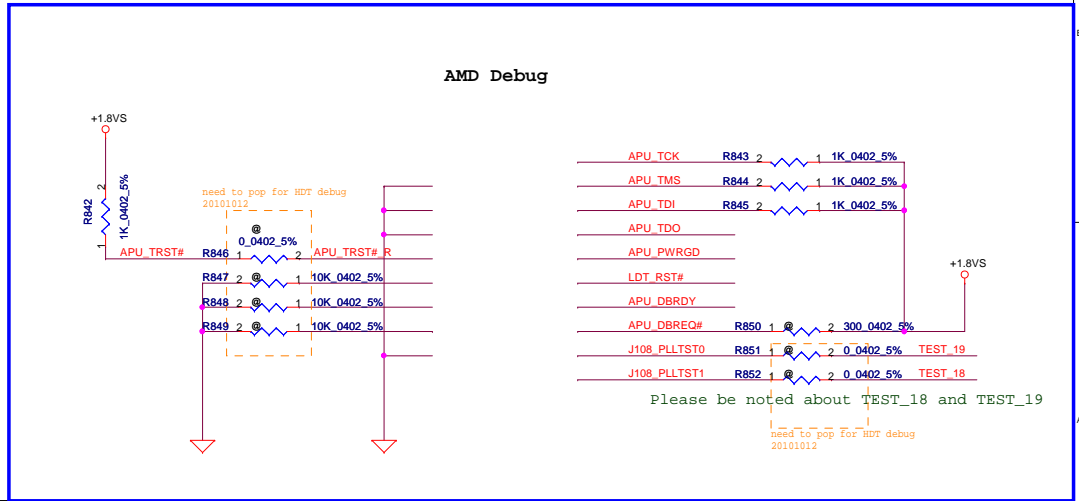
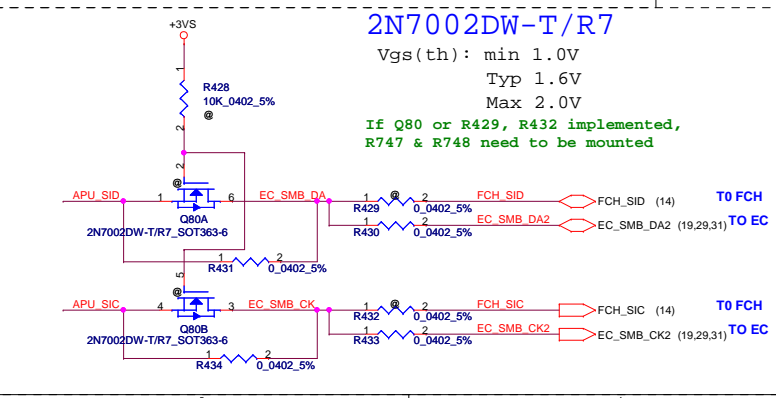
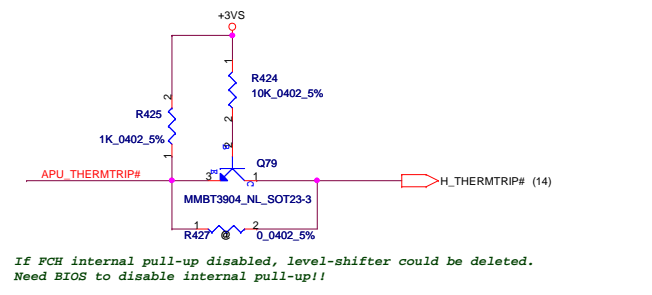
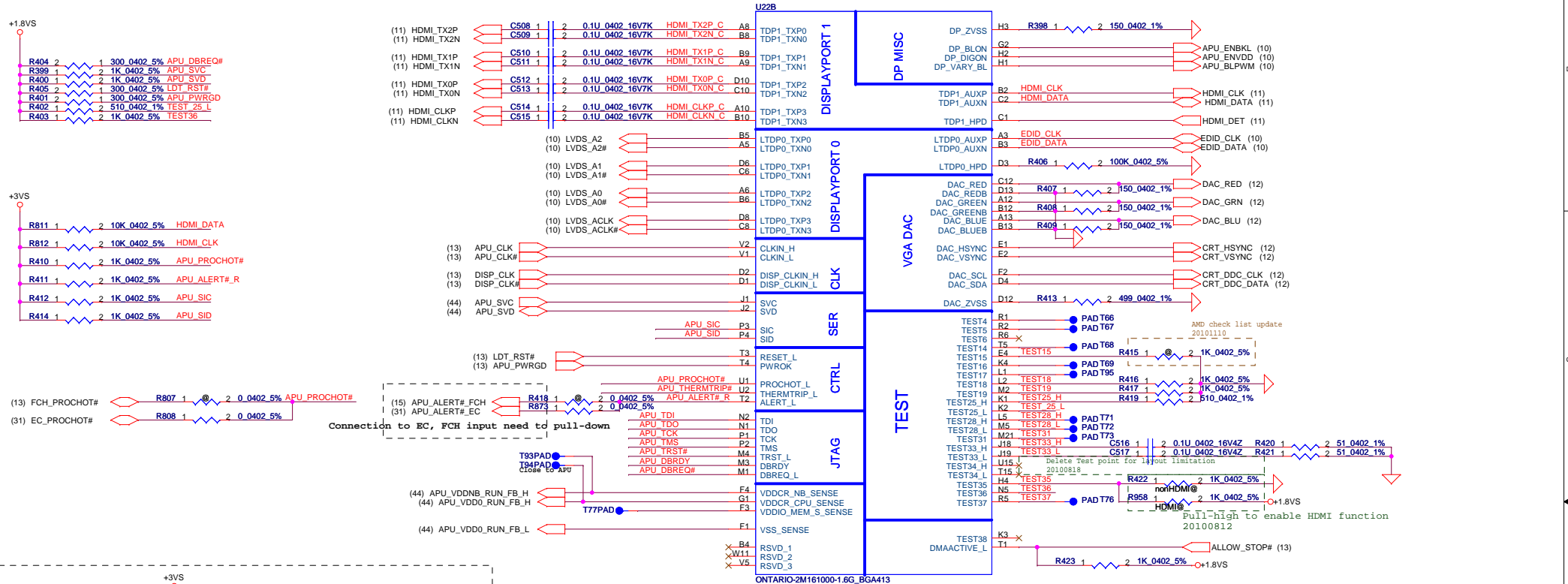
## BACO option :

PE\_GPIO0 : High ->Normal operation (dGPU is not reset on BACO mode)  
 PE\_GPIO1 : Low -> dGPU Power OFF ; High -> dGPU Power ON (always High)

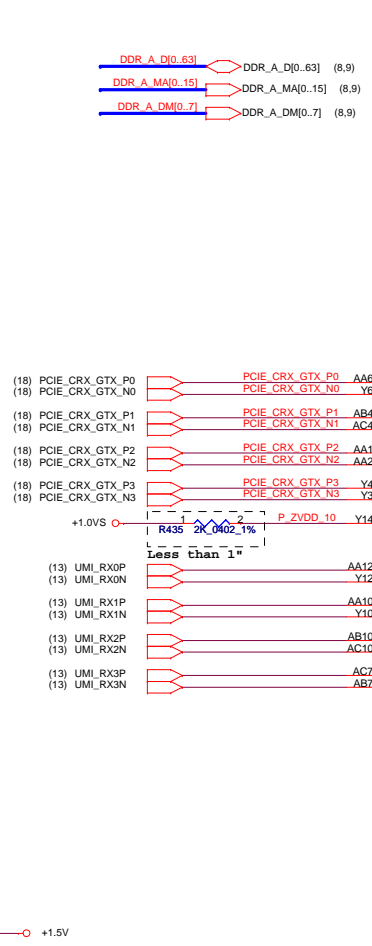
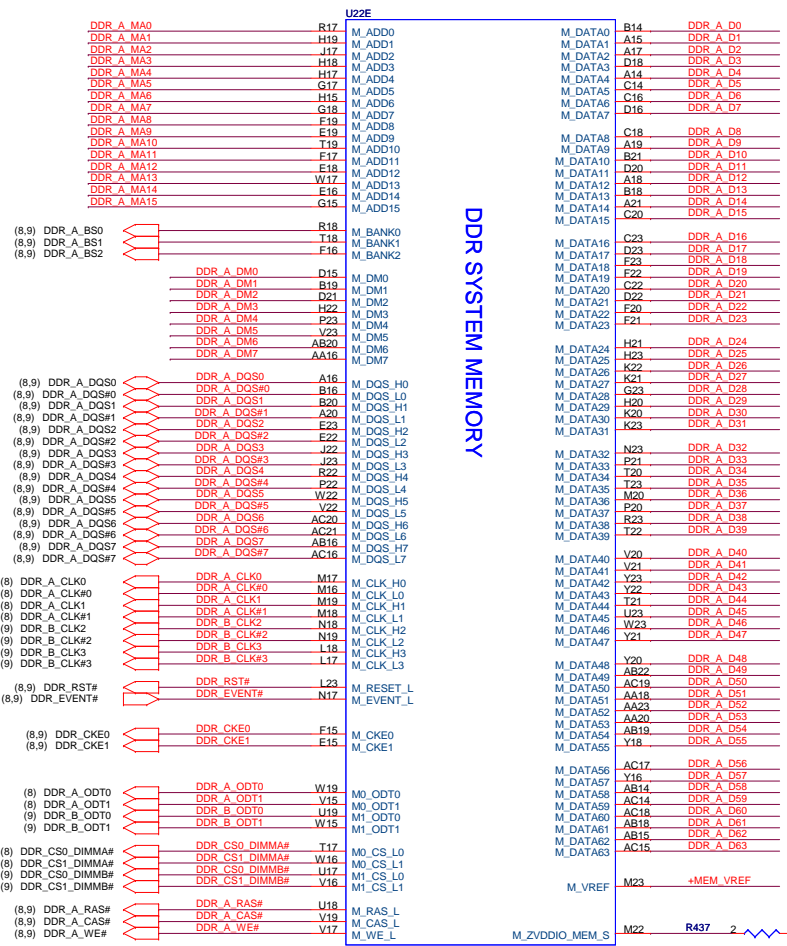
dGPU Power Pins	Voltage	PX 3.0	BACO Mode	Max current
PCIE_PVDD, PCIE_VDDR, TSVDD, VDDR4, VDD_CT, DPE_PVDD, DP[F:E]_VDD18, DP[D:A]_PVDD, DP[D:A]_VDD18, AVDD, VDD1DI, A2VDDQ, VDD2DI, DPLL_PVDD, MPV18, and SPV18	1.8V	OFF	ON	1679mA
DP[F:E]_VDD10, DP[D:A]_VDD10, DPLL_VDDC, and SPV10	1.0V	OFF	ON	575mA
PCIE_VDDC	1.0V	OFF	ON	2A
VDDR3 , and A2VDD	3.3V	OFF	ON	190mA
BIF_VDDC (current consumption = 55mA@1.0V, in BACO mode)	Same as VDDC	OFF	ON Same as PCIE_VDDC	70mA
VDDR1	1.5V	OFF	OFF	2.8A
VDDC/VDDCI	1.12V	OFF	OFF	12.9A



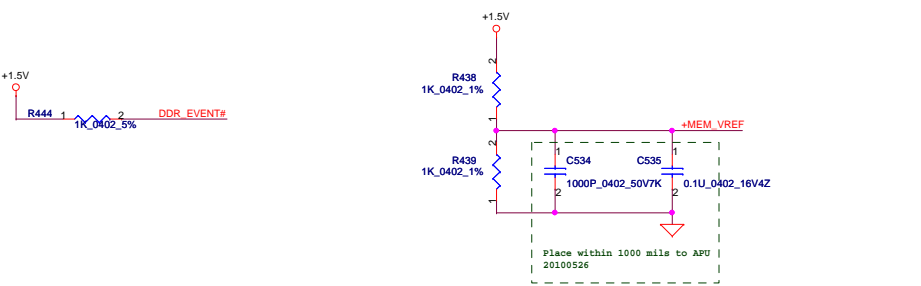
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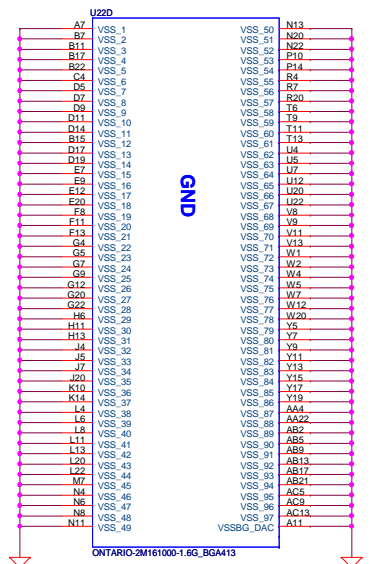
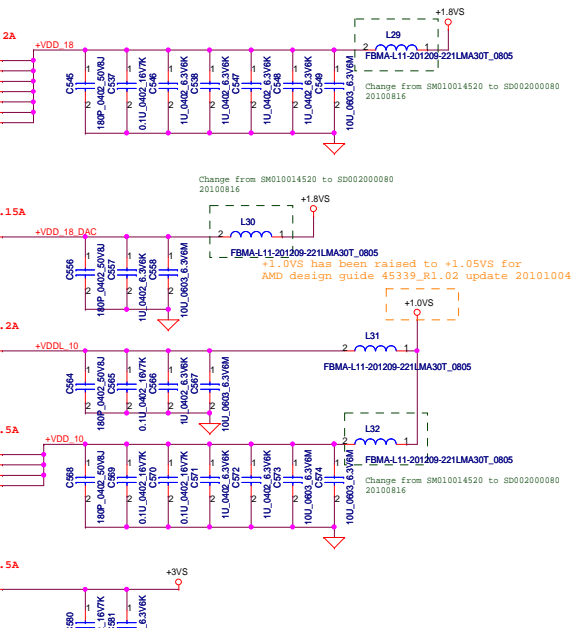
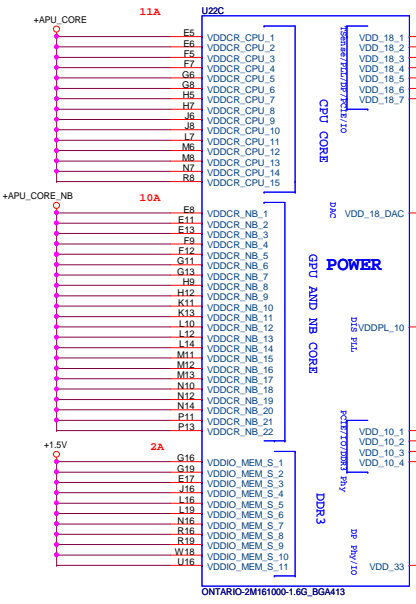
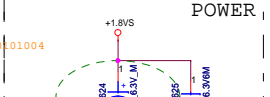
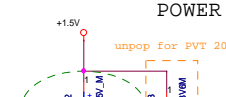
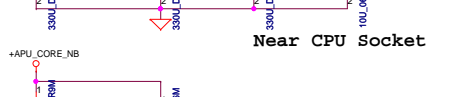
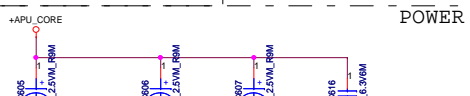
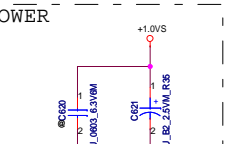
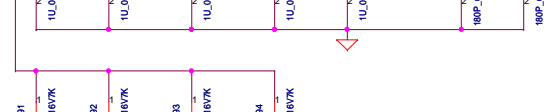
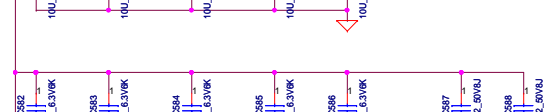
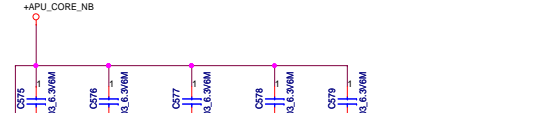
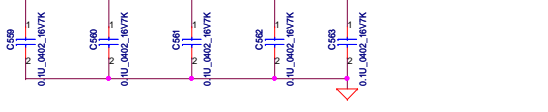
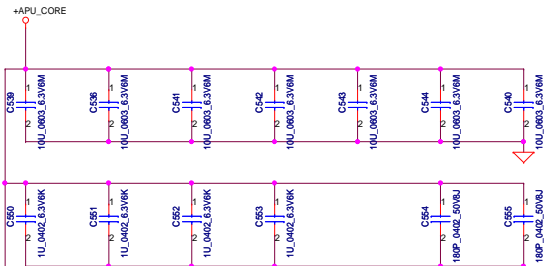


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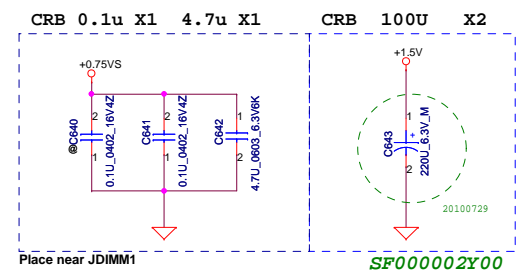
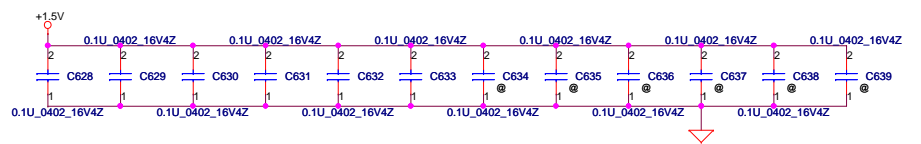
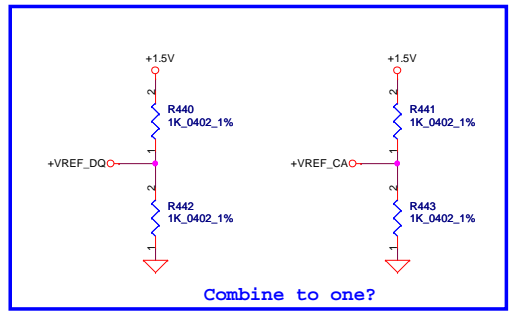
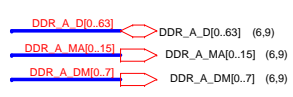
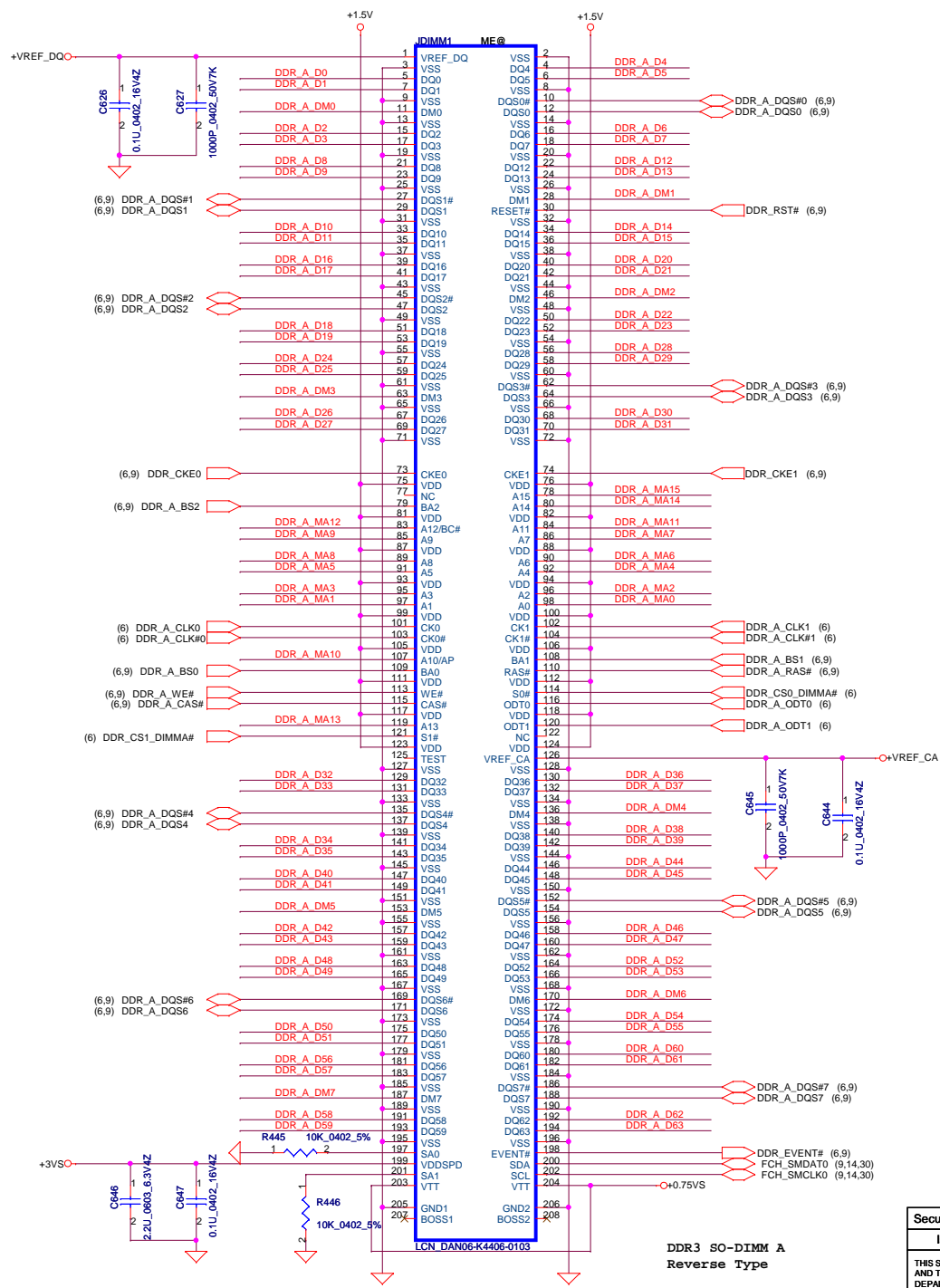
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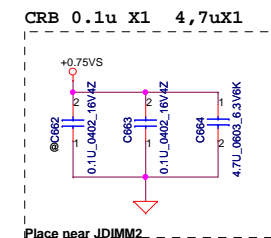
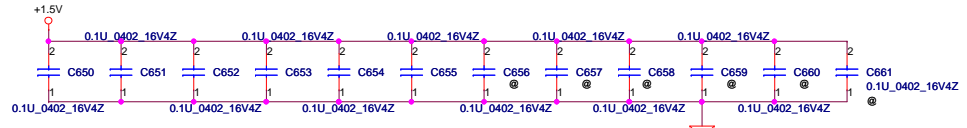
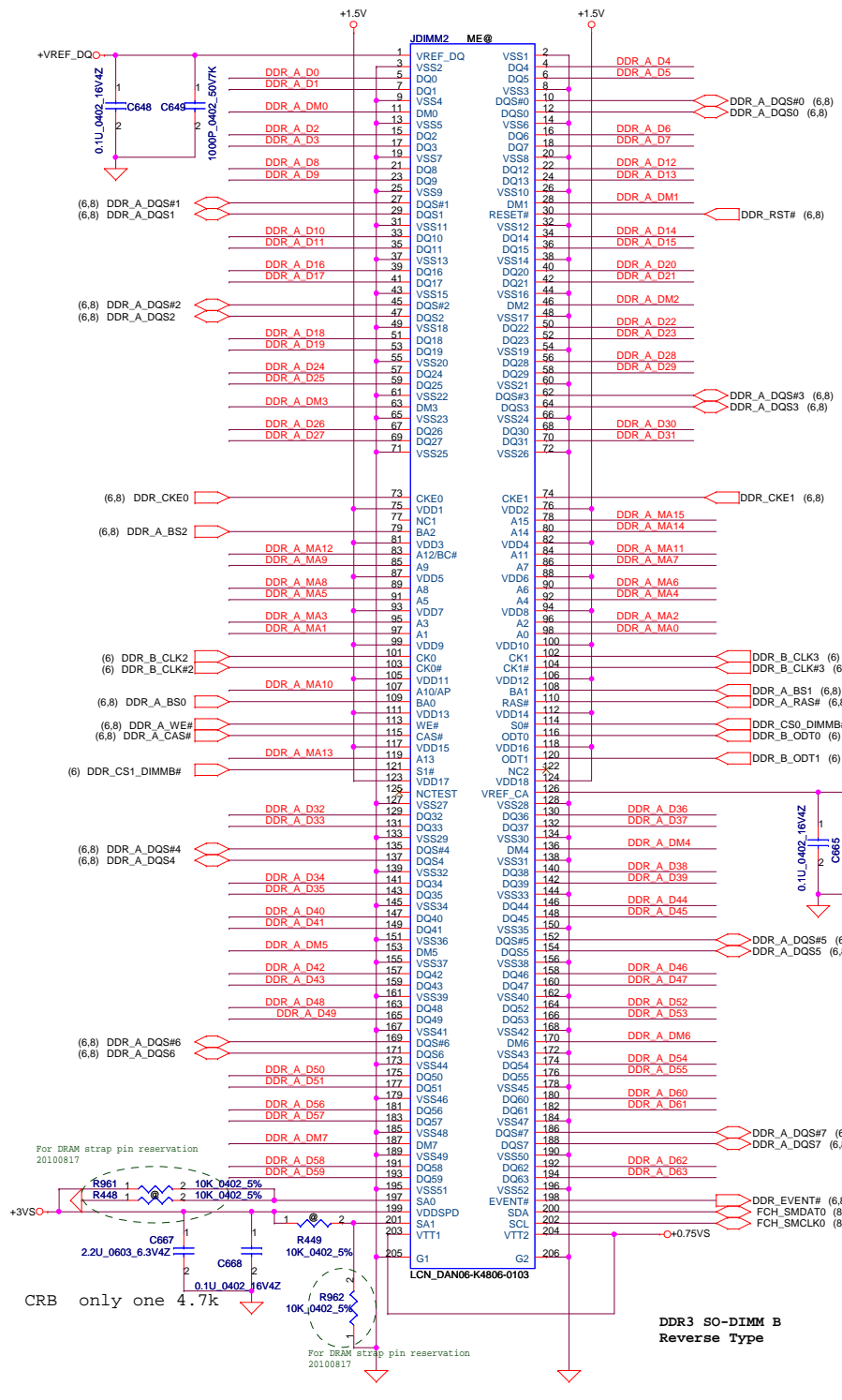
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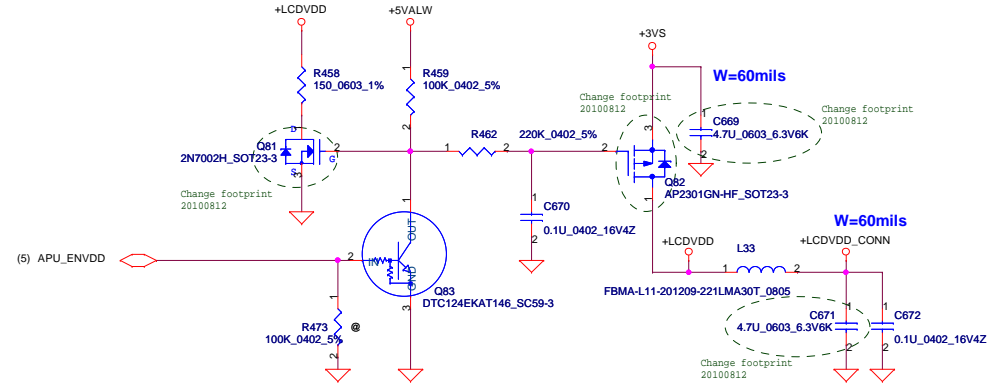
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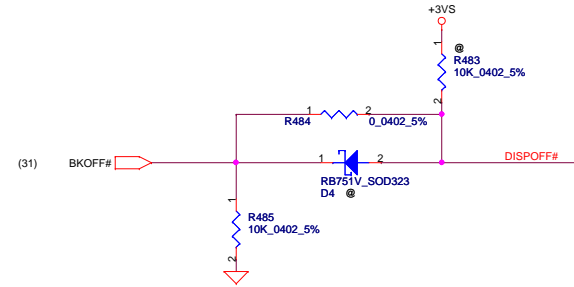
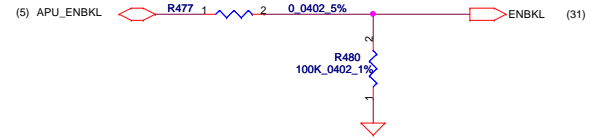
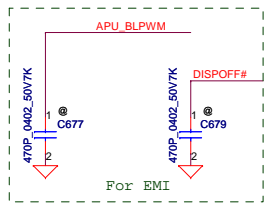
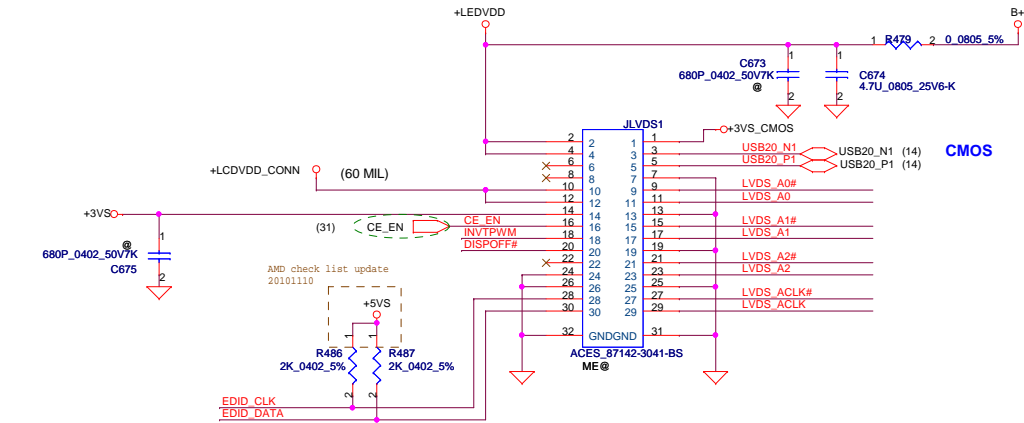
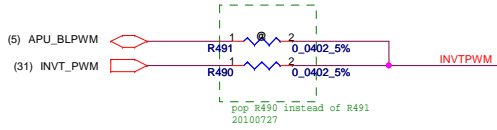


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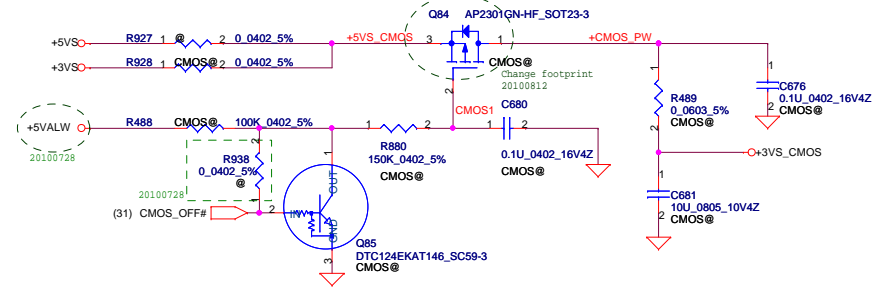
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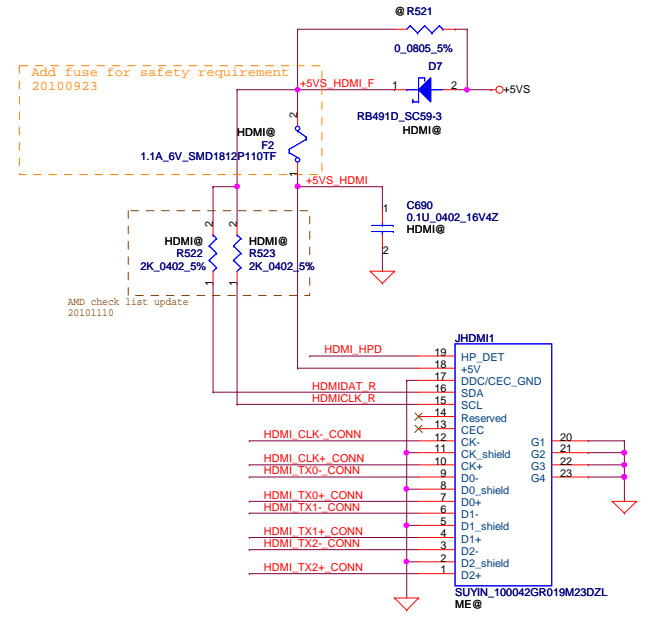
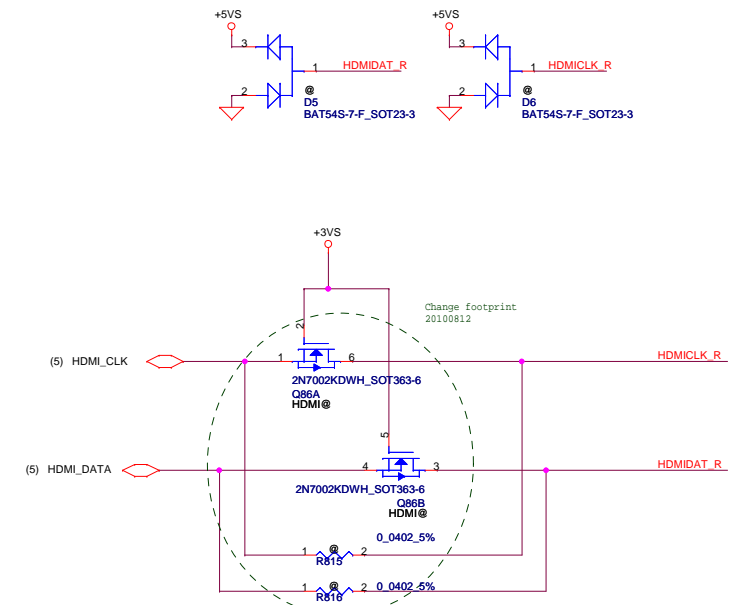
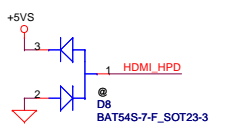
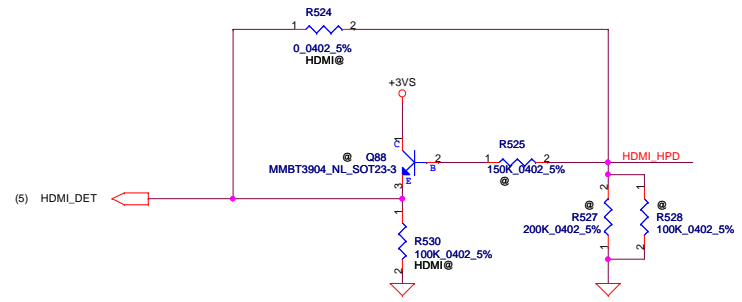
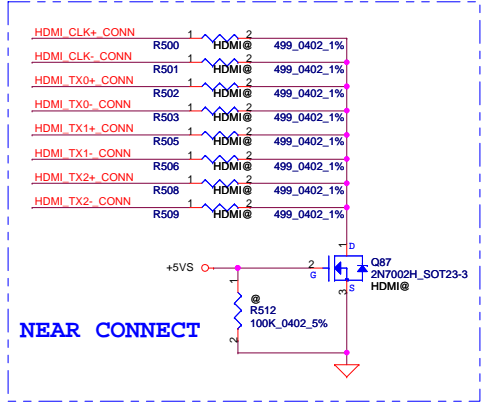
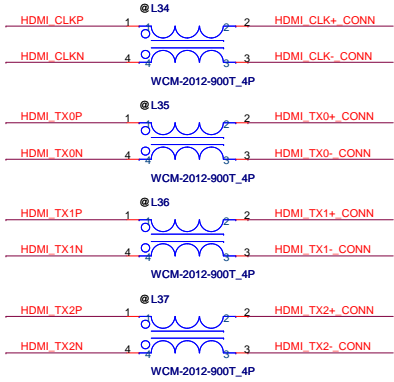


# CMOS Camera

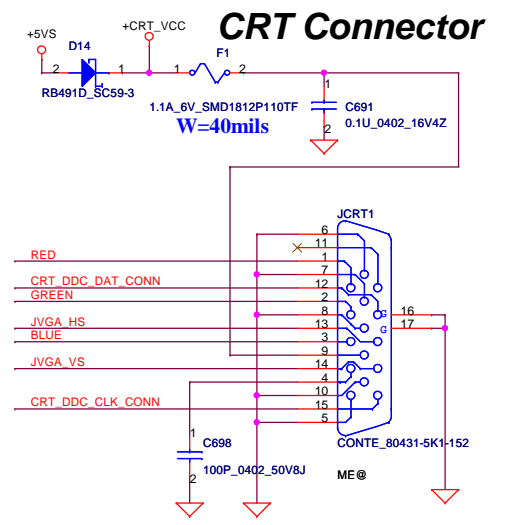
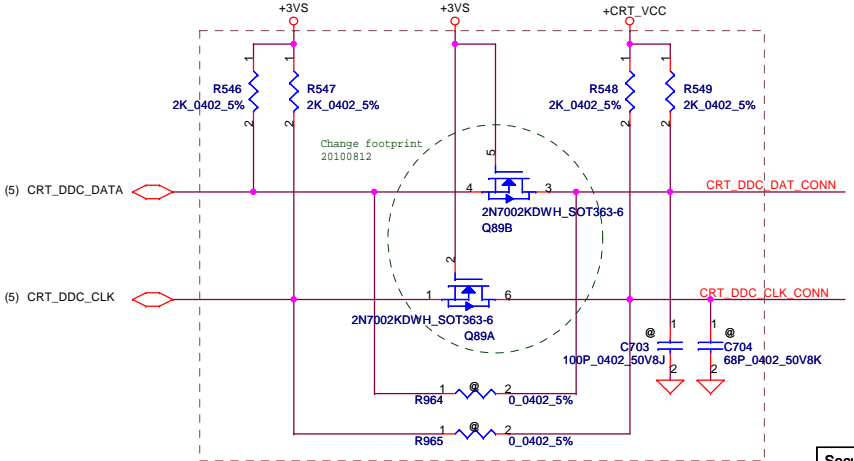
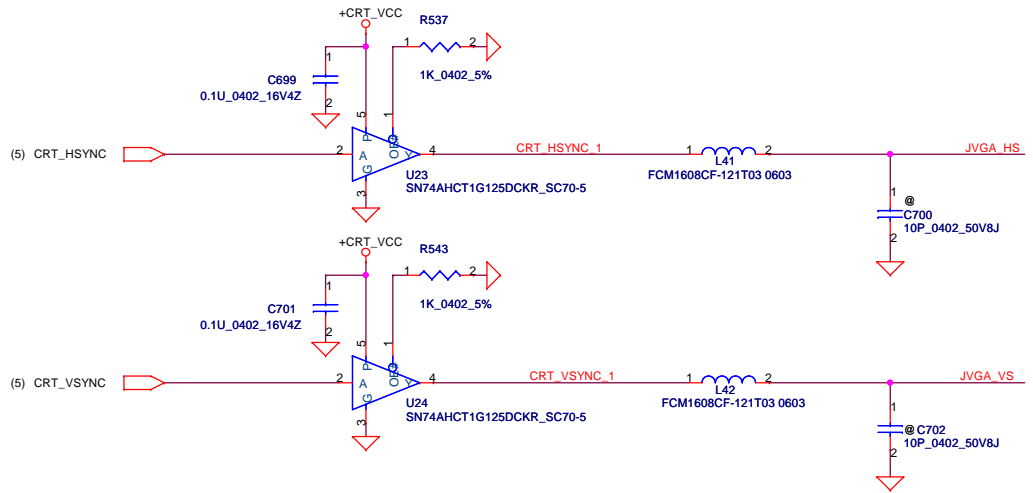
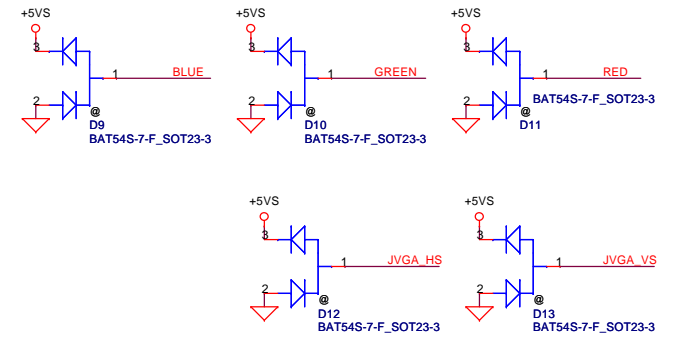
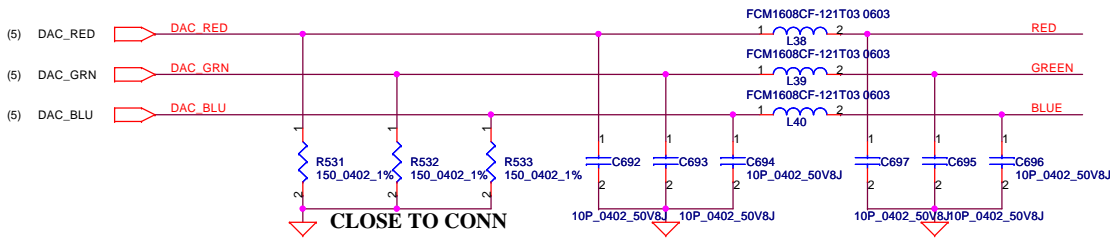


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Issued Date	2010/06/30	Deciphered Date	2012/06/30	Title	LVDS/CAMERA	
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				B	LA6755P/7P	1.0
				Date:	Tuesday, November 30, 2010	Sheet 10 of 48

(5) HDMI_CLKP	R513	1	HDMI@	2	0.0402_5%	HDMI_CLK+_CONN
(5) HDMI_CLKN	R514	1	HDMI@	2	0.0402_5%	HDMI_CLK-_CONN
(5) HDMI_TX0P	R515	1	HDMI@	2	0.0402_5%	HDMI_TX0+_CONN
(5) HDMI_TX0N	R516	1	HDMI@	2	0.0402_5%	HDMI_TX0-_CONN
(5) HDMI_TX1P	R517	1	HDMI@	2	0.0402_5%	HDMI_TX1+_CONN
(5) HDMI_TX1N	R518	1	HDMI@	2	0.0402_5%	HDMI_TX1-_CONN
(5) HDMI_TX2P	R519	1	HDMI@	2	0.0402_5%	HDMI_TX2+_CONN
(5) HDMI_TX2N	R520	1	HDMI@	2	0.0402_5%	HDMI_TX2-_CONN



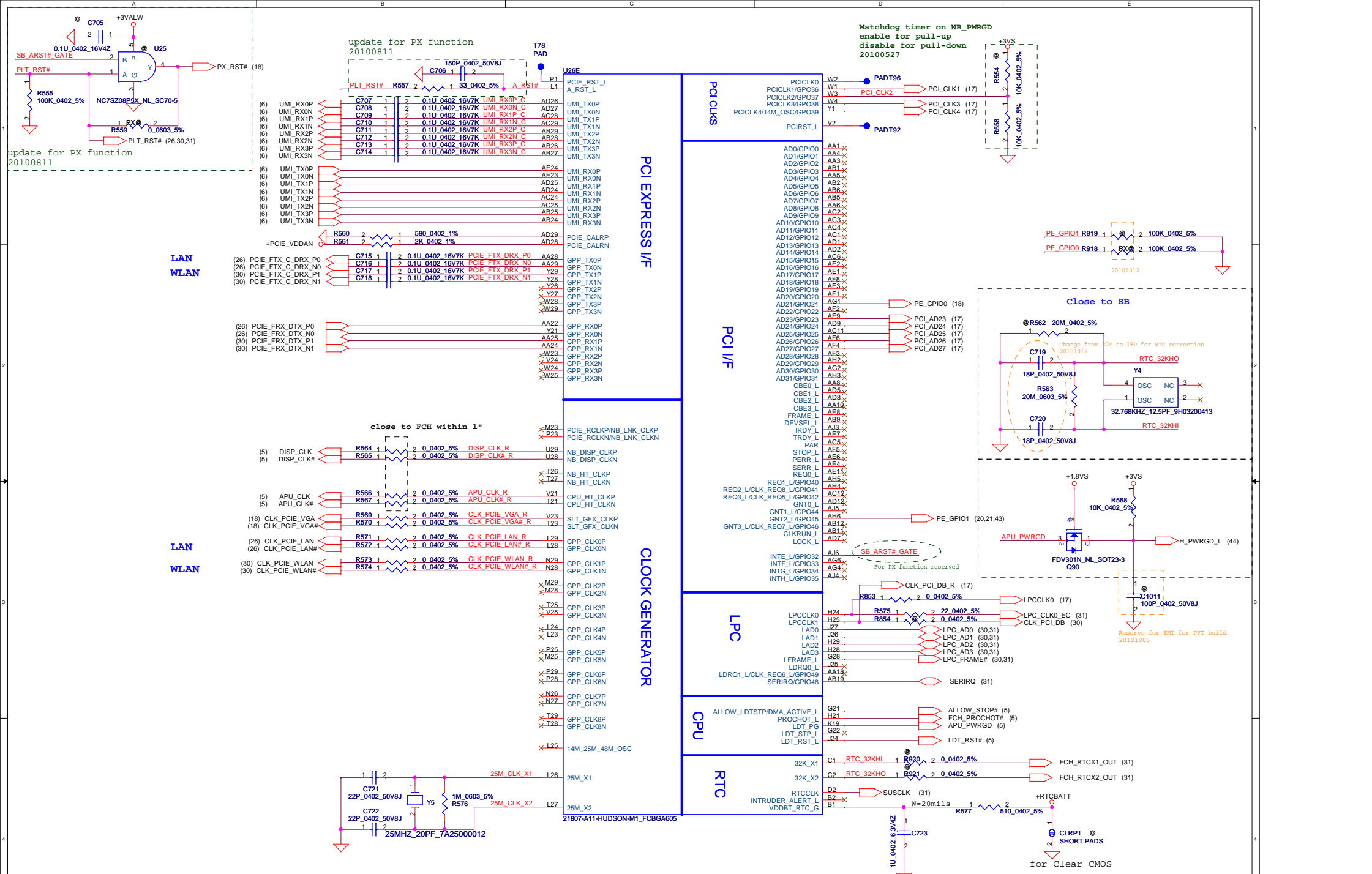
Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date		2010/06/30		Deciphered Date		2012/06/30		Title			
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Size	Document Number	LA6755P/7P		Rev	1.0			Date: Tuesday, November 30, 2010   Sheet 11 of 48			



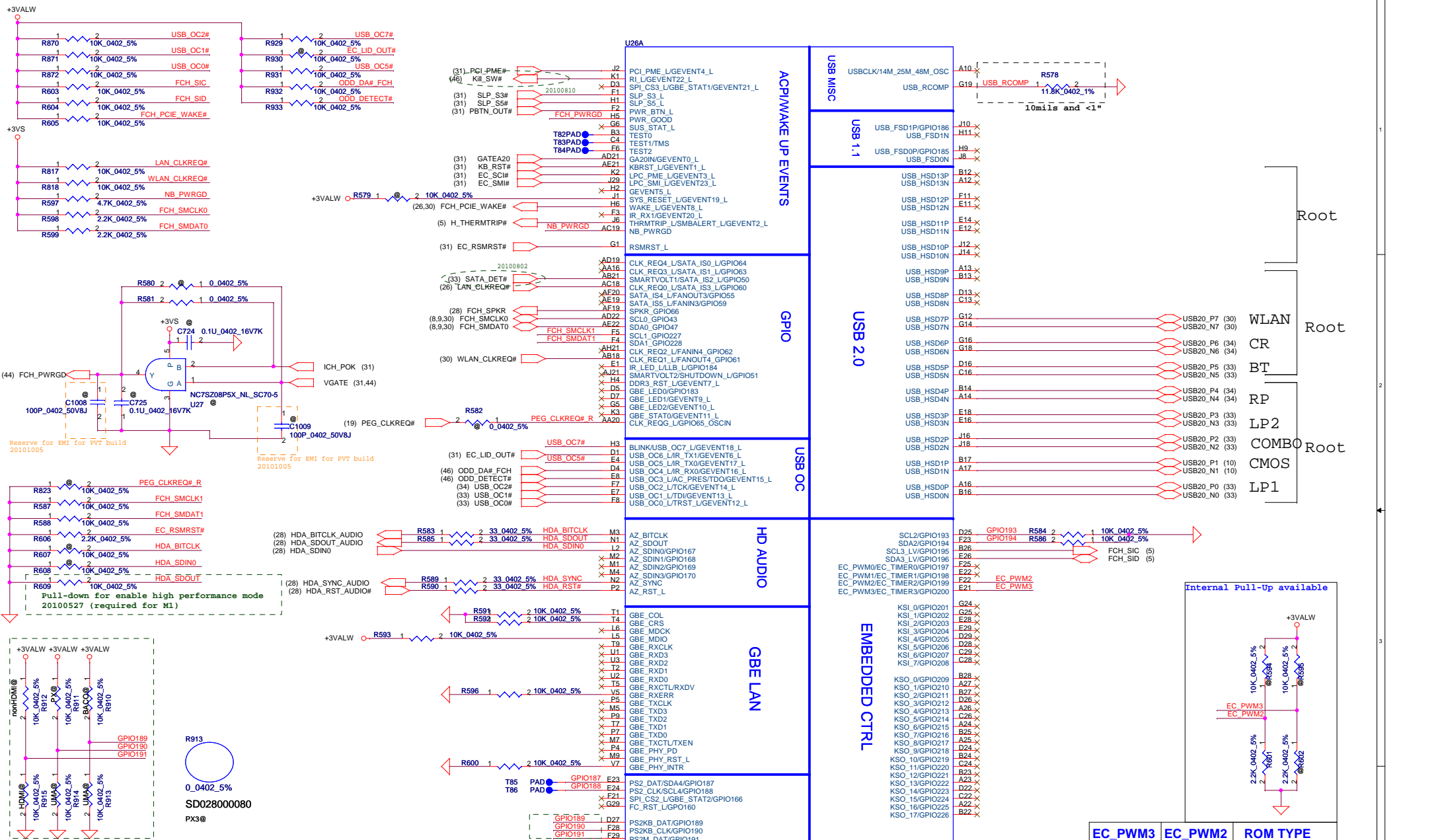
AMD check list update  
20101110

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Title			Compal Electronics, Inc.	
CRT Connector			Rev 1.0	
Size	Document Number	LA6755P/7P		
Custom	Date: Tuesday, November 30, 2010 Sheet 12 of 48			



Security Classification		Compal Secret Data		Title	
Issued Date	2010/06/30	Deciphered Date	2012/06/30	FCH PCIE/PCI/ACPI/LPC/RTC	
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Date	Tuesday, November 30, 2010	Sheet	13	of 48	



BOARD Config.	GPIO189	GPIO190	GPIO191	Function
	0	0	0	UMA
	1	0	0	DIS
	0	1	0	PX3
	1	1	0	PX4
	x	x	1	w/o HDMI

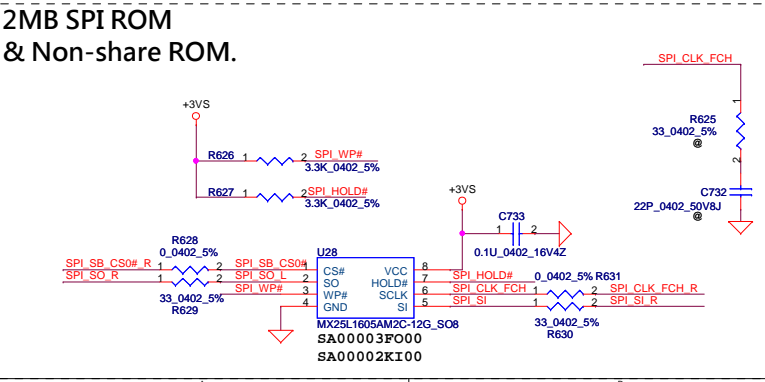
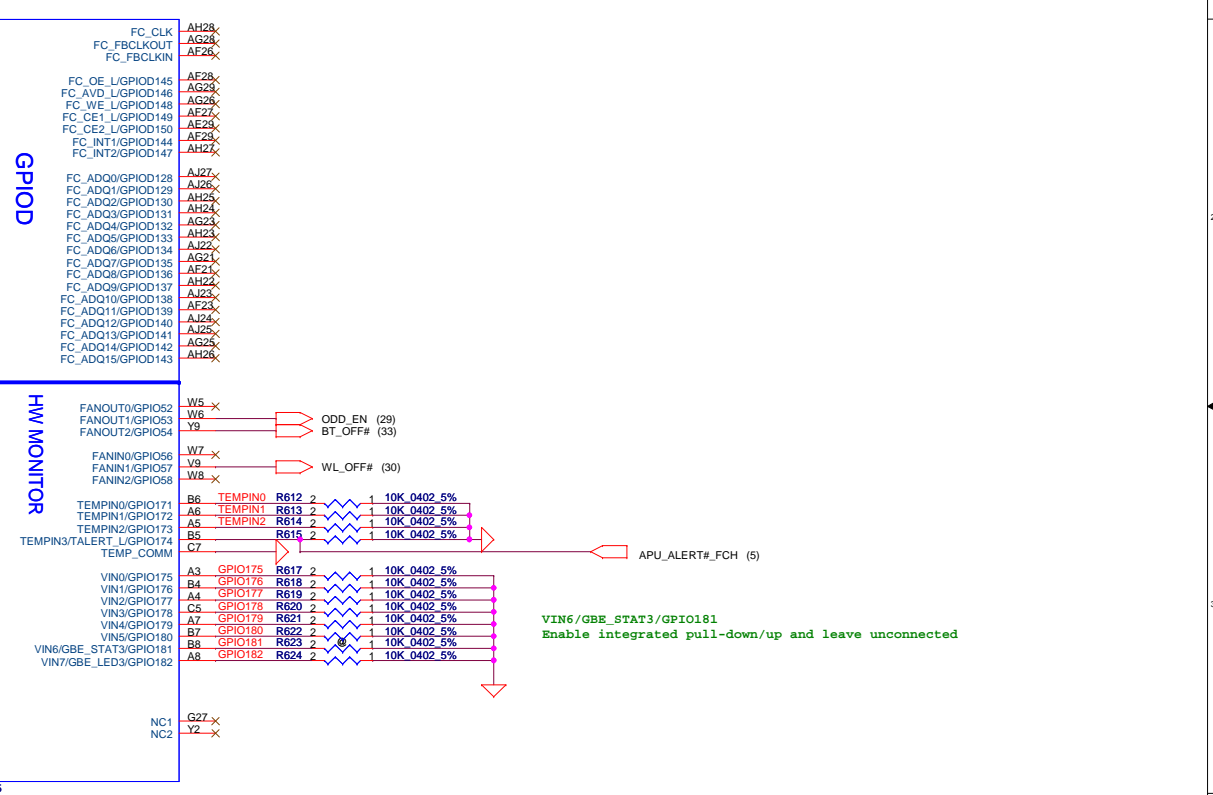
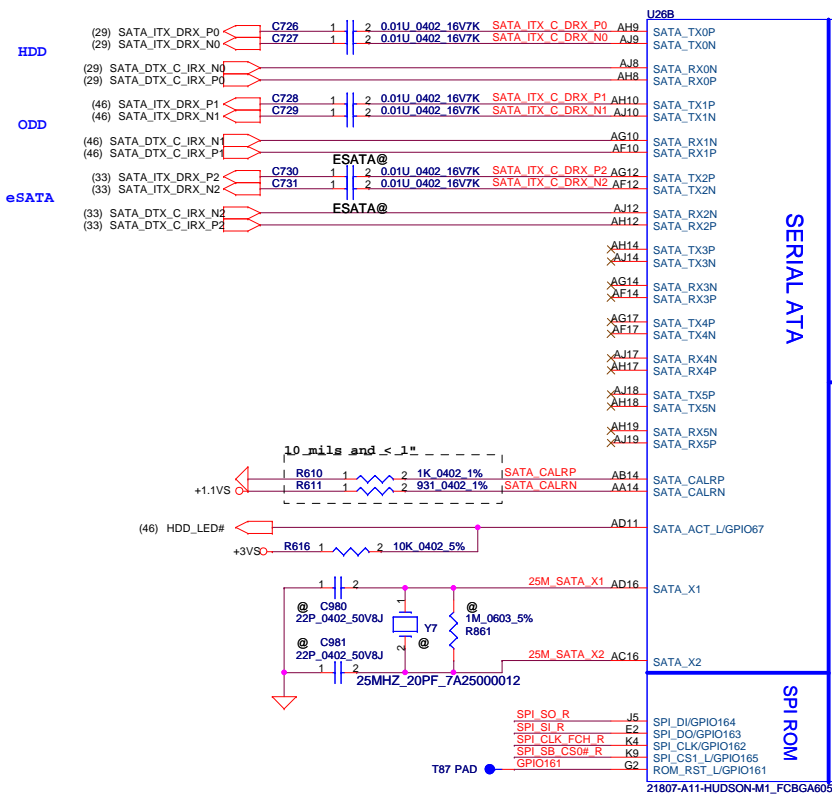
For BRD Config.

Component	Value	Pin
GPIO187	E23	T85
GPIO188	E24	T86
GPIO189	D27	
GPIO190	F28	
GPIO191	F29	
GPIO192	E27	

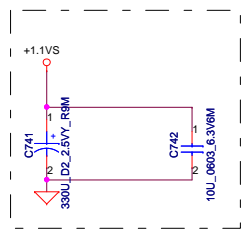
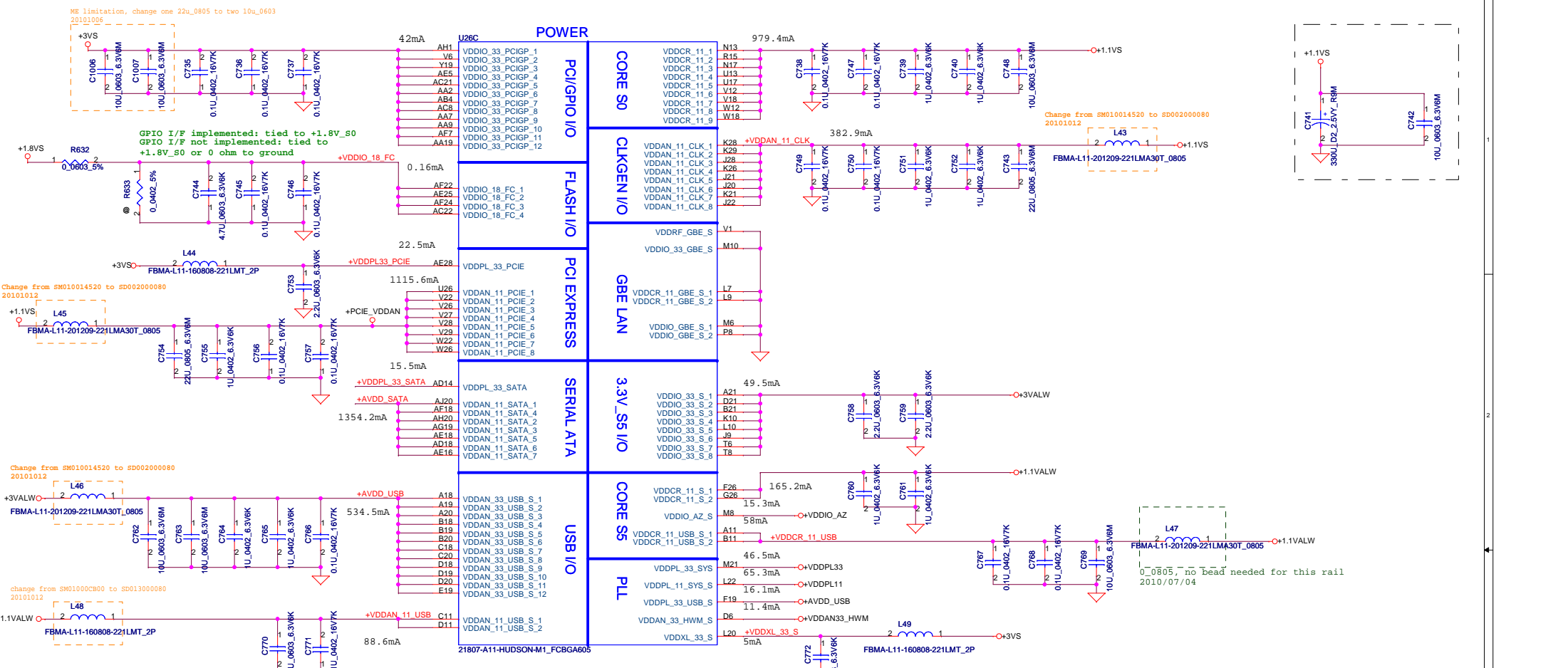
Security Classification	Compal Secret Data	
Issued Date	2010/06/30	Deciphered Date
		2012/06/30

21807-A11-HUDSON-M1\_FCBGA605

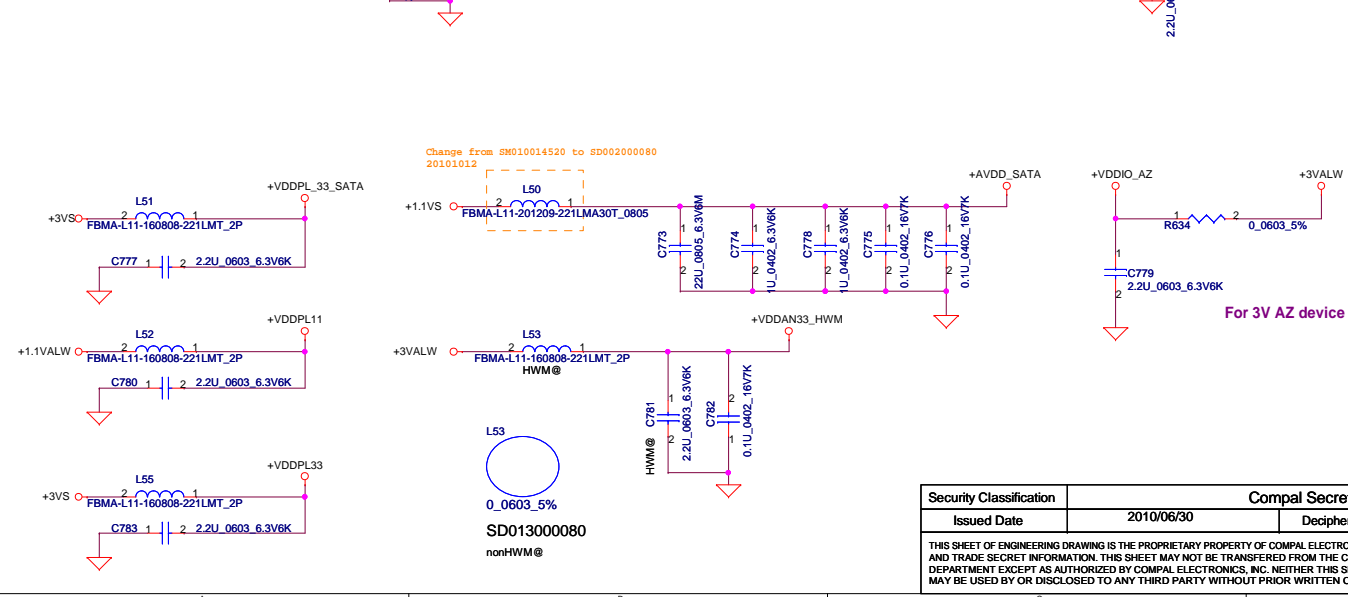
EC_PWM3	EC_PWM2	ROM TYPE
x	0	SPI ROM *
x	x	Reserved
0	0	Reserved
0	x	LPC ROM



Security Classification	Compal Secret Data		Title	
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				FCH-SATA/SPI
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FBMA-L11-201209-221LMA30T\_0805  
no bead needed for this rail  
2010/07/04

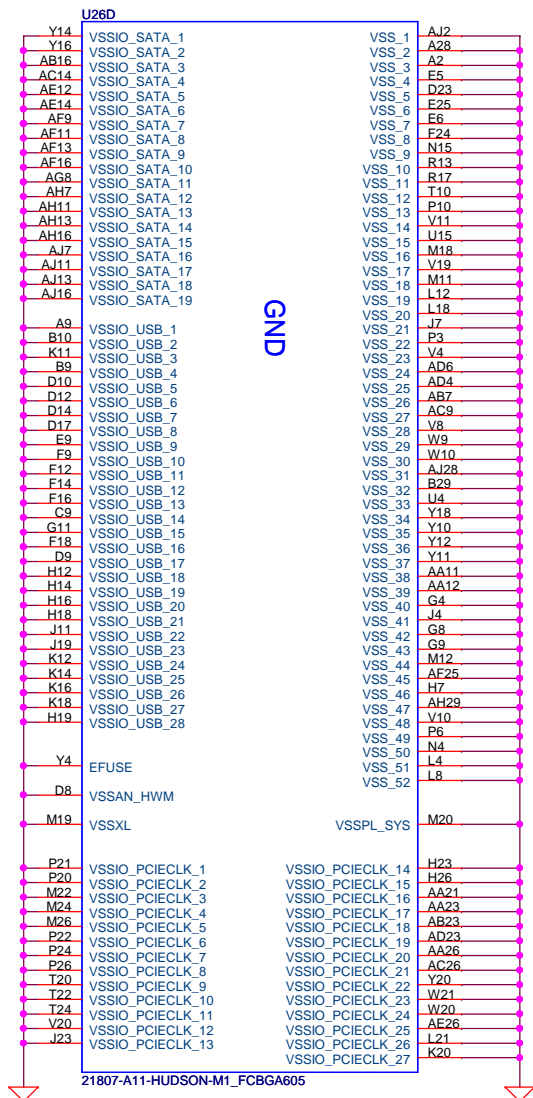


For 3V AZ device

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Issued Date	2010/06/30	Deciphered Date	2012/06/30
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Compal Electronics, Inc.			
FCH PWR			
Title	Document Number		Rev
	LA6755P/7P		1.0
Date:	Tuesday, November 30, 2010	Sheet	16 of 48

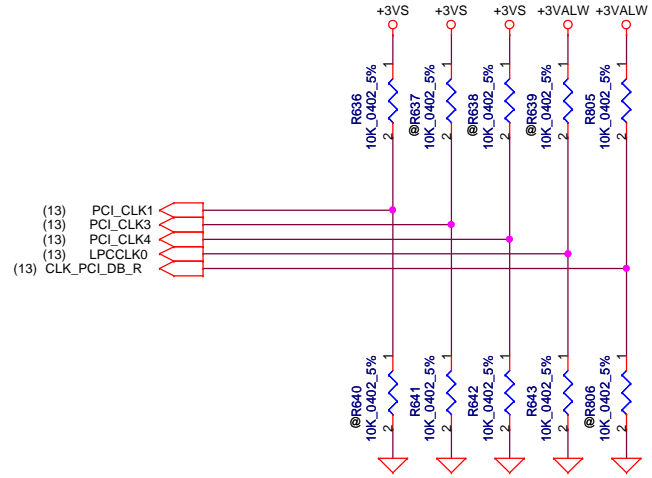




## REQUIRED STRAPS

Check Internal PU/PD

	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	CLK_PCI_DB				
<b>PULL HIGH</b>	ALLOW PCIE GEN2 <b>DEFAULT</b>	USE DEBUG STRAP	Reserved	internal EC ENABLE	Internal CLKGEN Mode				
<b>PULL LOW</b>	FORCE PCIE GEN1	IGNORE DEBUG STRAP	CLKGEN Mode Internal	internal EC DISABLE	External CLKGEN Mode				



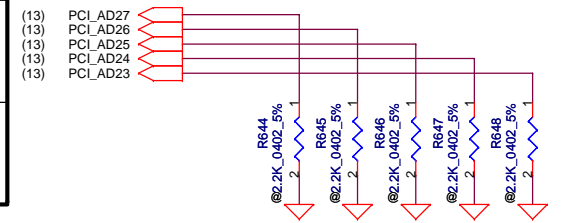
## DEBUG STRAPS

FCH M1 HAS 15K INTERNAL PU FOR PCI\_AD[27:23]

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23 Enable ROM Straps
<b>PULL HIGH</b>	USE internal PLL generated PLL CLK <b>DEFAULT</b>	ILA AUTORUN Disabled <b>DEFAULT</b>	Selects FC PLL <b>DEFAULT</b>	Disable I2C ROM <b>DEFAULT</b>	Required Setting <b>DEFAULT</b>
<b>PULL LOW</b>	BYPASS PCI PLL	ILA AUTORUN Enabled	FC PLL bypassed	Getting Value from I2C EPROM	Reserved

Check AD29,AD28 strap function

check default



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Issued Date	2010/06/30	Deciphered Date	2012/06/30	Title <b>FCH-VSS/Strap</b>		
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				Date: Tuesday, November 30, 2010	Sheet 17	of 48

(6) PCIE\_CTX\_GRX\_P[3..0]  
 (6) PCIE\_CTX\_GRX\_N[3..0]

PCIE\_CTX\_GRX\_P[3..0]  
 PCIE\_CTX\_GRX\_N[3..0]

PCIE\_CTX\_GRX\_P0 AF30  
 PCIE\_CTX\_GRX\_N0 AE31  
 PCIE\_CTX\_GRX\_P1 AE29  
 PCIE\_CTX\_GRX\_N1 AD28  
 PCIE\_CTX\_GRX\_P2 AD30  
 PCIE\_CTX\_GRX\_N2 AC31  
 PCIE\_CTX\_GRX\_P3 AC29  
 PCIE\_CTX\_GRX\_N3 AB28  
 AB30  
 AA29  
 Y30  
 W31  
 W29  
 V28  
 V30  
 U31  
 U29  
 T28  
 T30  
 R31  
 R29  
 P28  
 P30  
 N31  
 N29  
 M28  
 M30  
 L31  
 L29  
 K30

U8A

PCI EXPRESS INTERFACE

PCIE\_RX0P  
 PCIE\_RX0N  
 PCIE\_RX1P  
 PCIE\_RX1N  
 PCIE\_RX2P  
 PCIE\_RX2N  
 PCIE\_RX3P  
 PCIE\_RX3N  
 PCIE\_RX4P  
 PCIE\_RX4N  
 PCIE\_RX5P  
 PCIE\_RX5N  
 PCIE\_RX6P  
 PCIE\_RX6N  
 PCIE\_RX7P  
 PCIE\_RX7N  
 PCIE\_RX8P  
 PCIE\_RX8N  
 PCIE\_RX9P  
 PCIE\_RX9N  
 PCIE\_RX10P  
 PCIE\_RX10N  
 PCIE\_RX11P  
 PCIE\_RX11N  
 PCIE\_RX12P  
 PCIE\_RX12N  
 PCIE\_RX13P  
 PCIE\_RX13N  
 PCIE\_RX14P  
 PCIE\_RX14N  
 PCIE\_RX15P  
 PCIE\_RX15N

PCIE\_CRX\_GTX\_P[3..0]  
 PCIE\_CRX\_GTX\_N[3..0]

PCIE\_CRX\_GTX\_P[3..0] (6)  
 PCIE\_CRX\_GTX\_N[3..0] (6)

AH30 PCIE\_CRX\_C\_GTX\_P0 0.1U\_0402 10V7K 2 1 C273 PX@ PCIE\_CRX\_GTX\_P0  
 AG31 PCIE\_CRX\_C\_GTX\_N0 0.1U\_0402 10V7K 2 1 C272 PX@ PCIE\_CRX\_GTX\_N0  
 AG29 PCIE\_CRX\_C\_GTX\_P1 0.1U\_0402 10V7K 2 1 C274 PX@ PCIE\_CRX\_GTX\_P1  
 AF28 PCIE\_CRX\_C\_GTX\_N1 0.1U\_0402 10V7K 2 1 C275 PX@ PCIE\_CRX\_GTX\_N1  
 AF27 PCIE\_CRX\_C\_GTX\_P2 0.1U\_0402 10V7K 2 1 C276 PX@ PCIE\_CRX\_GTX\_P2  
 AF26 PCIE\_CRX\_C\_GTX\_N2 0.1U\_0402 10V7K 2 1 C277 PX@ PCIE\_CRX\_GTX\_N2  
 AD27 PCIE\_CRX\_C\_GTX\_P3 0.1U\_0402 10V7K 2 1 C278 PX@ PCIE\_CRX\_GTX\_P3  
 AD26 PCIE\_CRX\_C\_GTX\_N3 0.1U\_0402 10V7K 2 1 C279 PX@ PCIE\_CRX\_GTX\_N3  
 AC25  
 AB25  
 Y23  
 Y24  
 AB27  
 AB26  
 Y27  
 Y26  
 W24  
 W23  
 V27  
 U26  
 U24  
 U23  
 T26  
 T27  
 T24  
 T23  
 P27  
 P26  
 P24  
 P23  
 M27  
 M26  
 M24  
 M23

U8F

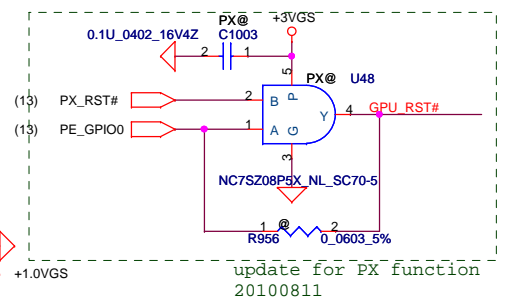
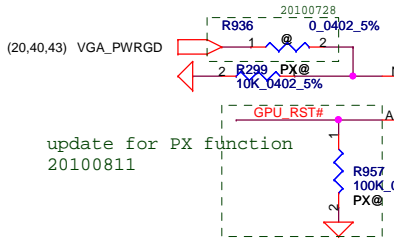
LVDS CONTROL VARY\_BL DIGON AB11 AB12  
 TXCLK\_UP\_DPF3P AH20  
 TXCLK\_UN\_DPF3N AJ19  
 TXOUT\_U0P\_DPF2P AL21  
 TXOUT\_U0N\_DPF2N AK20  
 TXOUT\_U1P\_DPF1P AH22  
 TXOUT\_U1N\_DPF1N AJ21  
 TXOUT\_U2P\_DPF0P AL23  
 TXOUT\_U2N\_DPF0N AK22  
 TXOUT\_U3P AK24  
 TXOUT\_U3N AJ23  
 LVTMDP  
 TXCLK\_LP\_DPE3P AL15  
 TXCLK\_LN\_DPE3N AK14  
 TXOUT\_L0P\_DPE2P AH16  
 TXOUT\_L0N\_DPE2N AJ15  
 TXOUT\_L1P\_DPE1P AL17  
 TXOUT\_L1N\_DPE1N AK16  
 TXOUT\_L2P\_DPE0P AH18  
 TXOUT\_L2N\_DPE0N AJ17  
 TXOUT\_L3P AL19  
 TXOUT\_L3N AK18

216-0774207-A11ROB\_FCBGA631  
 PX@

LVDS

(13) CLK\_PCIE\_VGA  
 (13) CLK\_PCIE\_VGA#

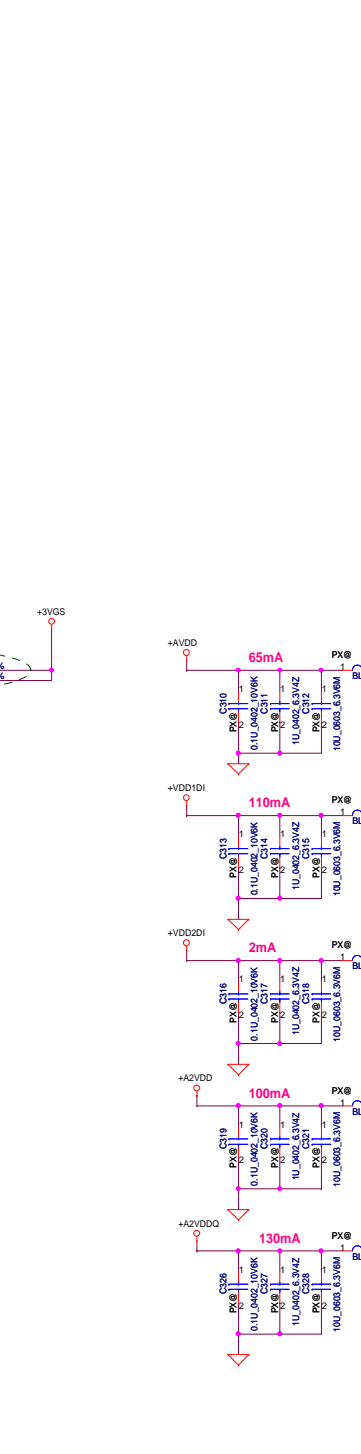
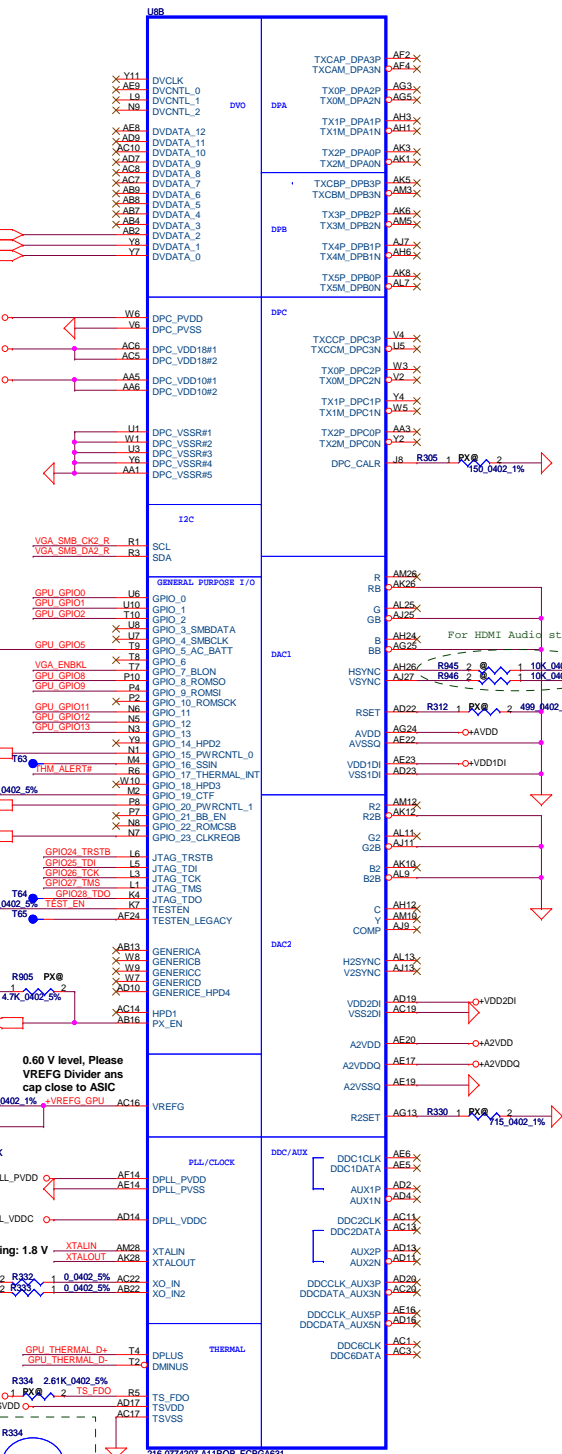
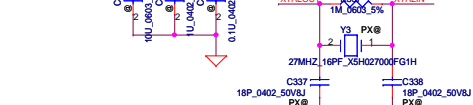
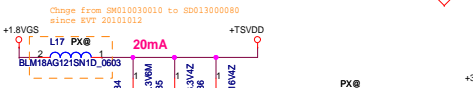
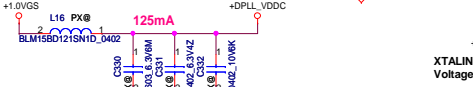
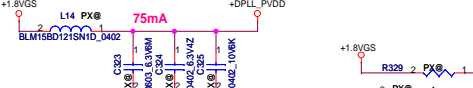
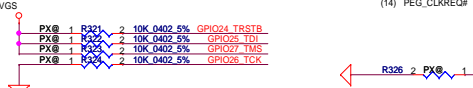
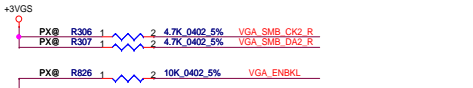
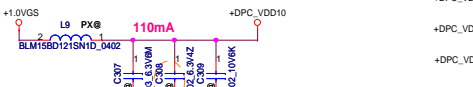
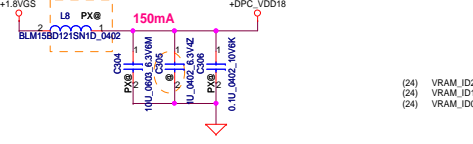
CLK\_PCIE\_VGA AK30  
 CLK\_PCIE\_VGA# AK32



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Size	Document Number			Rev	
B	LA6755P/7P			1.0	
Date:	Tuesday, November 30, 2010		Sheet 18 of 48		

TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for desktop)

change from SM01000900 to SD02800080  
20101012



### CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

Internal pull down

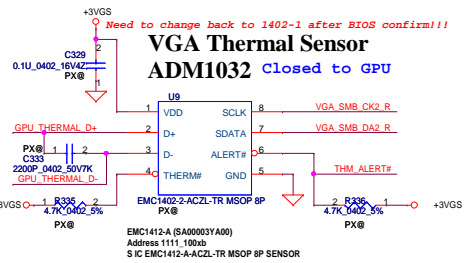
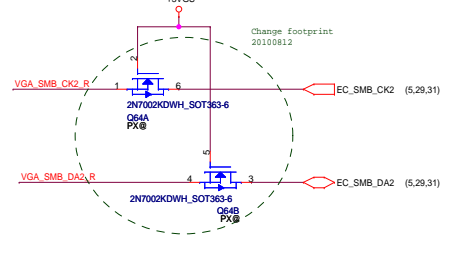
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	PCI FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPIO1	PCI TRANSMITTER DE-EMPHASIS ENABLED	0
RSVD	GPIO2	0 : 2.5GT/s ; 1 : 5.0GT/s, internal PD.	0
RSVD	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	000
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
RSVD	H2SYNC		0
RSVD	GENERICC		0
AUD[0]	HSYNC	AUD[0] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	11

**AMD RESERVED CONFIGURATION STRAPS**  
ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOs ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET

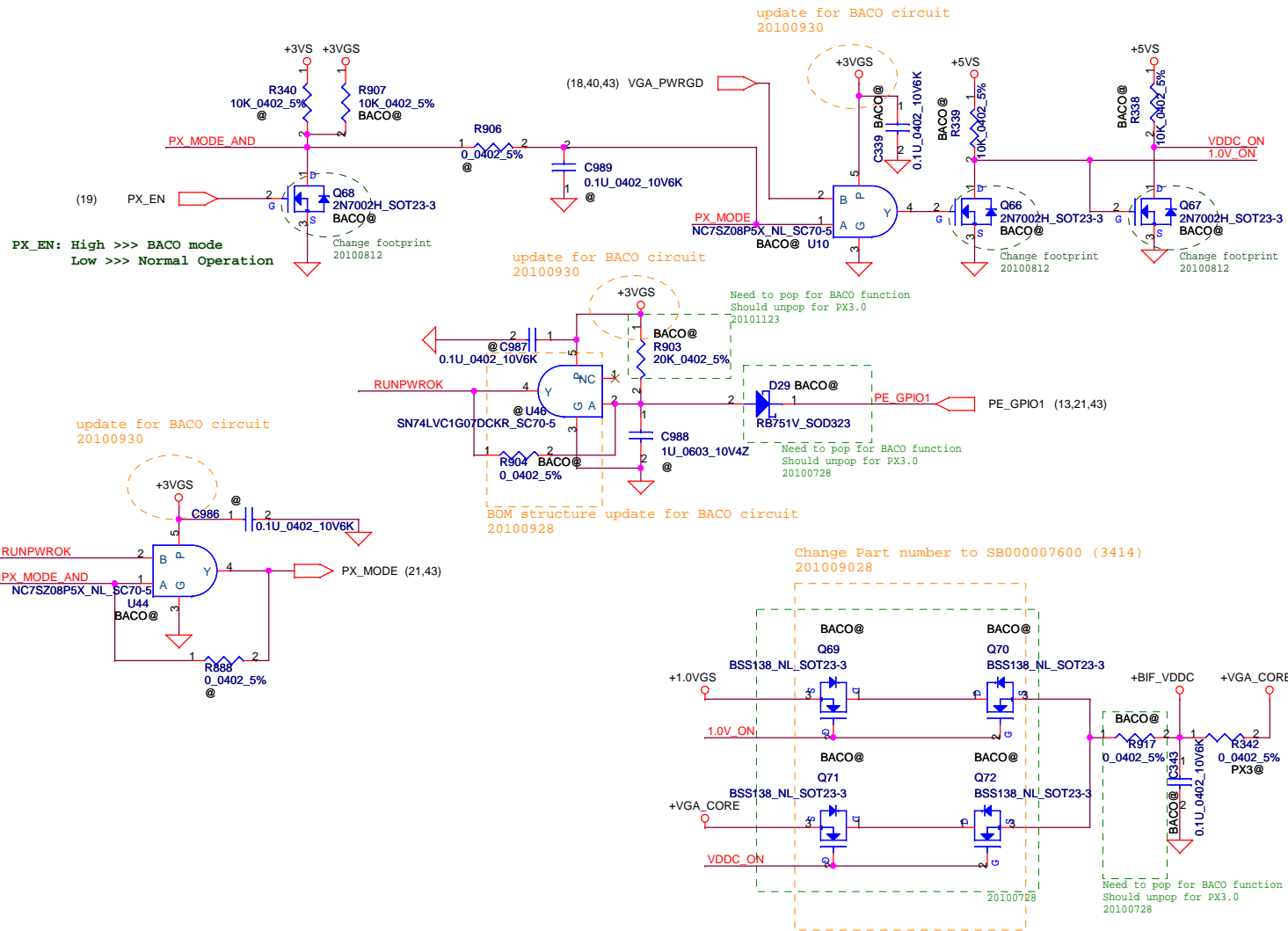
GPIO21 H2SYNC GENERICC GPIO2 GPIO8

### STRAPS

- GPU GPIO0 R309 2 PX@ 10k 0.402 5%
- GPU GPIO1 R310 2 PX@ 10k 0.402 5%
- GPU GPIO2 R311 2 PX@ 10k 0.402 5%
- GPU GPIO5 R308 2 PX@ 10k 0.402 5%
- GPU GPIO8 R313 2 PX@ 10k 0.402 5%
- GPU GPIO9 R314 2 PX@ 10k 0.402 5%
- GPU GPIO11 R315 2 PX@ 10k 0.402 5%
- GPU GPIO12 R316 2 PX@ 10k 0.402 5%
- GPU GPIO13 R317 2 PX@ 10k 0.402 5%

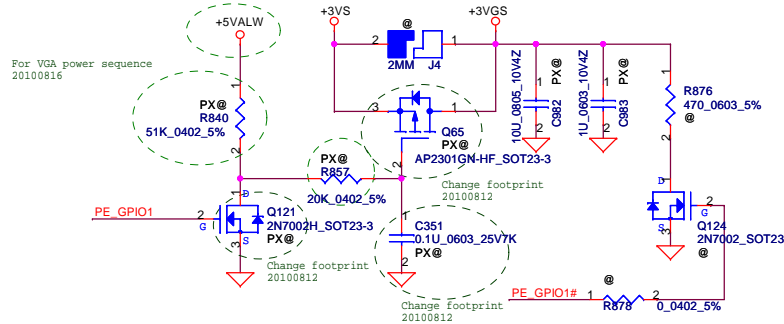


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Title		RobsonXT-S3 Main Generic/MSIC	
Size	Document Number	LA675P/7P	Rev 1.0
Date:	Tuesday, November 30, 2010	ISheet	19 of 48

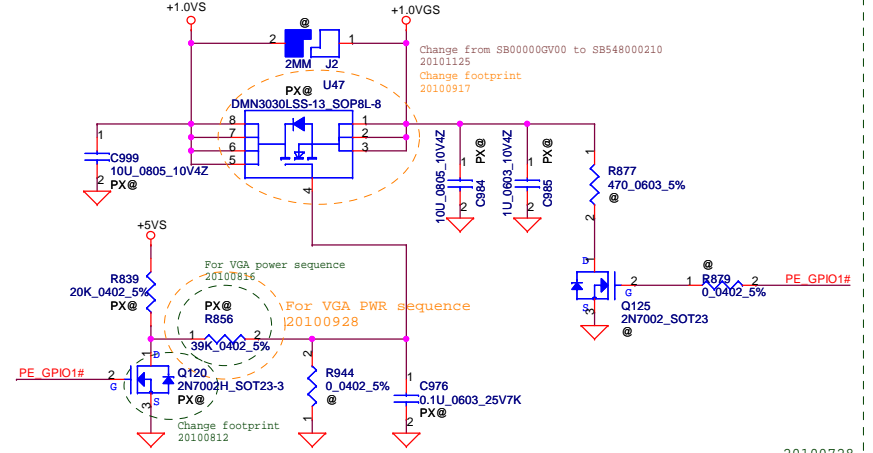


Security Classification	Compal Secret Data		Compal Electronics, Inc.	
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Size B	Document Number	LA6755P/7P		Rev 1.0
Date:	Tuesday, November 30, 2010	Sheet	20 of 48	

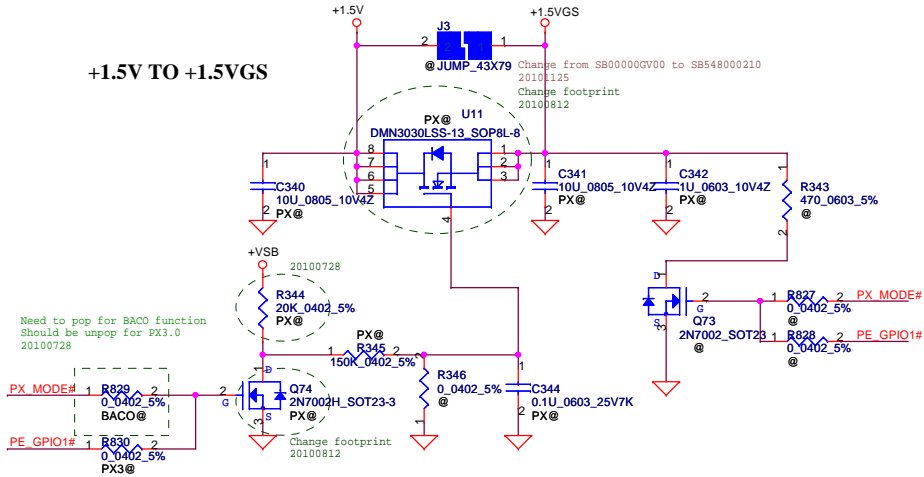
**+3.3VS TO +3.3VGS**



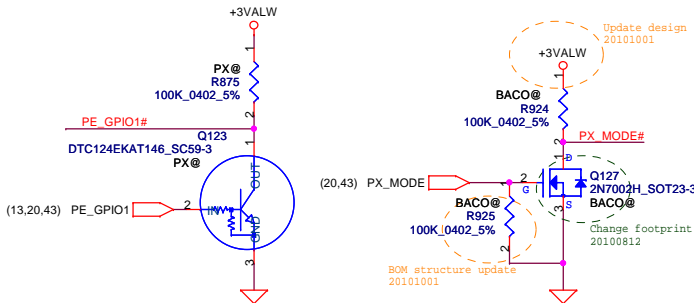
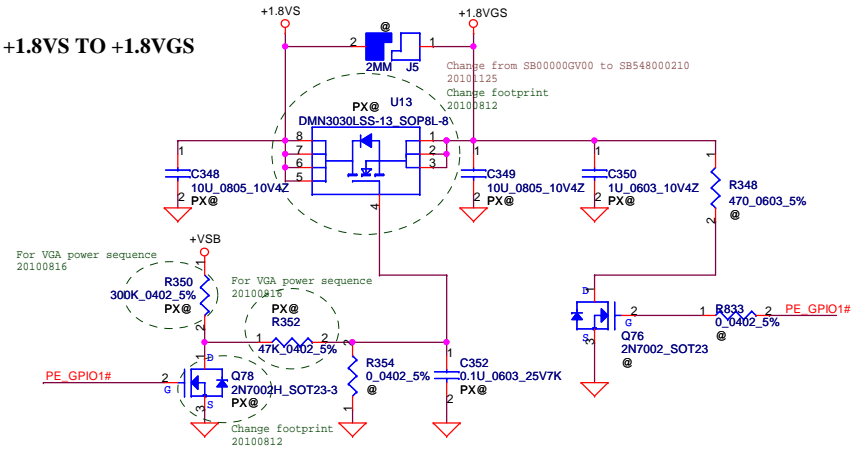
**+VGA\_PCIE TO +1.0VGS**



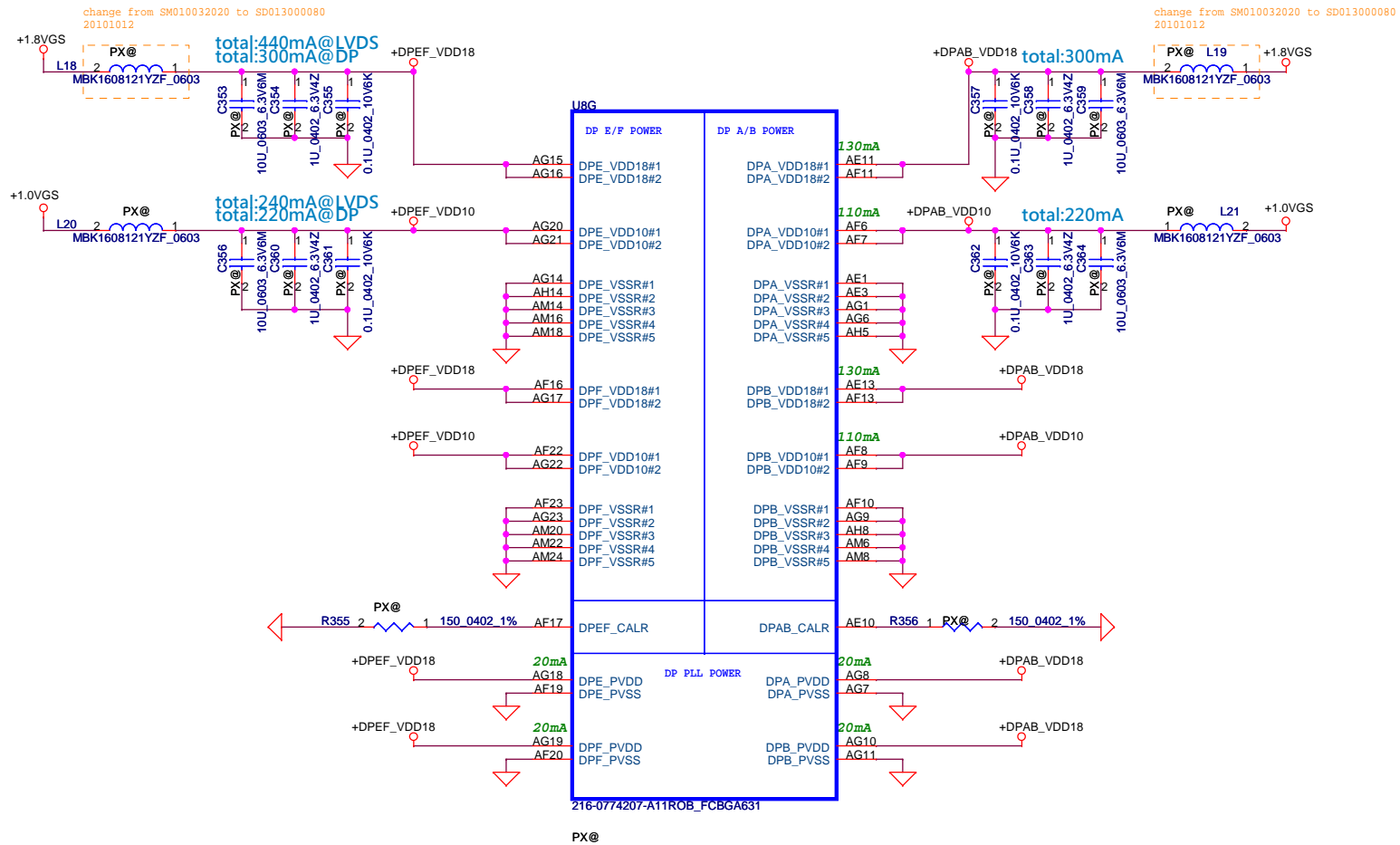
**+1.5V TO +1.5VGS**



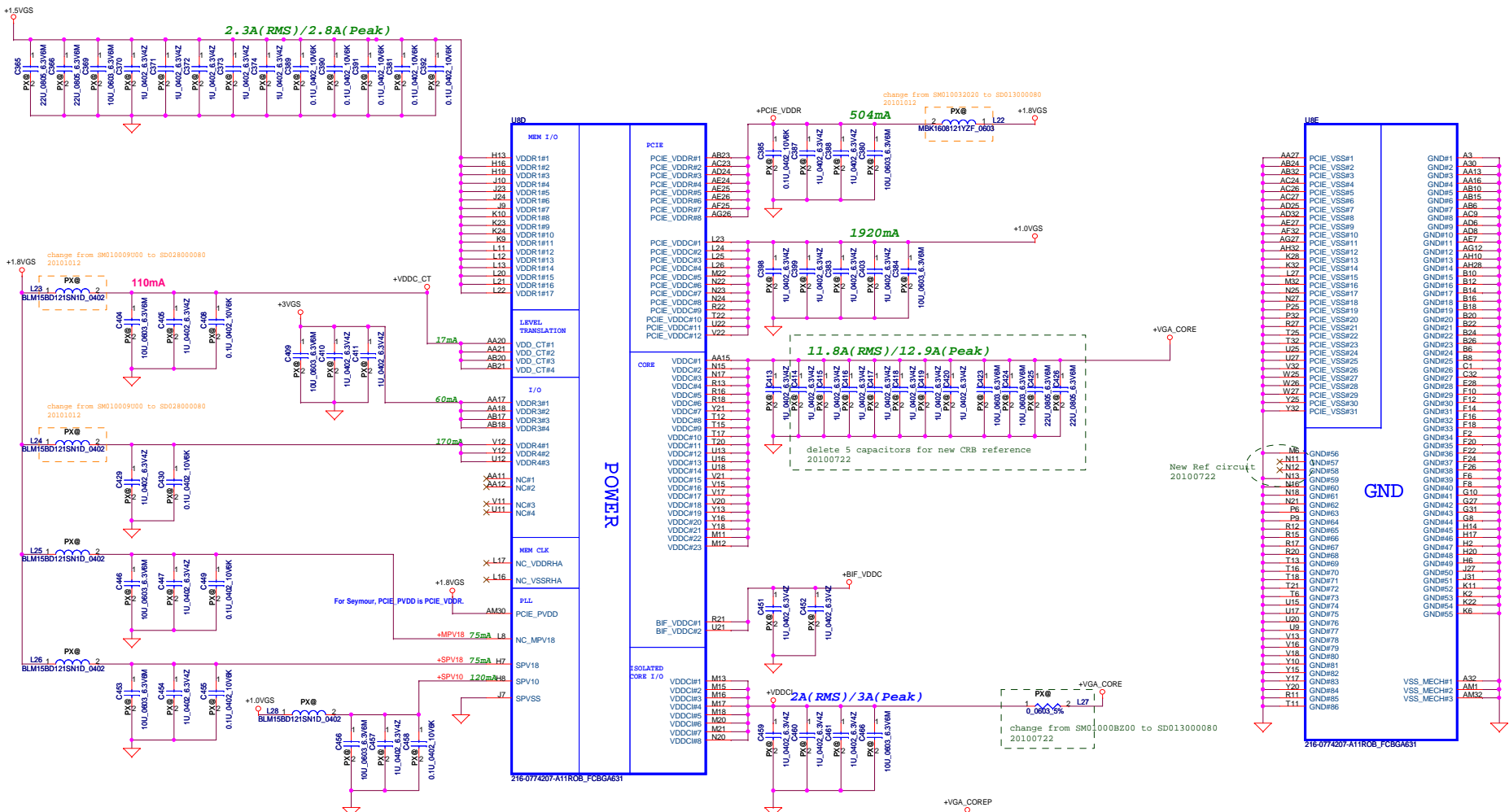
**+1.8VS TO +1.8VGS**



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Size Custom	Document Number	LA6755P/7P		Rev	1.0
Date: Tuesday, November 30, 2010	Sheet	21	of	48	

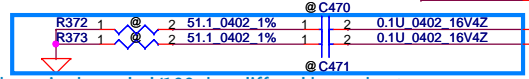
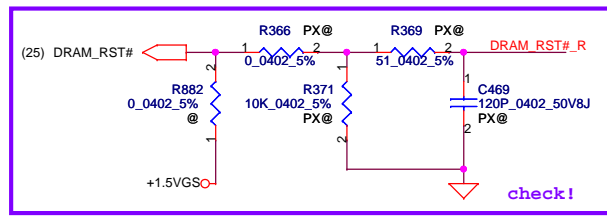
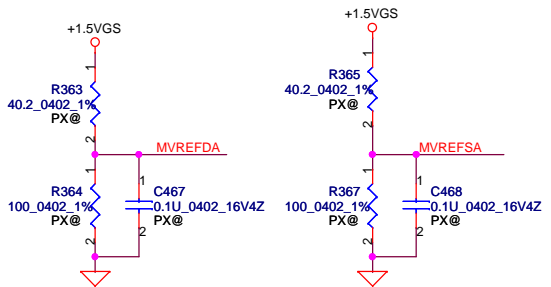


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Issued Date	2010/06/30	Deciphered Date	2012/06/30	Title RobsonXT-S3 DP PWR		
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				Date:	Tuesday, November 30, 2010	Sheet 22 of 48

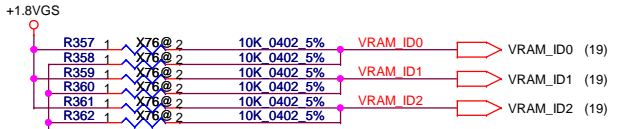
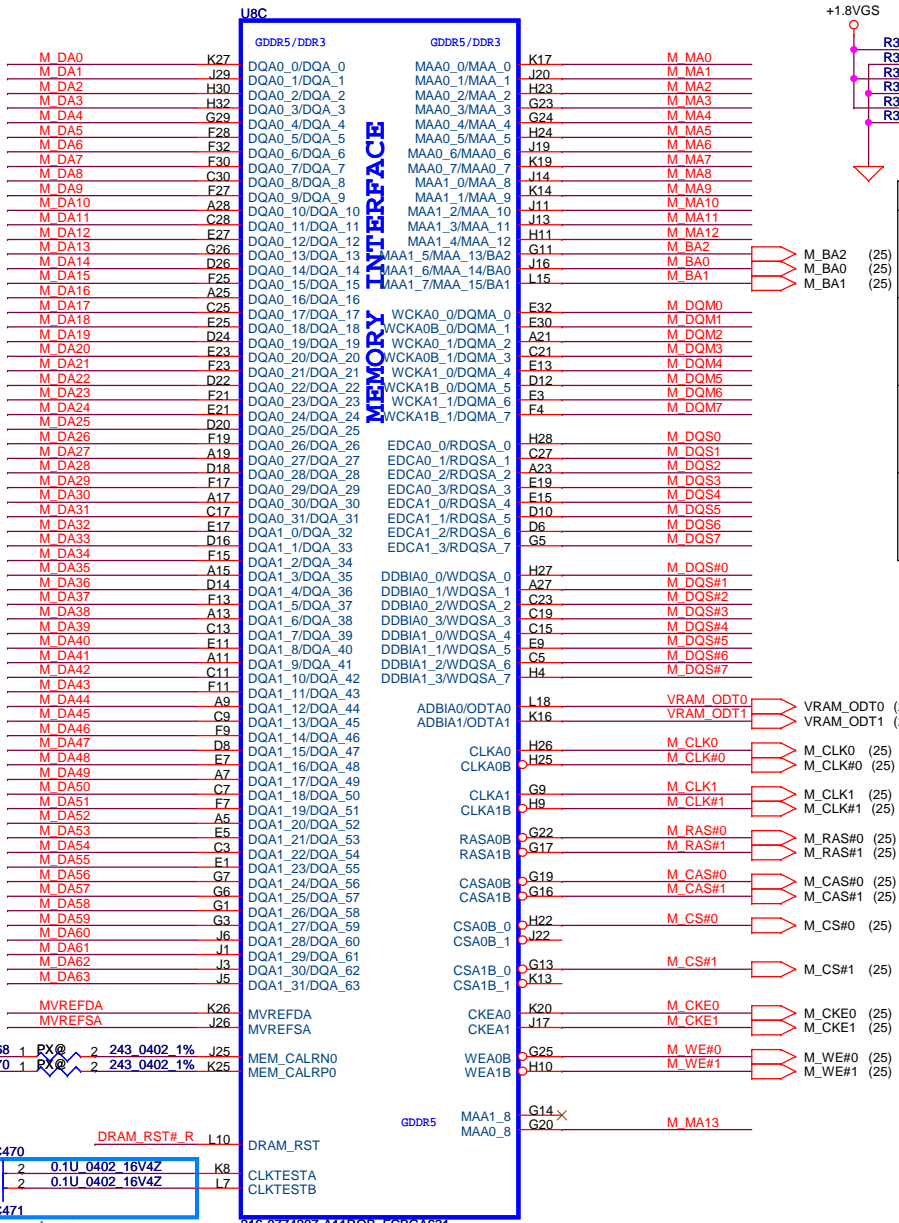


Source	dist.	0.1u	1u	10u
1.5VGS	VDDR1	10	10	5
1.8VGS	PCIE_VDDR	2	3	1
VGA_core	PCIE_VDDC	7	1	
	VDDC		25	6
	VDDCI		6	2

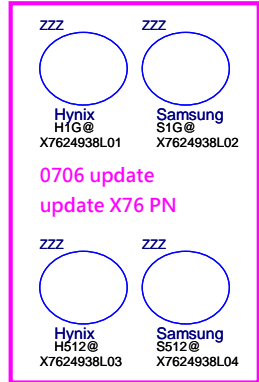
- (25) M\_DA[63..0] M\_DA[63..0]
- (25) M\_MA[13..0] M\_MA[13..0]
- (25) M\_DQM[7..0] M\_DQM[7..0]
- (25) M\_DQS[7..0] M\_DQS[7..0]
- (25) M\_DQS#[7..0] M\_DQS#[7..0]



Route 50ohms single-ended/100ohm diff and keep short debug only, for clock observation, if not need, DNI.



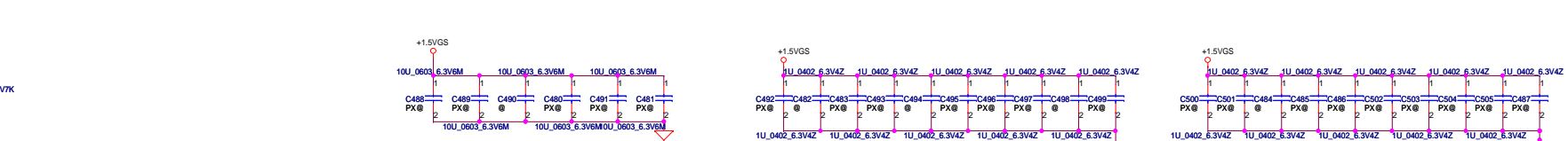
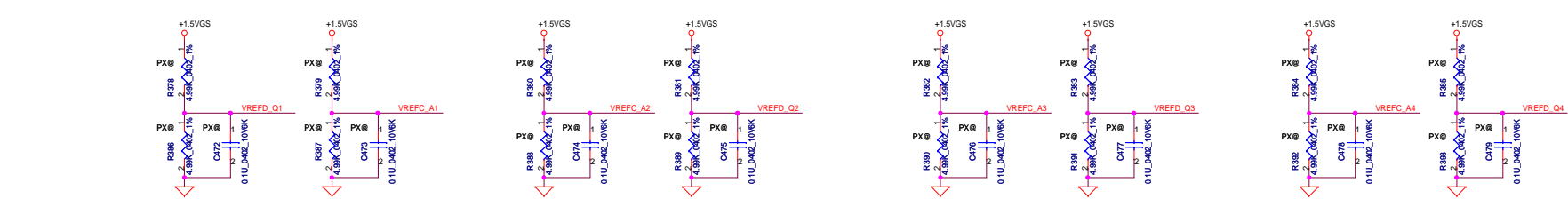
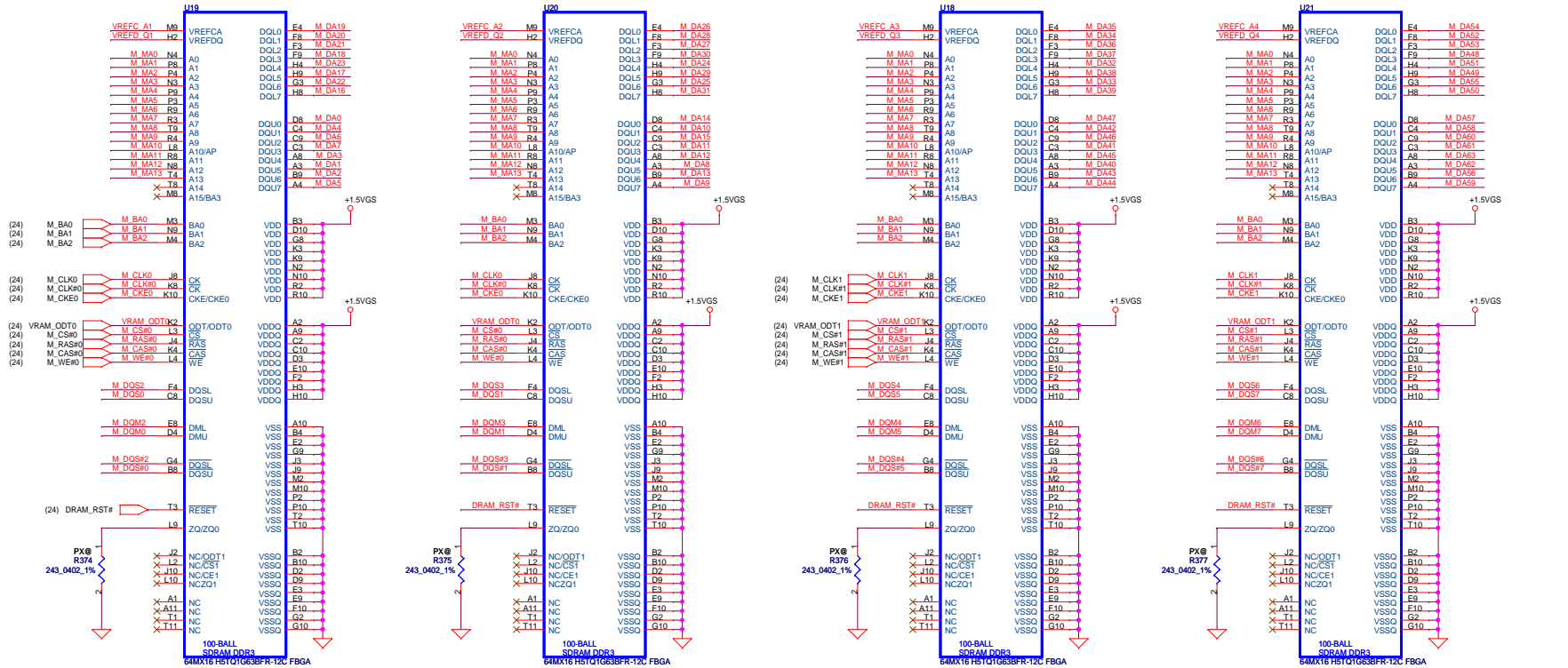
Vendor	VRAM_ID0	VRAM_ID1	VRAM_ID2
Hynix 512MB PN:SA000032460	1	0	0
Hynix 1GB PN:SA00003VS20	1	0	1
Samsung 512MB PN:SA000035700	0	1	0
Samsung 1GB PN:SA00003MQ20	0	1	1



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				Date:	Tuesday, November 30, 2010
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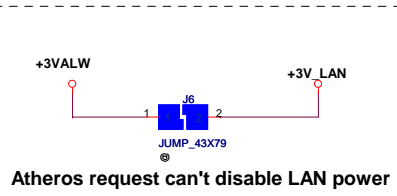


- (24) M\_DA[63..0] M\_DA[63..0]
- (24) M\_MA[13..0] M\_MA[13..0]
- (24) M\_DQM[7..0] M\_DQM[7..0]
- (24) M\_DQS[7..0] M\_DQS[7..0]
- (24) M\_DQS#[7..0] M\_DQS#[7..0]

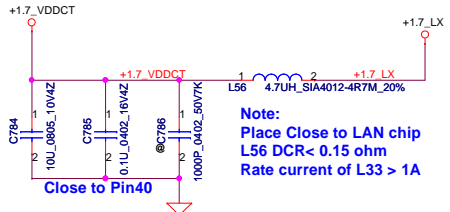


**VRAM P/N :**  
 Hynix : SA000041S10 (S IC D3 64MX16 H5TQ1G63BFR-11C FBGA C38! )  
 Samsung : SA000041T10 (S IC D3 64MX16 K4W1G1646E-HC11 FBGA C38! )  
 update VRAM PN 0619 update

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Size	C	Document Number	LA6755P/7P	Rev 1.0
Date:	Tuesday, November 30, 2010	Sheet	25	of 48

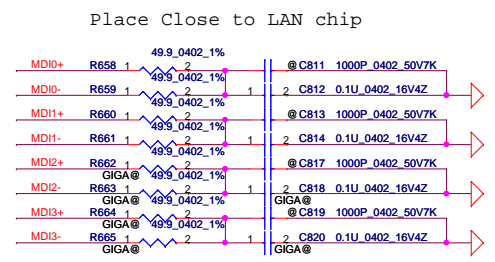
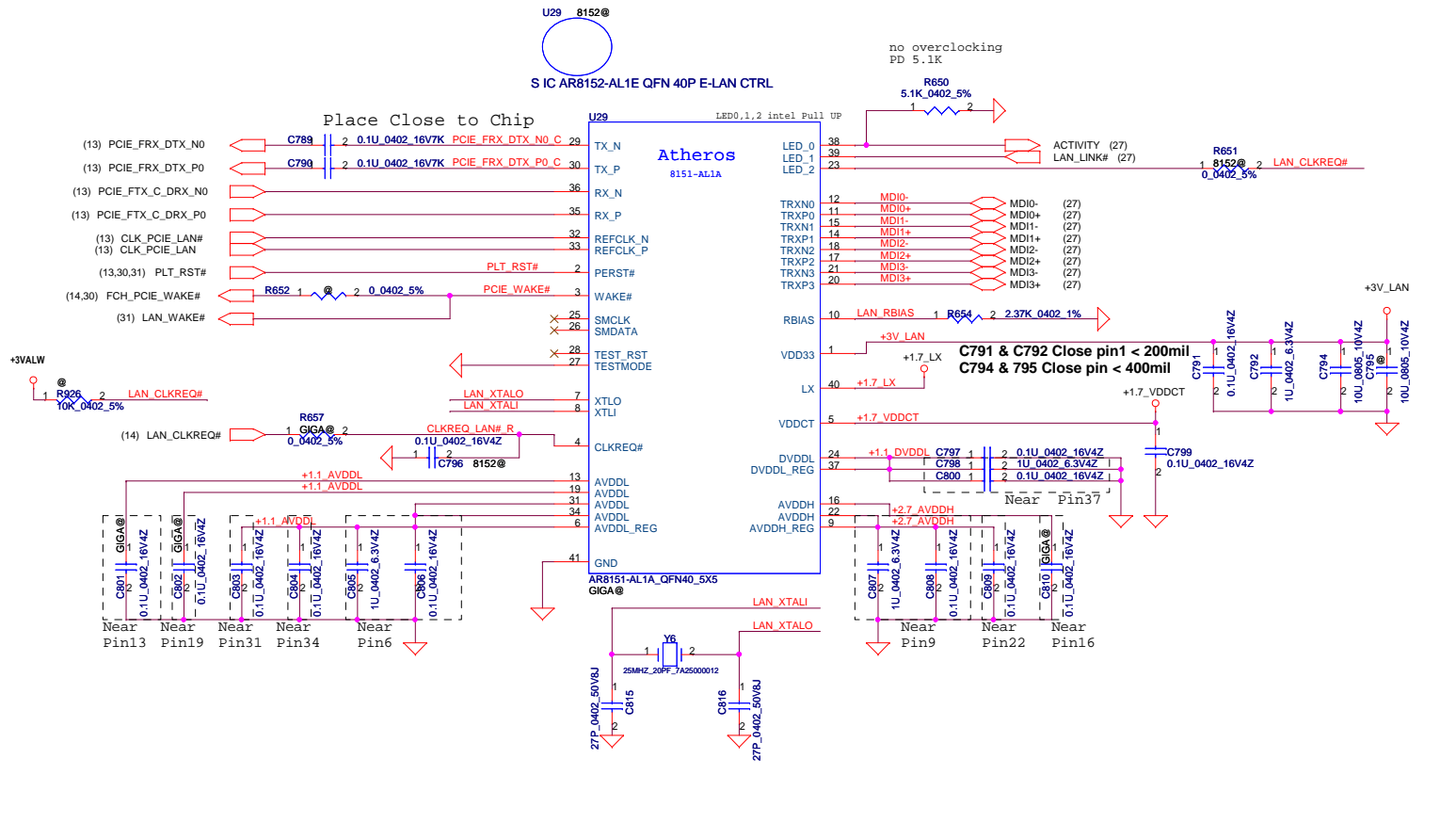


Atheros request can't disable LAN power



Power On strapping

Pin	Description	Chip Default
LED0	H:Over Clock Enable L:Over Clock Disable *	H
LED2	H:SWR Switch mode regulator Select * AR8151 Pin23=LED2. AR8152, Pin23 is CLKREQ	--



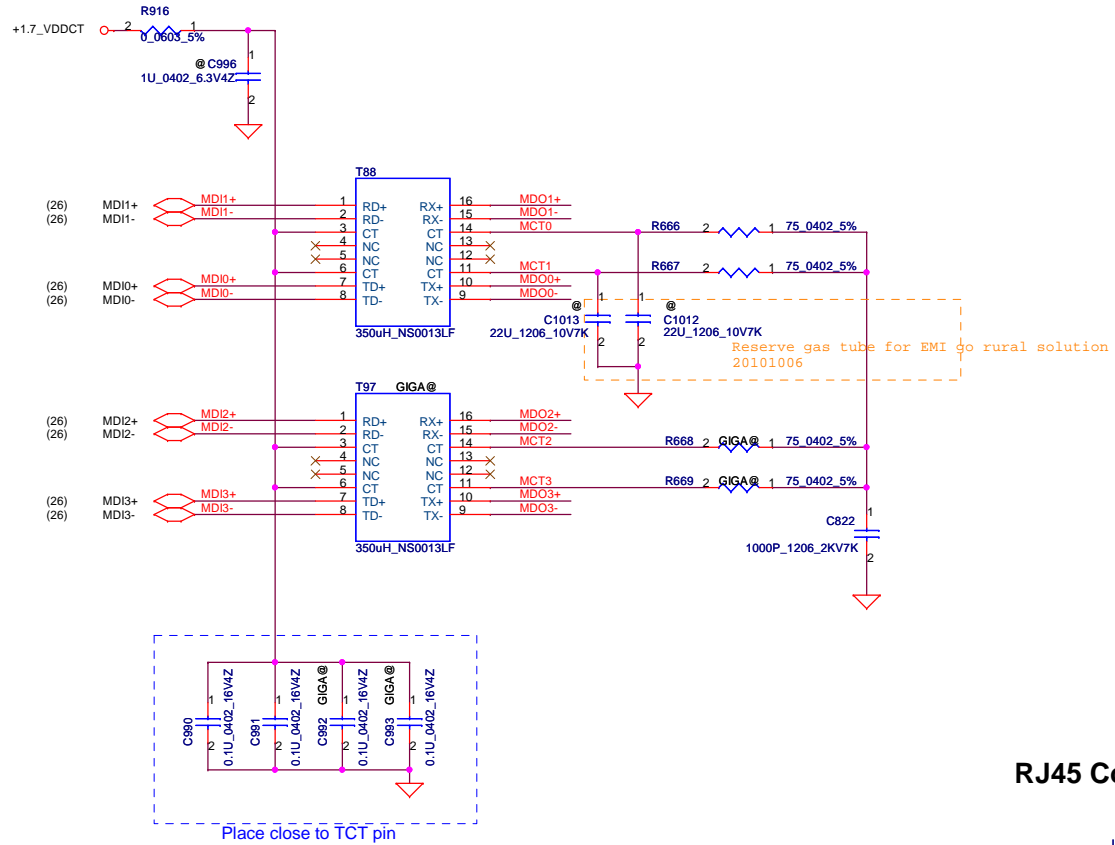
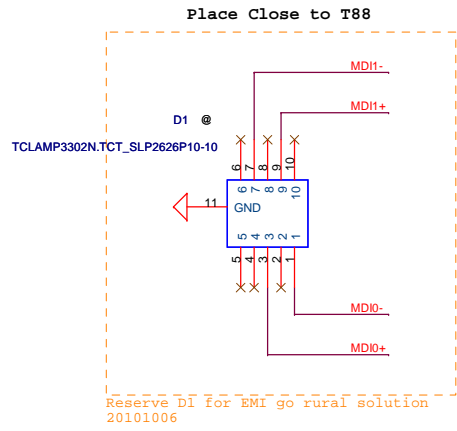
8152 no mount MDI3+,MDI3-,MDI2-,MDI2+ resistor and cap

	Pin4	Configure		Pin23	Configure
		R657	C796		
AR8152	VDDCT_REG		*	CLKREQn	*
AR8151	CLKREQn	*		LED [ 2 ]	

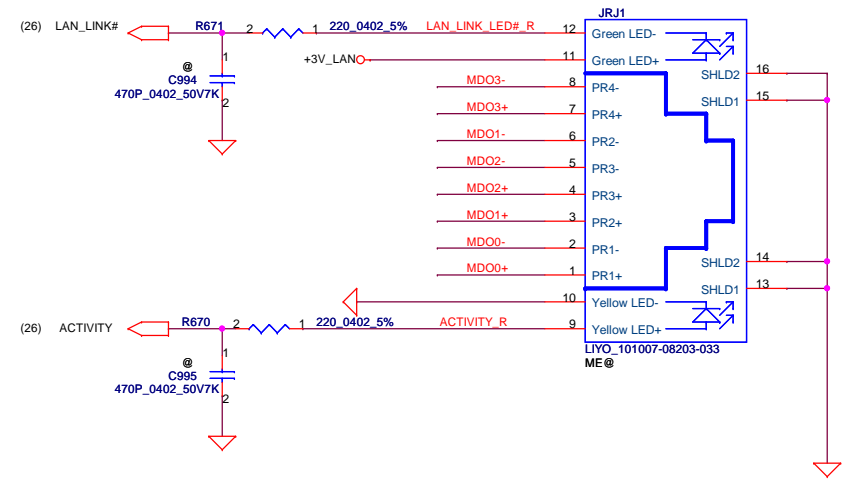
Security Classification	Compal Secret Data	
Issued Date	2010/06/30	Deciphered Date
		2012/06/30

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Title	LAN-AR8151/8152	
Size Custom	Document Number	Rev
	LA6755P/7P	1.0
Date:	Tuesday, November 30, 2010	Sheet 26 of 48

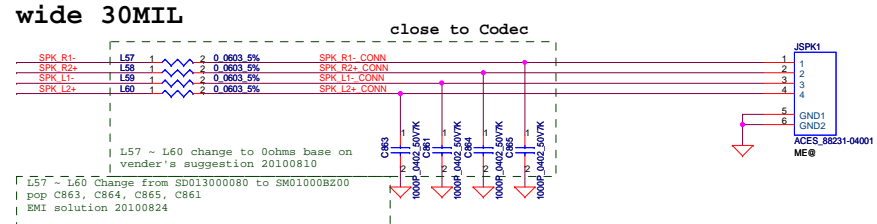
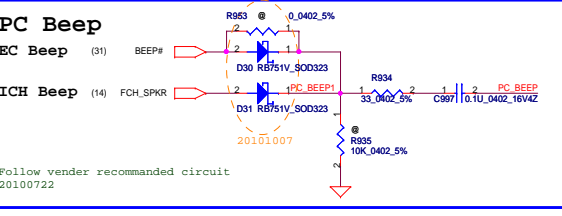
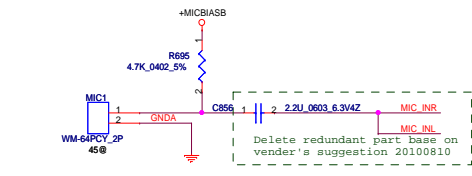
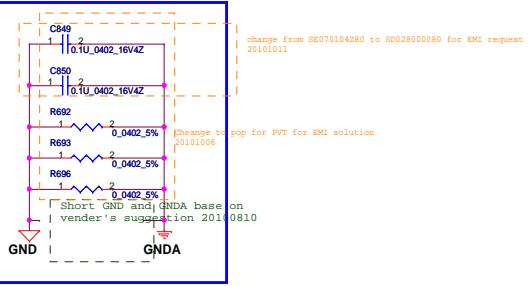
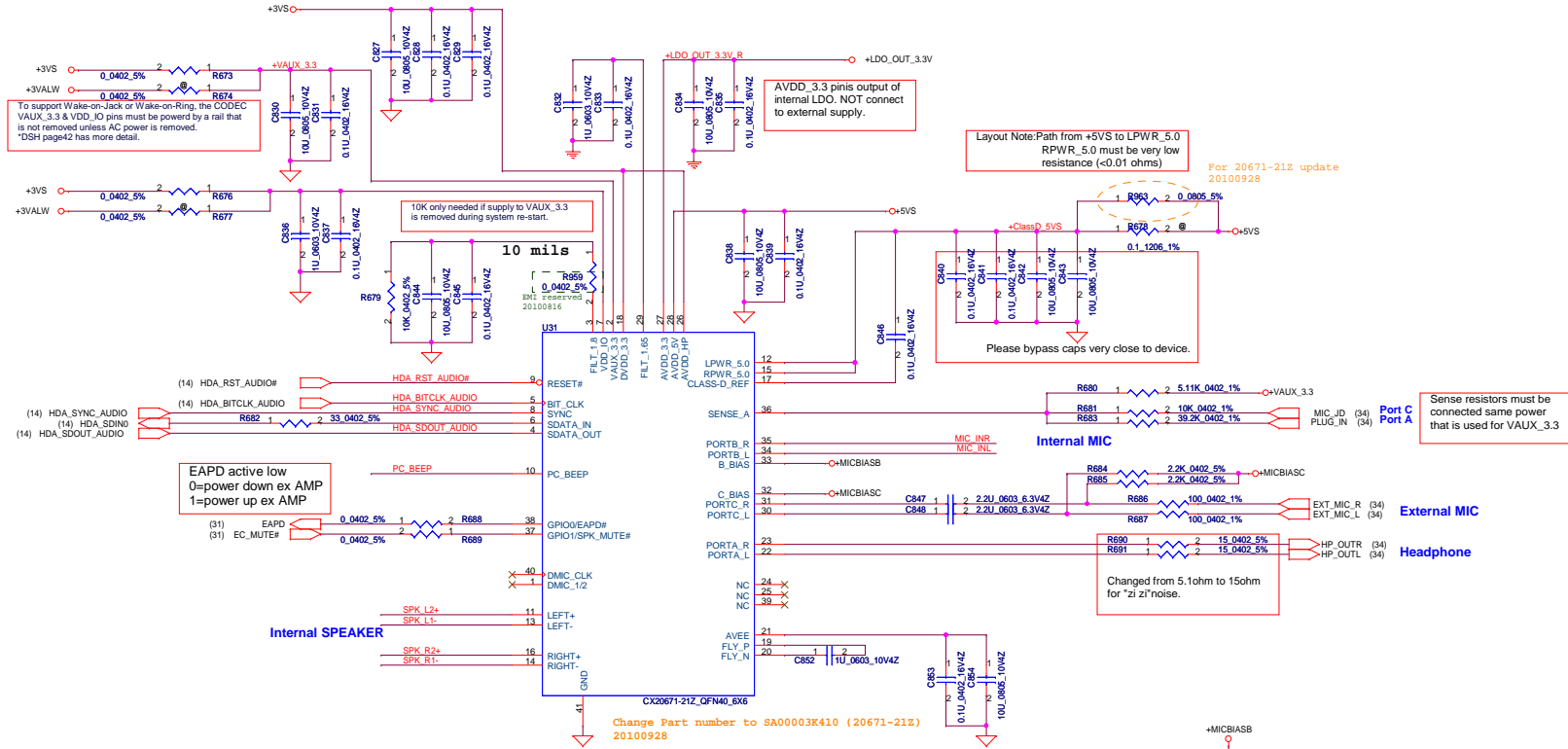
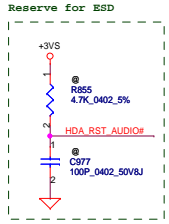
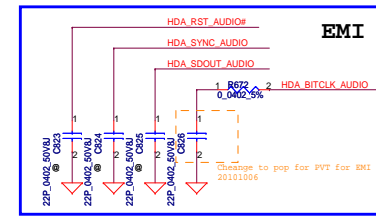


### RJ45 Conn.

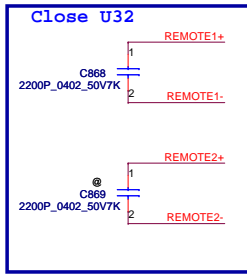


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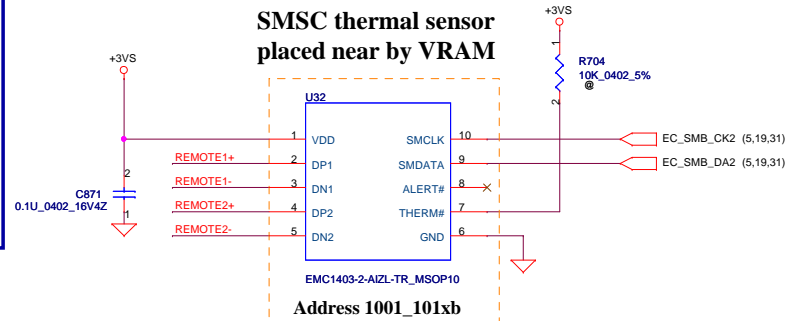
**CX20671**  
**High Definition Audio Codec SoC**  
**With Integrated Class-D Stereo**  
**Amplifier.**  
 An integrated 5 V to 3.3 V Low-dropout  
 voltage regulator (LDO).  
 An integrated 3.3 V to 1.8V Low-dropout  
 voltage regulator (LDO).



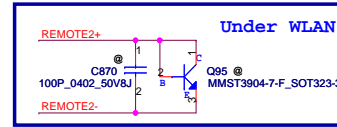
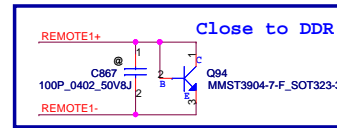
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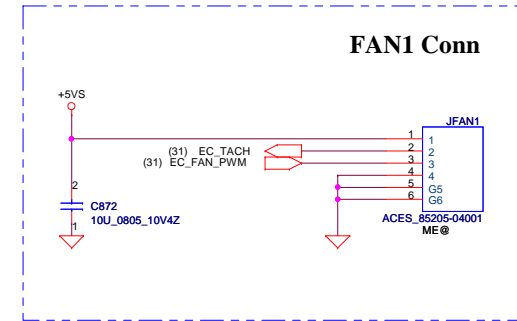
**SMSC thermal sensor placed near by VRAM**



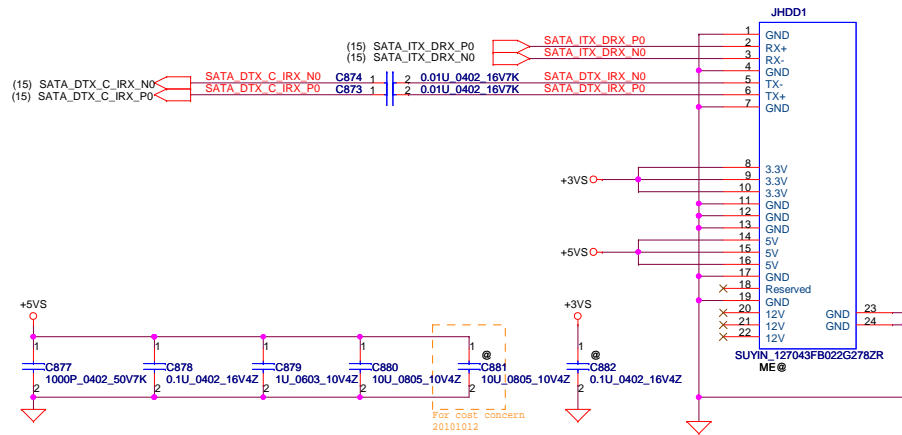
Change from SA000029210 to SA000046C00 for main source



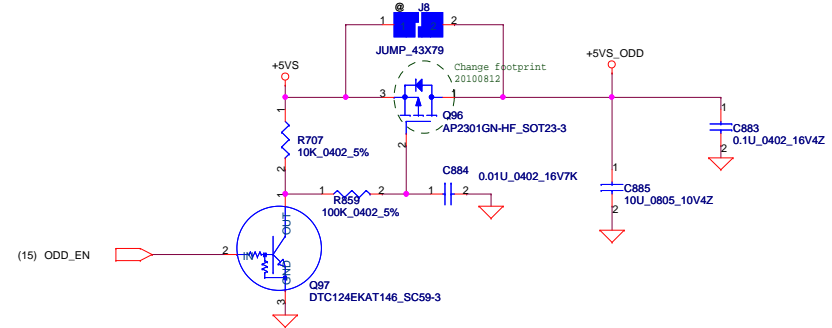
REMOTE1,2+/-:  
Trace width/space:10/10 mil  
Trace length:<8"



**SATA HDD Conn.**

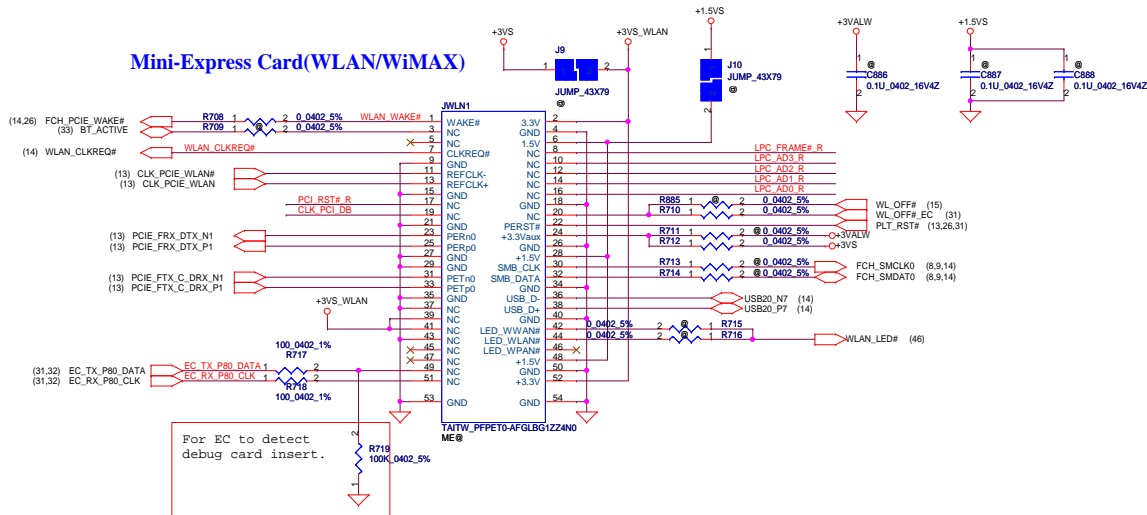


**ODD Power Control**



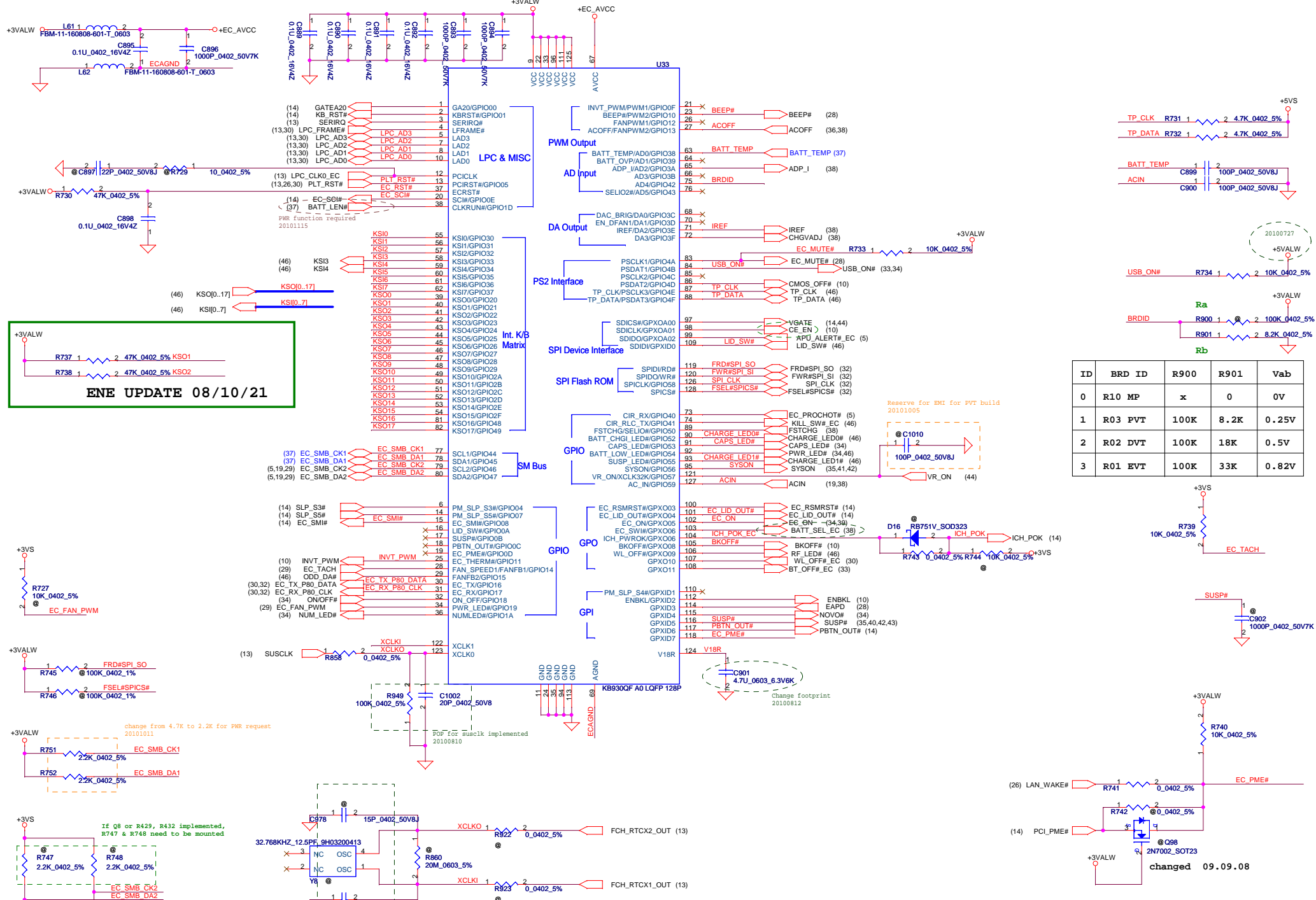
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Issued Date	2010/06/30	Deciphered Date	2012/06/30	HDD/ODD/EMC1403/FAN	
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# Mini-Express Card for WLAN/WiMAX(Half)



**Reserve for SW mini-pcie debug card.  
Series resistors closed to KBC side.**

LPC_FRAME#_R	R720	1	2	0.0402_5%	LPC_FRAME#	LPC_FRAME# (13,31)
LPC_AD3_R	R721	1	2	0.0402_5%	LPC_AD3	LPC_AD3 (13,31)
LPC_AD2_R	R722	1	2	0.0402_5%	LPC_AD2	LPC_AD2 (13,31)
LPC_AD1_R	R723	1	2	0.0402_5%	LPC_AD1	LPC_AD1 (13,31)
LPC_AD0_R	R724	1	2	0.0402_5%	LPC_AD0	LPC_AD0 (13,31)
PCI_RST#_R	R725	1	2	0.0402_5%	PCI_RST#	PCI_RST# (13)
CLK_PCI_DB					CLK_PCI_DB	CLK_PCI_DB (13)

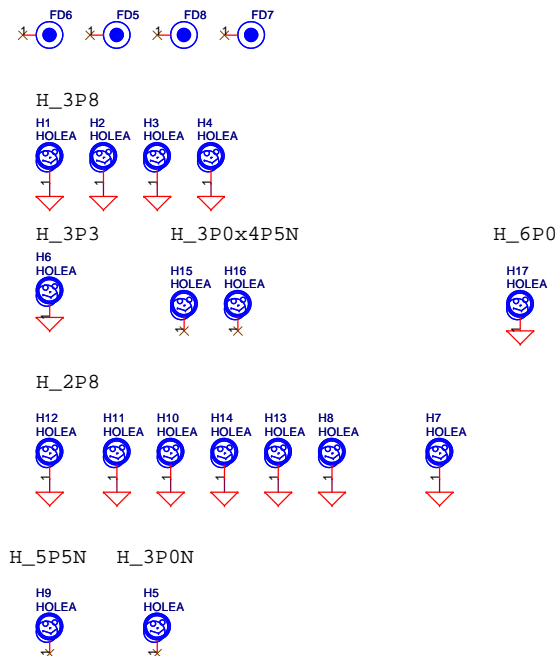
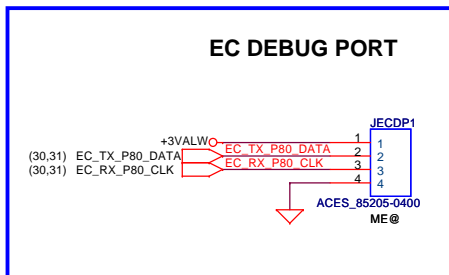
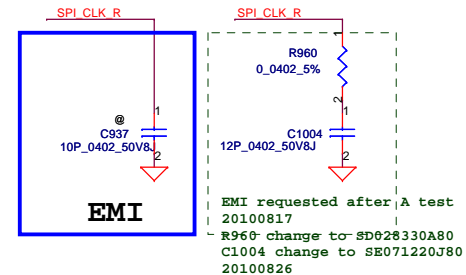
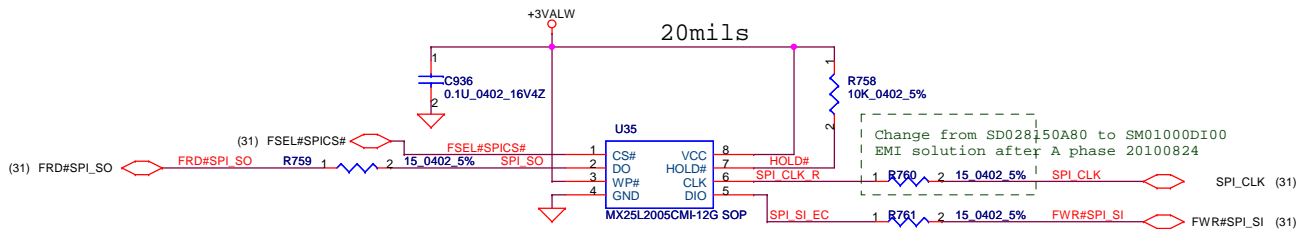


**ENE UPDATE 08/10/21**

ID	BRD ID	R900	R901	Vab
0	R10 MP	x	0	0V
1	R03 PVT	100K	8.2K	0.25V
2	R02 DVT	100K	18K	0.5V
3	R01 EVT	100K	33K	0.82V

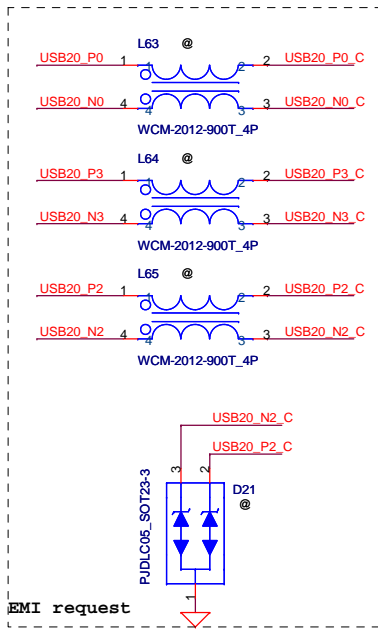
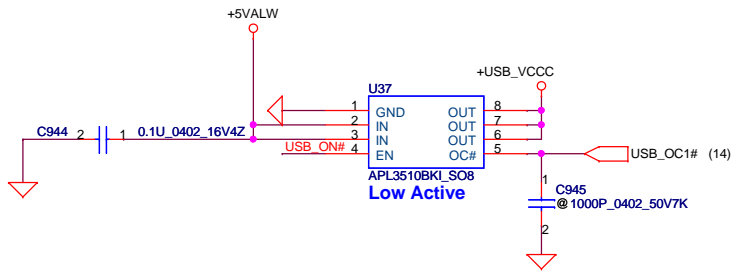
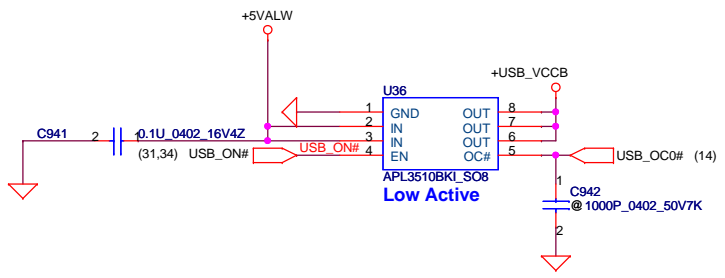
Security Classification		Compal Secret Data		Title	
Issued Date	2010/06/30	Deciphered Date	2012/06/30	BIOS & EC I/O Port	
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**FOR EC 128KB SPI ROM  
(150mil PACKAGE)  
SA00003FL10  
SA00003JD00**

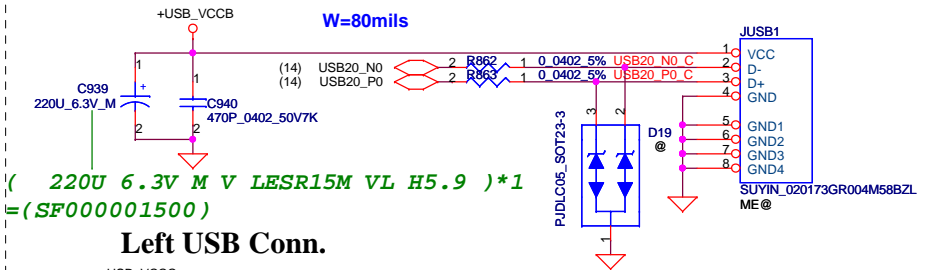


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				1.0	

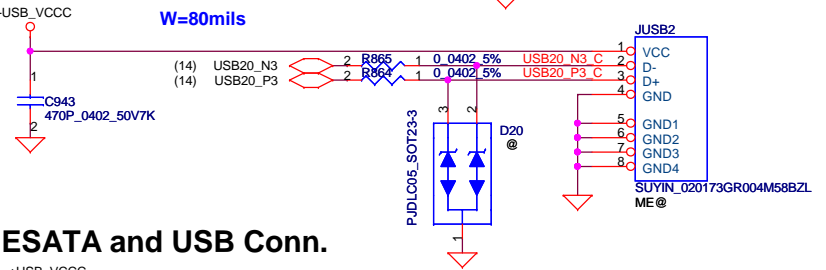




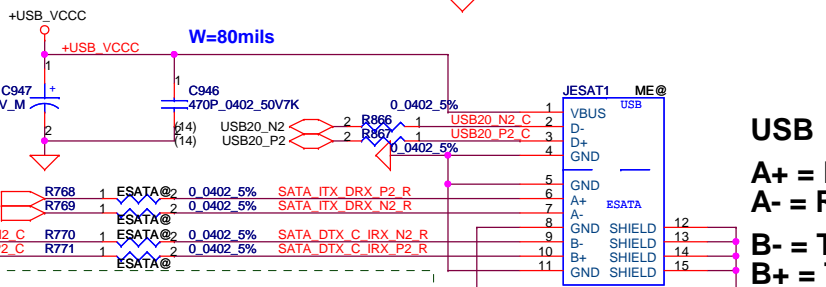
**Left USB Conn.**



**Left USB Conn.**

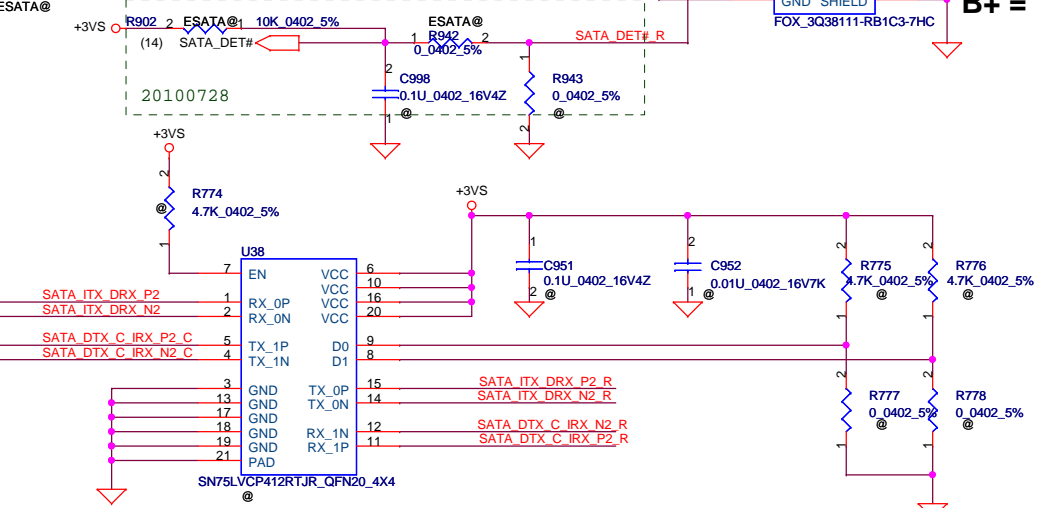
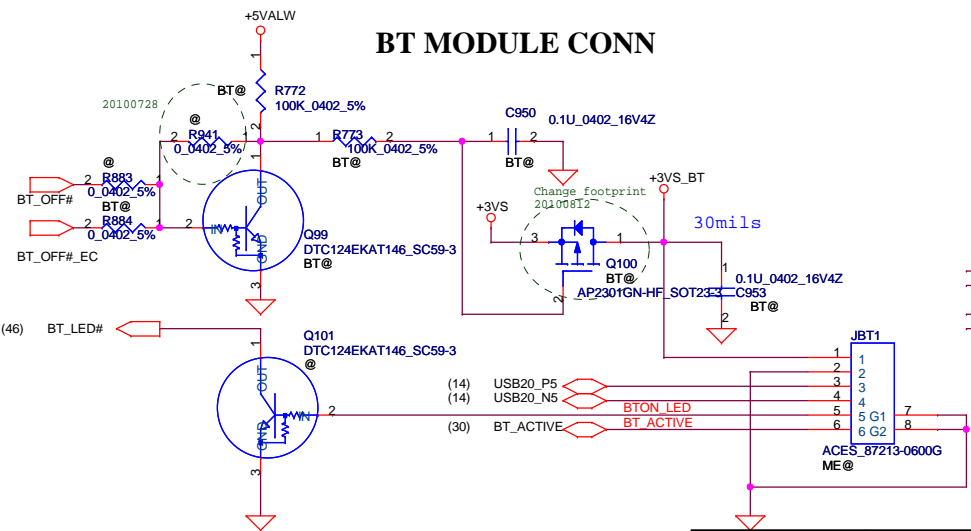


**ESATA and USB Conn.**



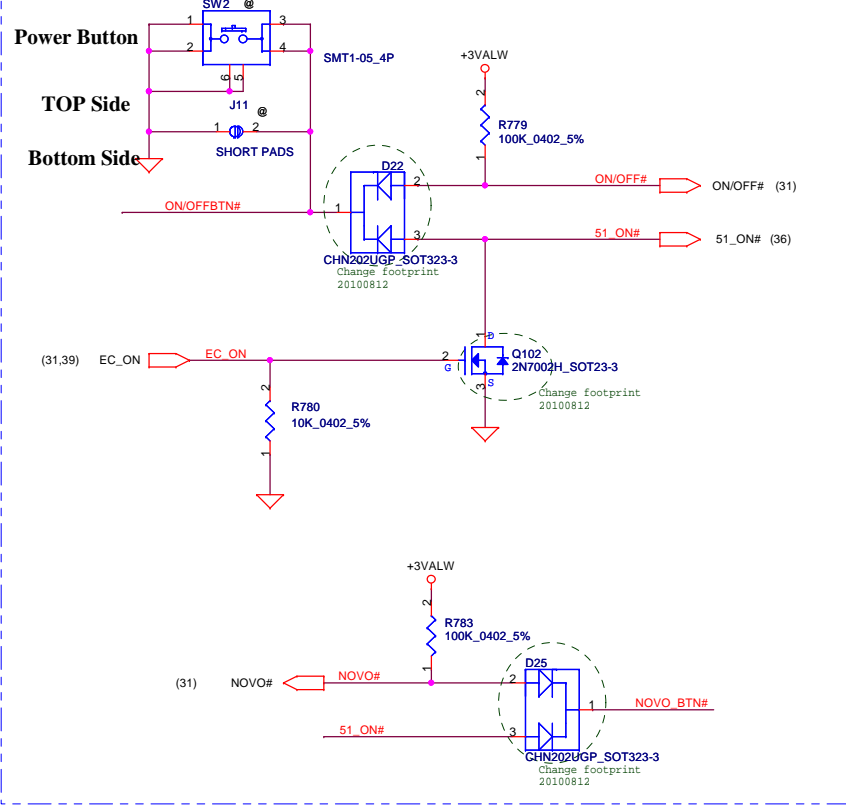
**USB**  
**A+ = RXP**  
**A- = RXN**  
**B- = TXN**  
**B+ = TXP**

**BT MODULE CONN**

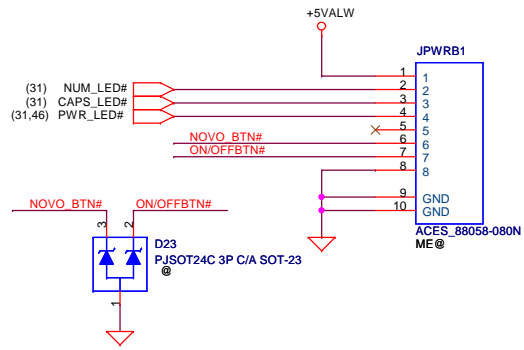


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Size	Document Number	Rev		Date	
Custom	LA6755P/7P	1.0		Tuesday, November 30, 2010	
				Sheet 33 of 48	

# ON/OFF switch

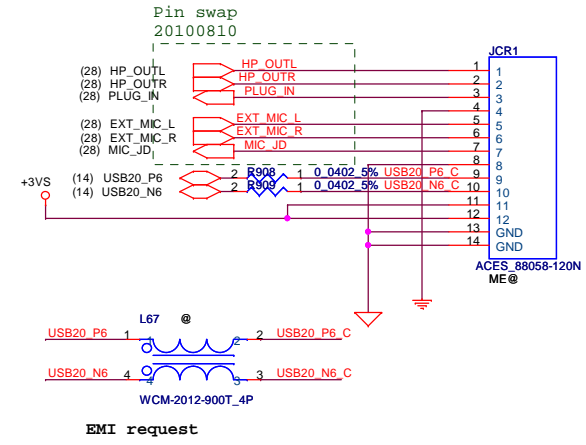


# Power Button Board Conn. 8pin

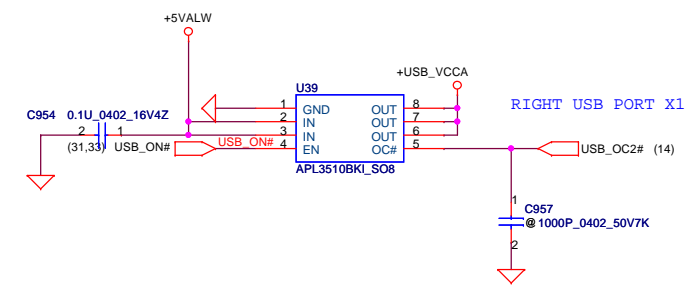


*EMI REQUEST 1ST = SCA00000E00  
2ST = SCA00000R00*

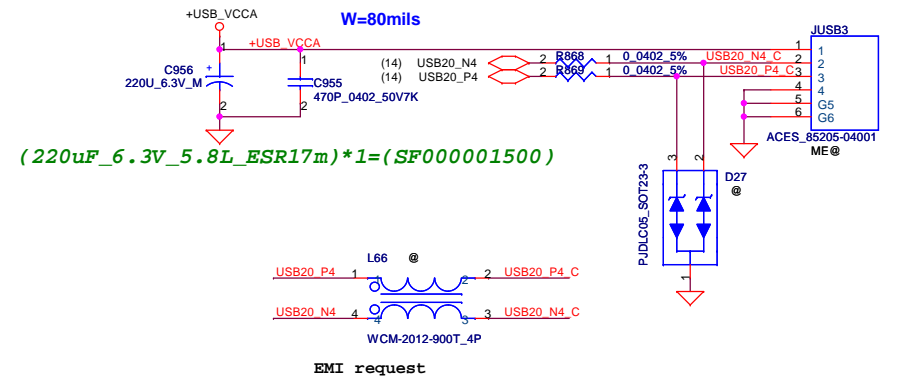
# Card Reader/Audio Jack SB CONN



EMI request

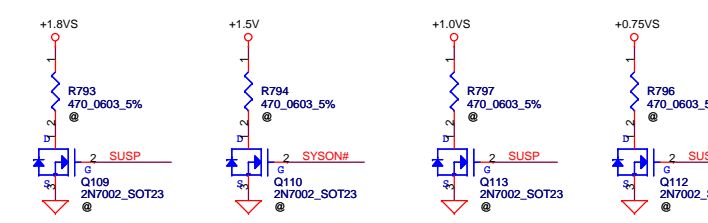
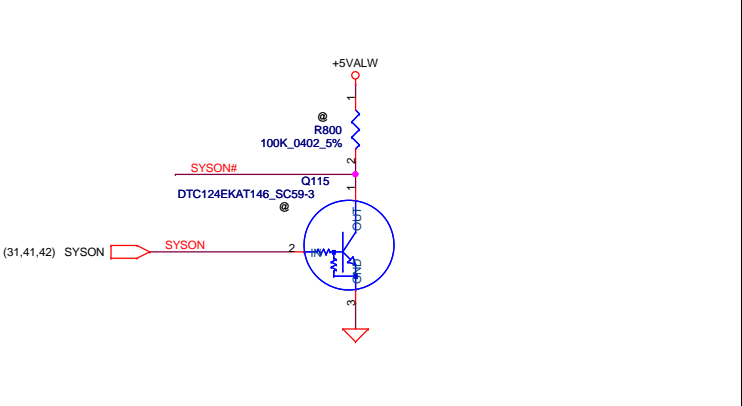
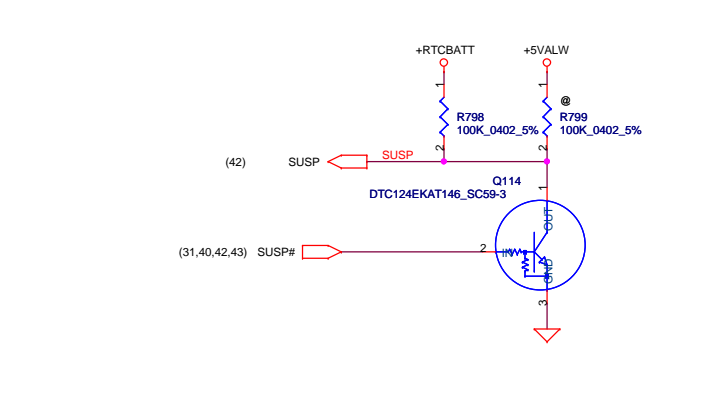
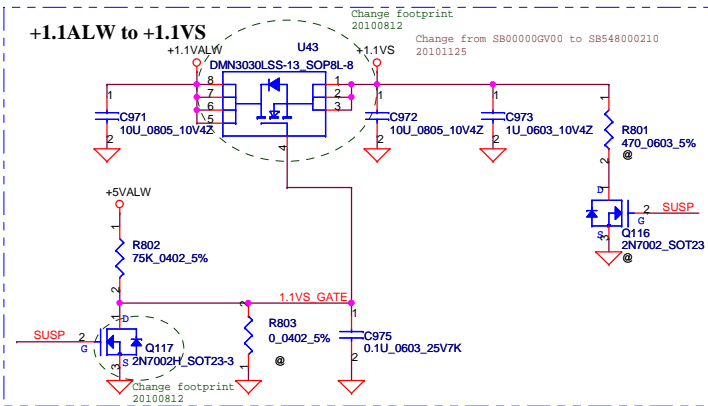
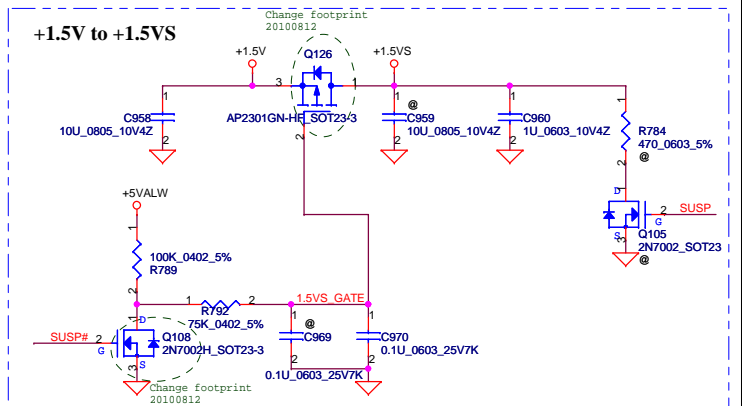
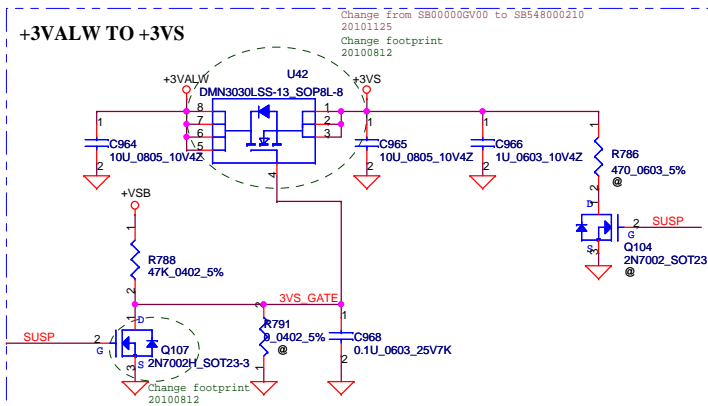
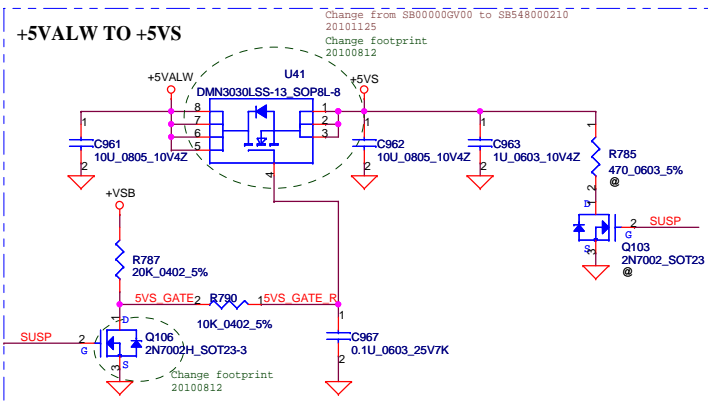


# Right USB Conn.



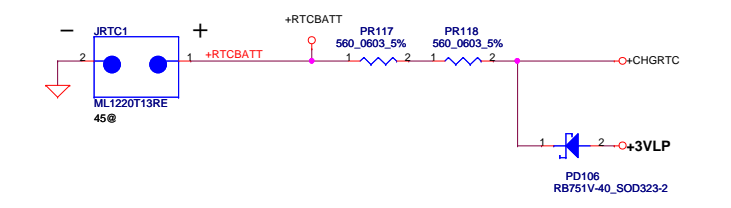
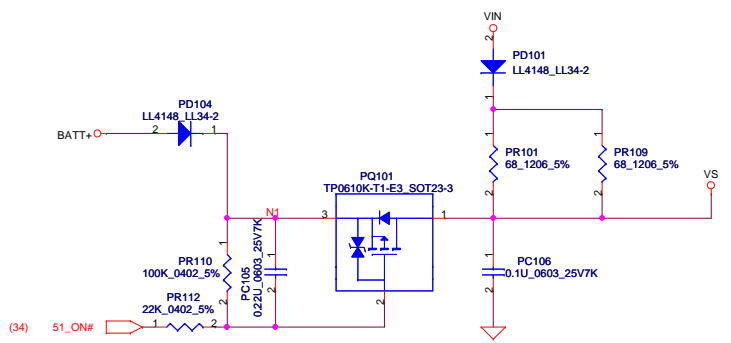
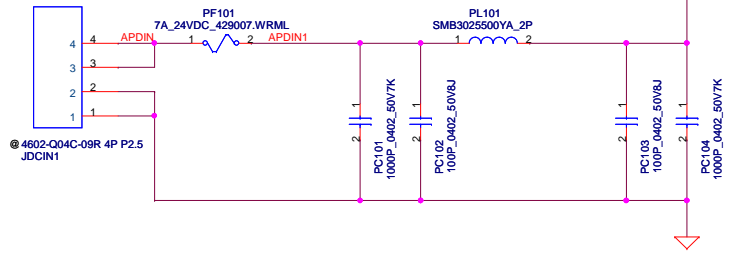
EMI request

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Size Custom	Document Number	LA6755P/7P		Rev 1.0
Date:	Tuesday, November 30, 2010	Sheet	34 of 48	

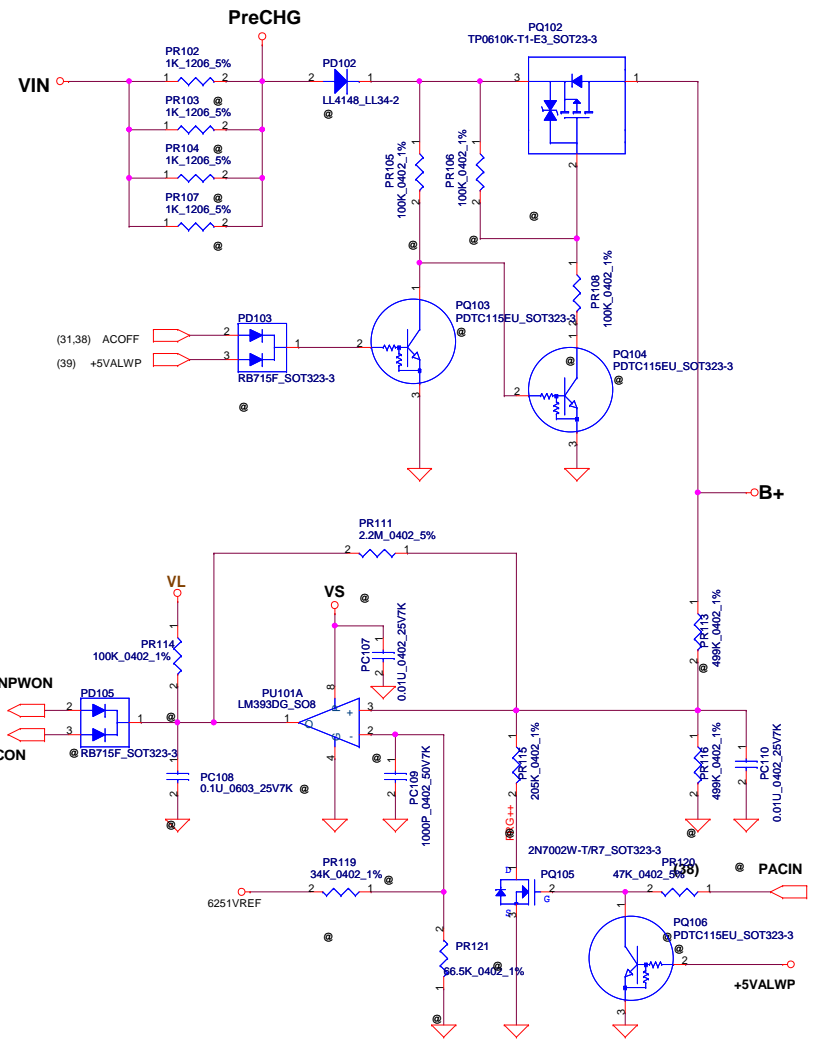


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/06/30	Deciphered Date	2012/06/30	Title	
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Size	Document Number	LA6755P/7P		Rev	1.0
Date	Tuesday, November 30, 2010	Sheet	35	of	48

DC030006J00



Precharge detector  
15.97V/14.84V FOR  
ADAPTOR



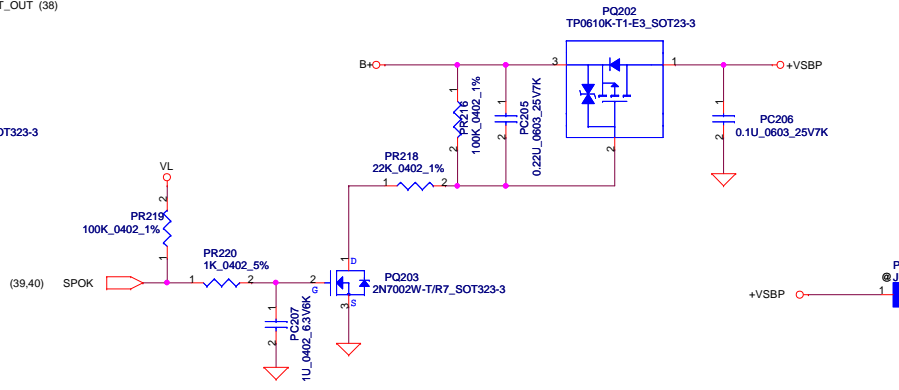
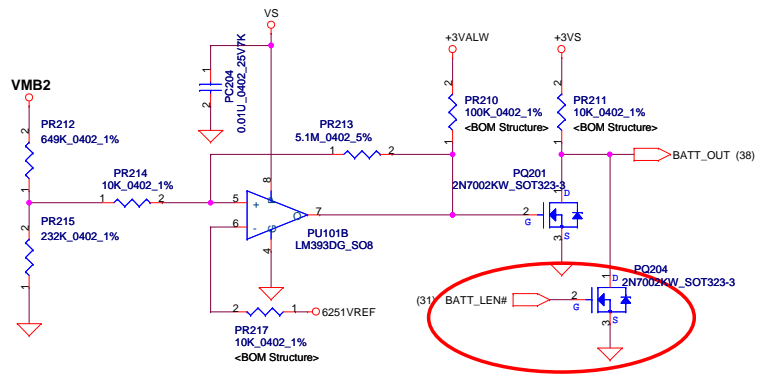
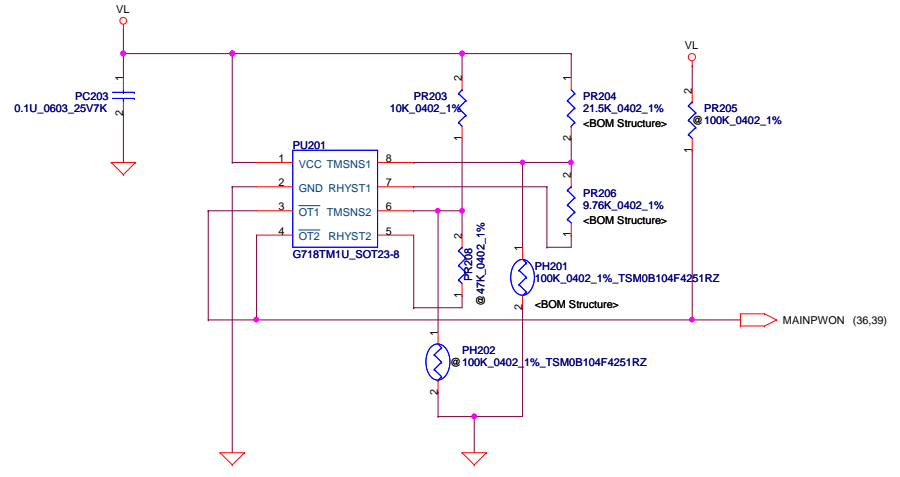
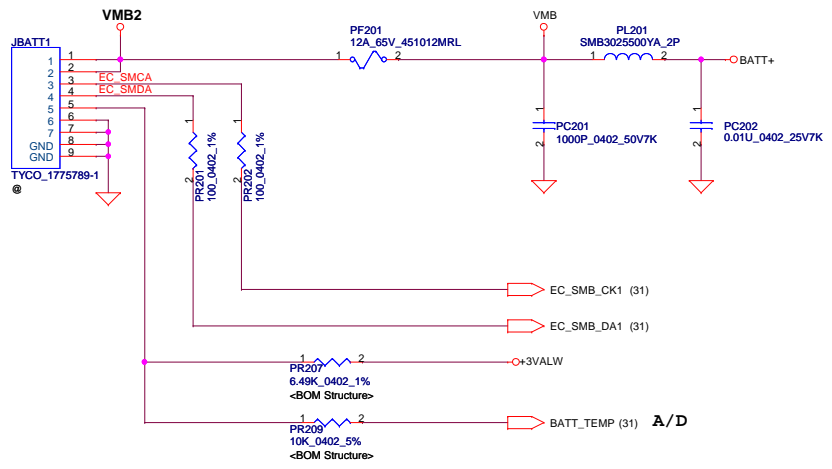
ACIN

Precharge detector			
	Min.	typ.	Max.
L-->H	14.991V	15.381V	15.782V
H-->L	13.860V	14.247V	14.621V

BATT ONLY

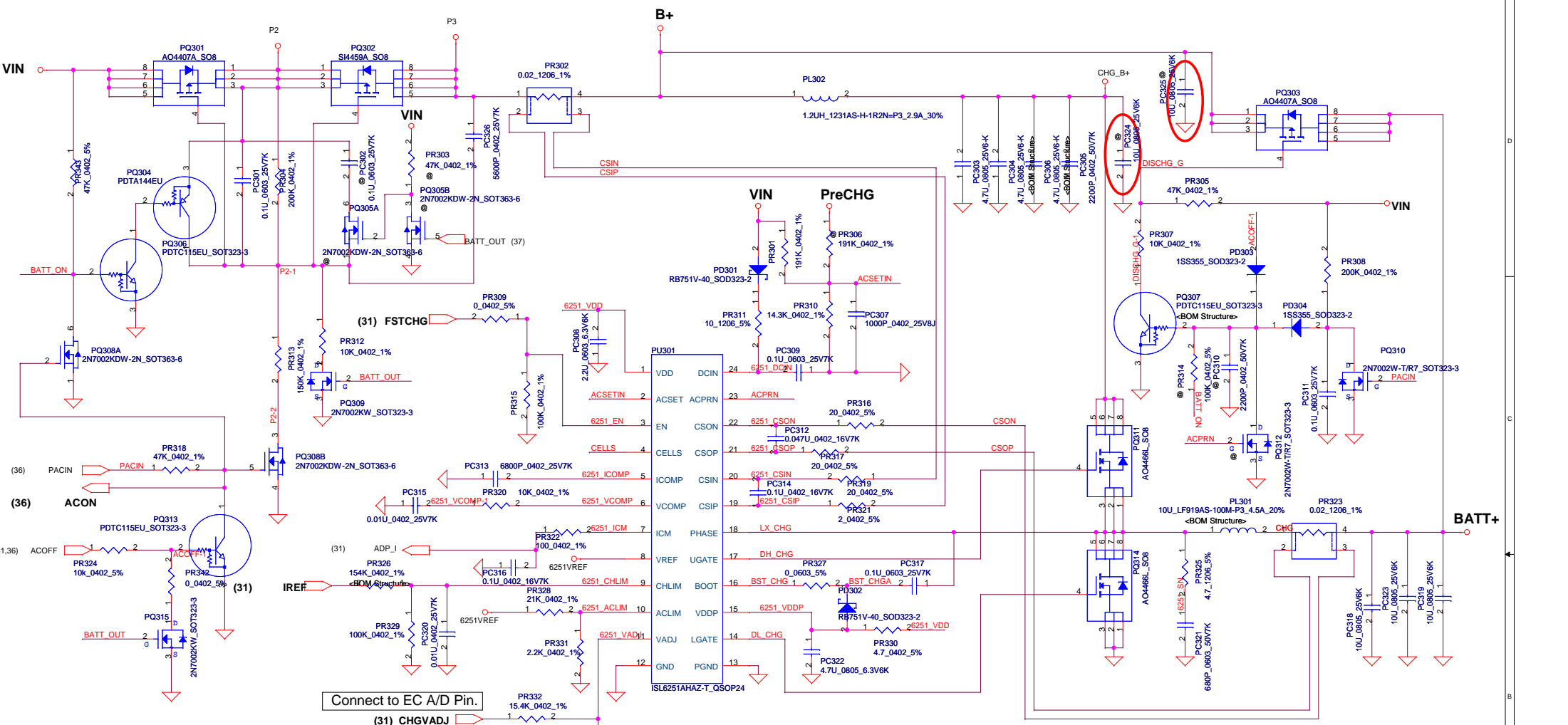
Precharge detector			
	Min.	typ.	Max.
L-->H	7.196V	7.349V	7.505V
H-->L	6.138V	6.214V	6.056V

PH1 under CPU bottom side :  
 CPU thermal protection at 92 degree C  
 Recovery at 56 degree C



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		2012/06/30
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<b>Compal Electronics, Inc.</b>		
<b>BATTERY CONN/OTP</b>		
Title	Document Number	Rev
	<b>PAWGC</b>	0.1
Date:	Tuesday, November 30, 2010	Sheet 37 of 47



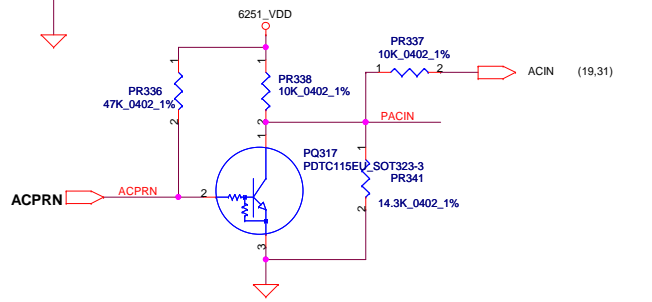
Connect to EC A/D Pin.  
(31) CHGVADJ

CHGVADJ=(Vcell-4)/0.10627	
Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

CC=0.25A-3A  
IREF=1.016\*Icharge  
IREF=0.254V-3.048V  
VCHLIM need over 95mV

**DIS CP mode (65W\*85%)**  
 $V_{aLim}=2.39 \cdot ((2.2K/152K) + (2.2K/152K + 21K/152K)) = 0.25136V$   
 $linput = (1/0.02) \cdot ((0.05 \cdot V_{aLim}) / 2.39 + 0.05)$   
 where  $V_{aLim} = 0.25136V$ ,  $linput = 2.76293A$   
**PR328=21K**  
**PR331=2.2K**  
**PR302=20mohm**

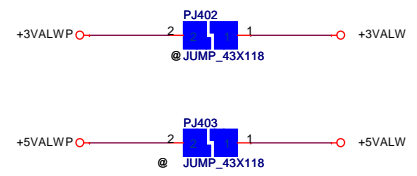
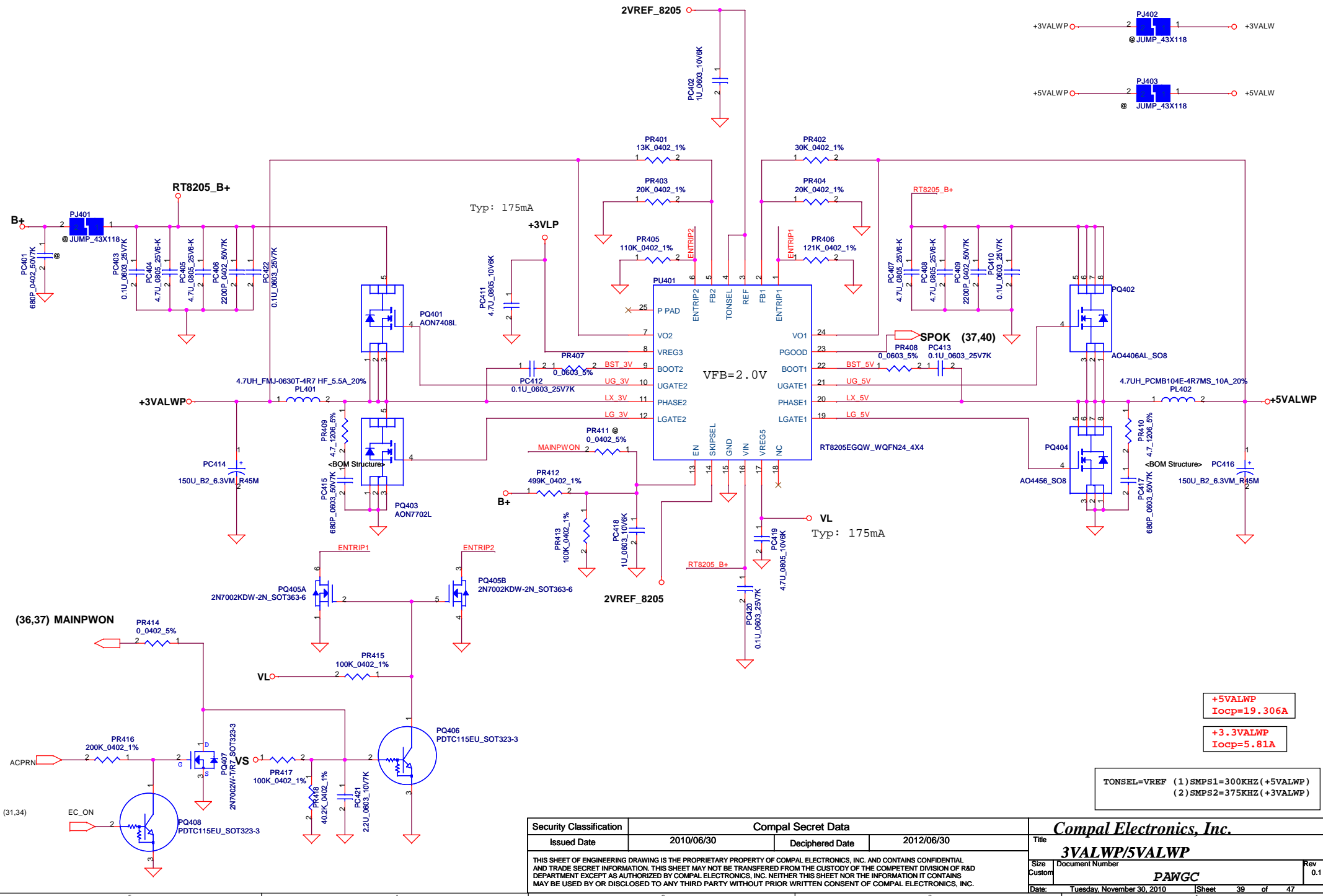
**UMA CP mode (40W\*85%)**  
 $V_{aLim} = 2.39 \cdot ((31.6K/152K) / (31.6K/152K + 12.1K/152K)) = 1.6731V$   
 $linput = (1/0.05) \cdot ((0.05 \cdot V_{aLim}) / 2.39 + 0.05)$   
 where  $V_{aLim} = 1.6731V$ ,  $linput = 1.7A$   
**PR328=12.1K(SD034121280)**  
**PR331=31.6K(SD034316280)**  
**PR302=50mohm(SD0000C110)**



**4cell : VDD**  
**3cell : GND**

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				PAWGC	
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Note:  
 Use TPS51125 IC can remove RTC referenece LDO  
 Use TPS51427 IC must keep RTC referenece LDO



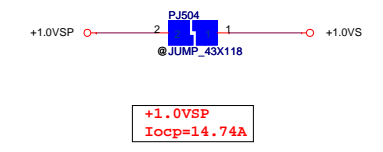
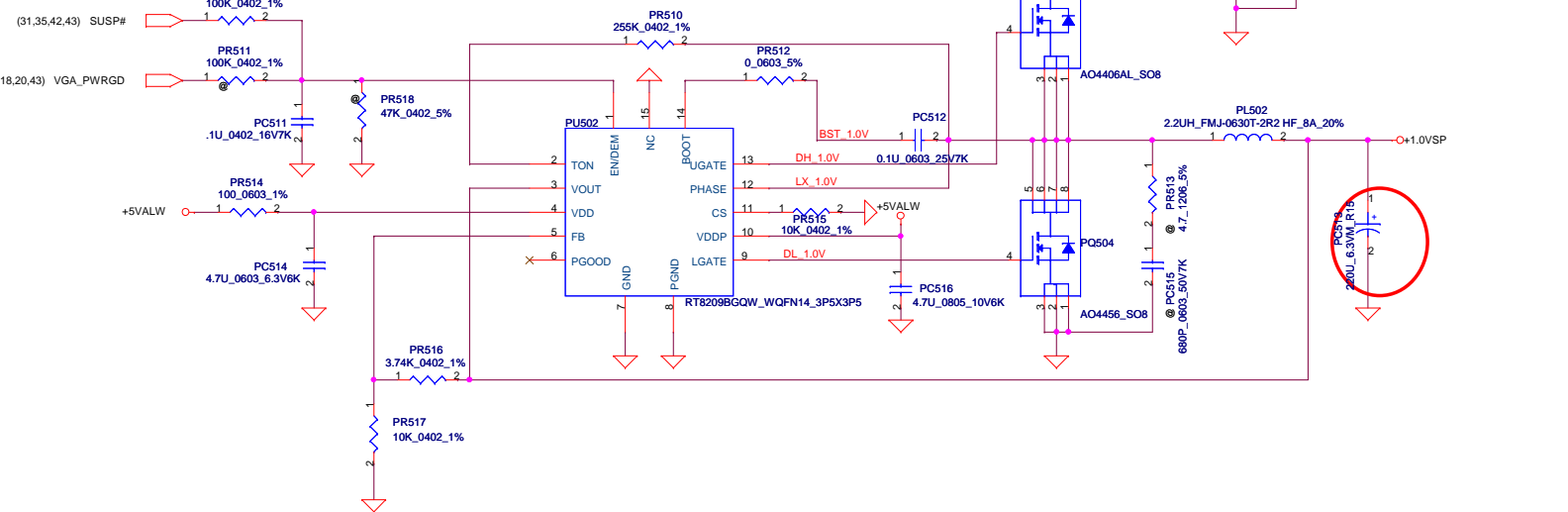
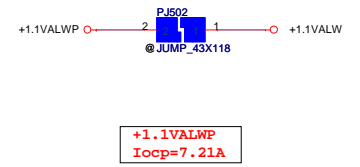
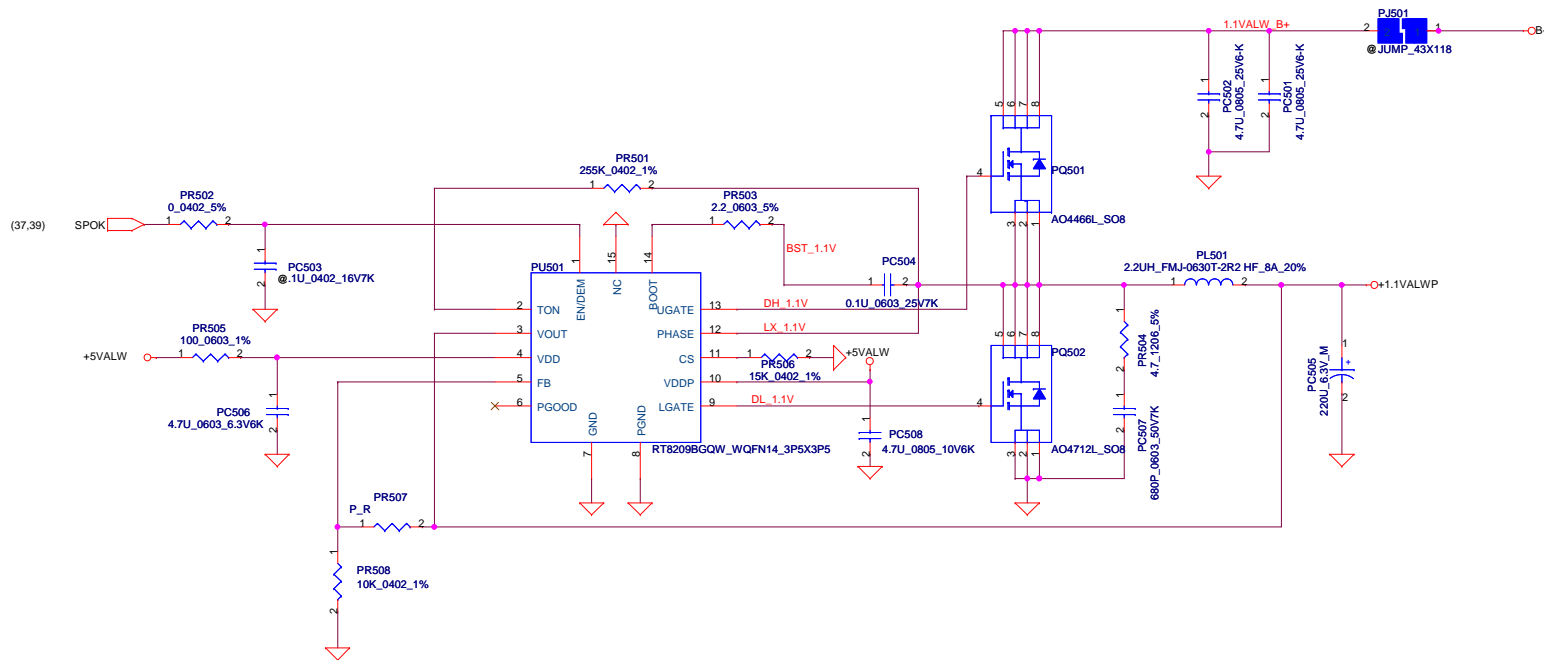
**+5VALWP**  
 Iocp=19.306A

**+3.3VALWP**  
 Iocp=5.81A

TONSEL=VREF (1) SMPs1=300KHZ (+5VALWP)  
 (2) SMPs2=375KHZ (+3VALWP)

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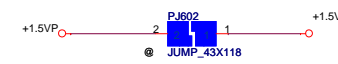
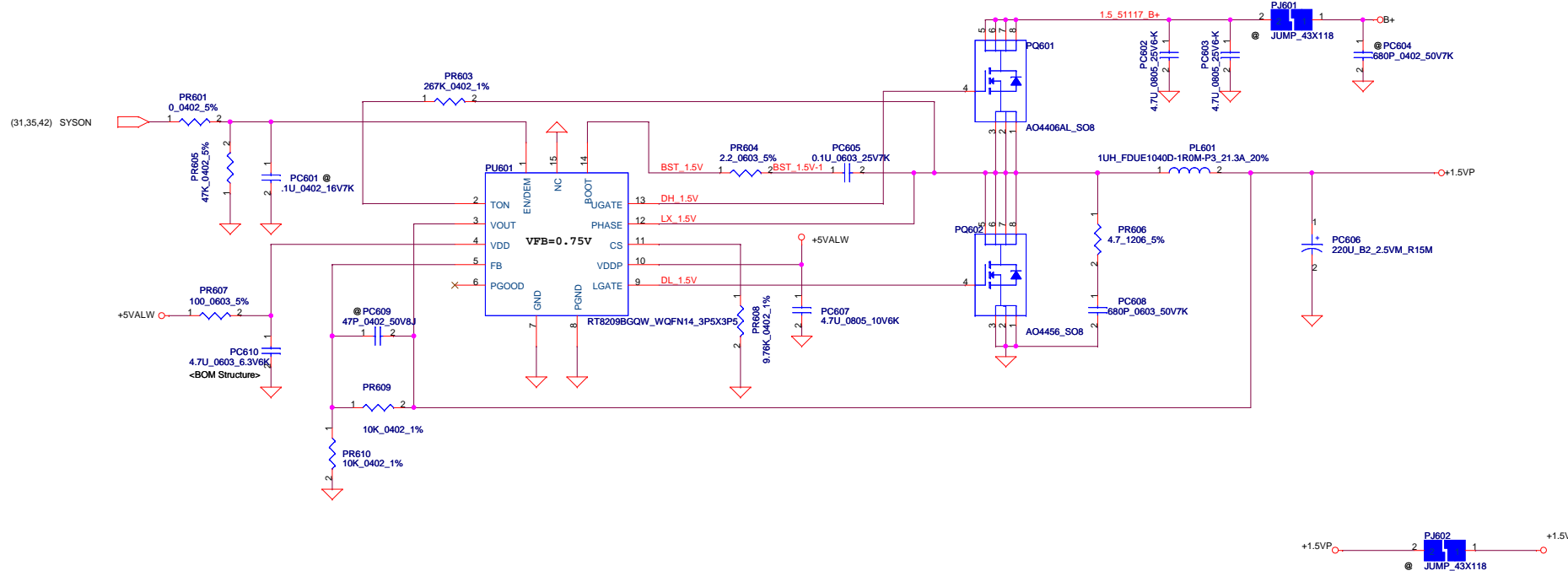
<b>Compal Electronics, Inc.</b> <b>3VALWP/5VALWP</b>		
Title	Document Number	Rev
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Custom		
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<b>Compal Electronics, Inc.</b> <b>+1.1VALWP/+1.0VSP</b>		
Title	Document Number	Rev
	PAWGC	0.1
Date:	Tuesday, November 30, 2010	Sheet 40 of 47





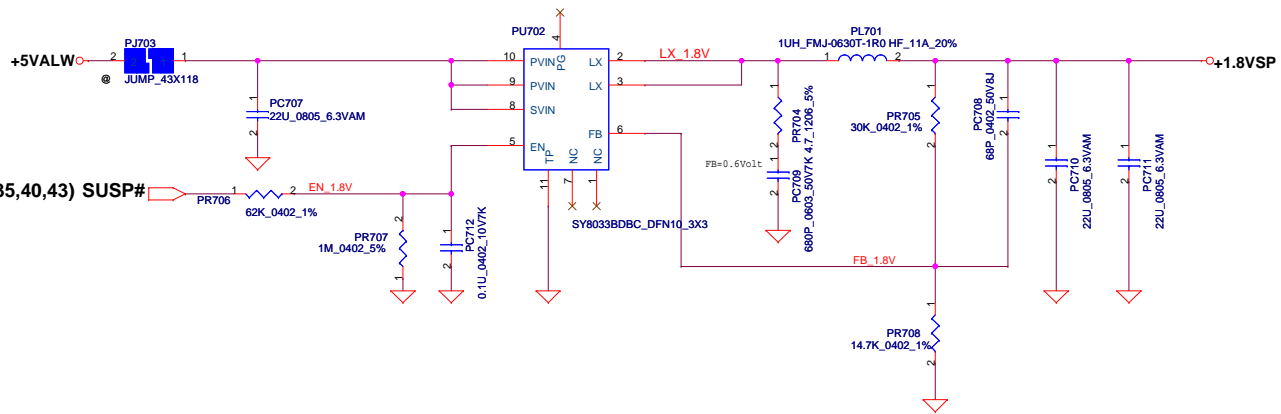
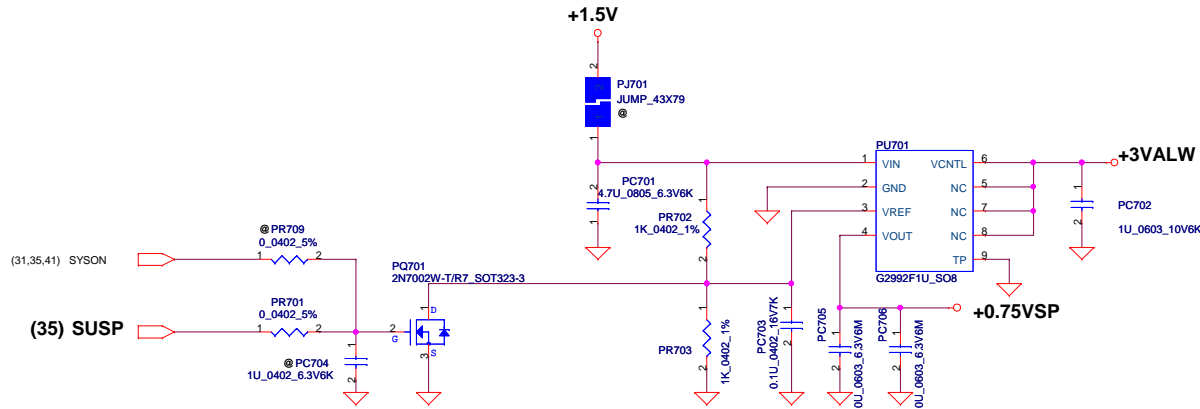
**+1.5VP**  
**I<sub>ocp</sub>=15.6A**

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Issued Date	2010/06/30	Deciphered Date	2012/06/30	1.5VP	
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				Date: Tuesday, November 30, 2010	

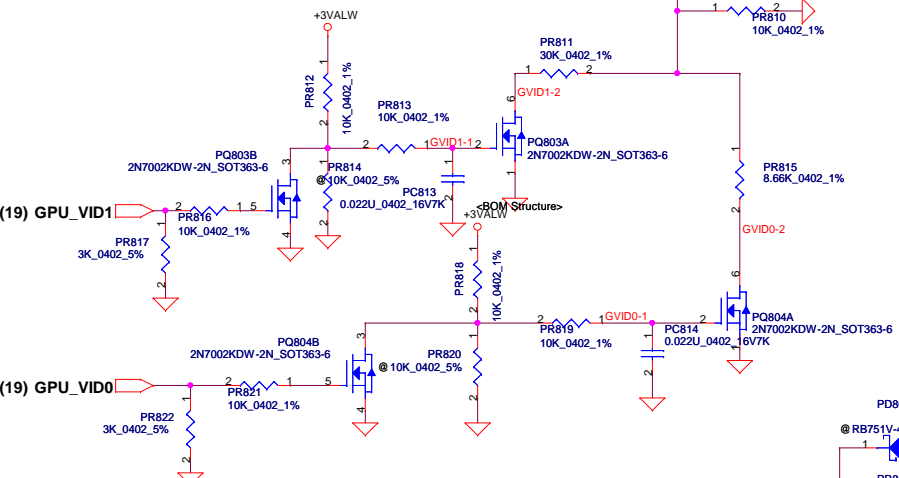
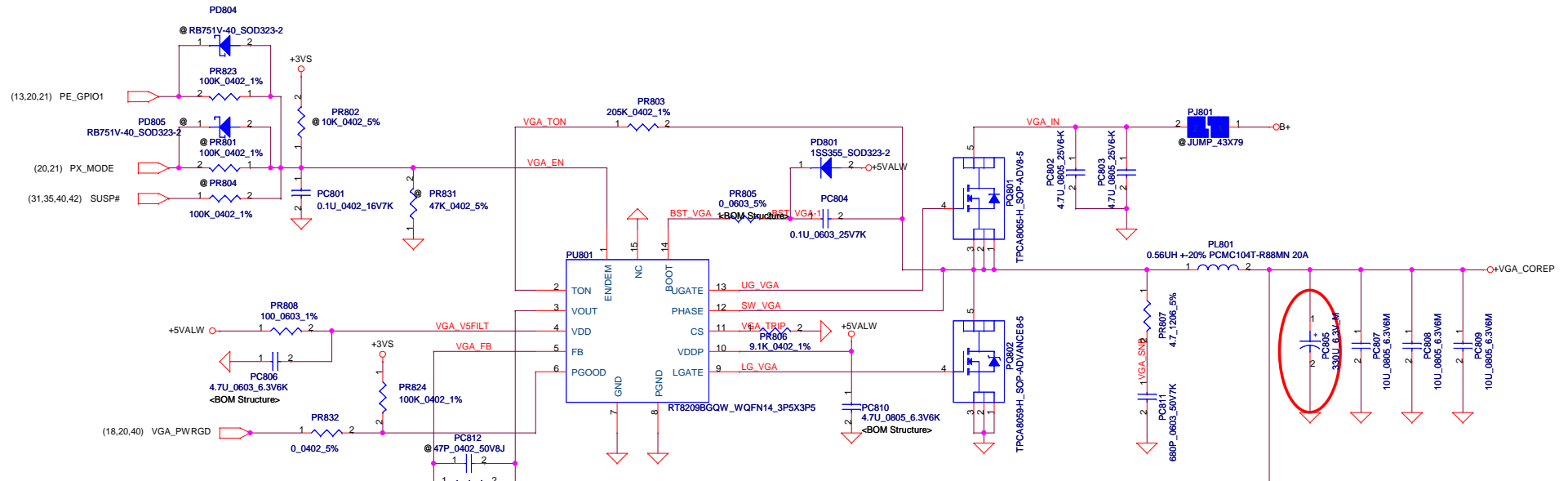
**Compal Electronics, Inc.**

**1.5VP**

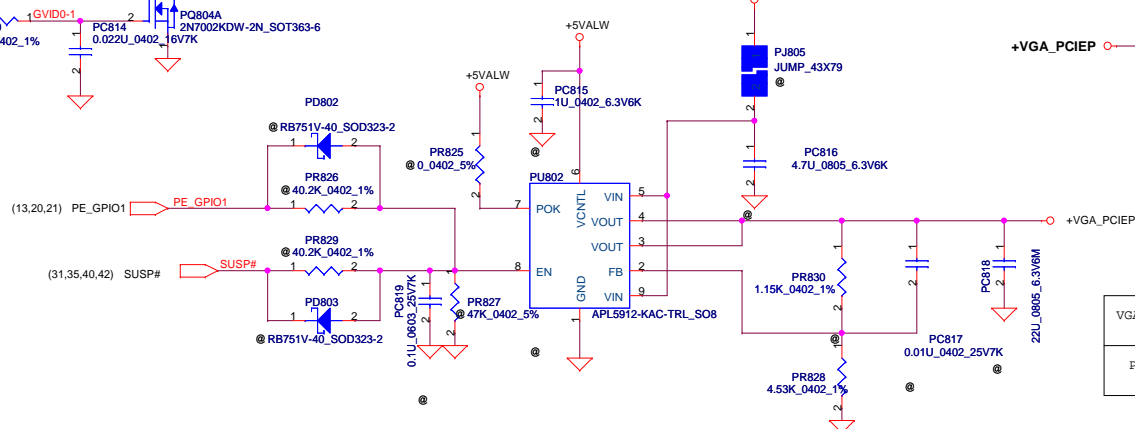
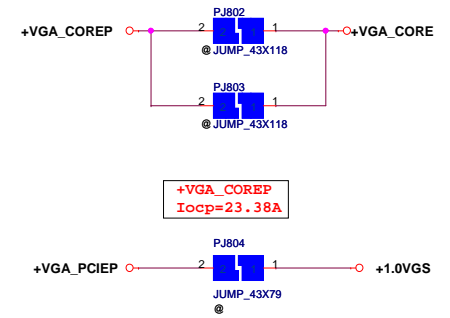
**PAWGC**



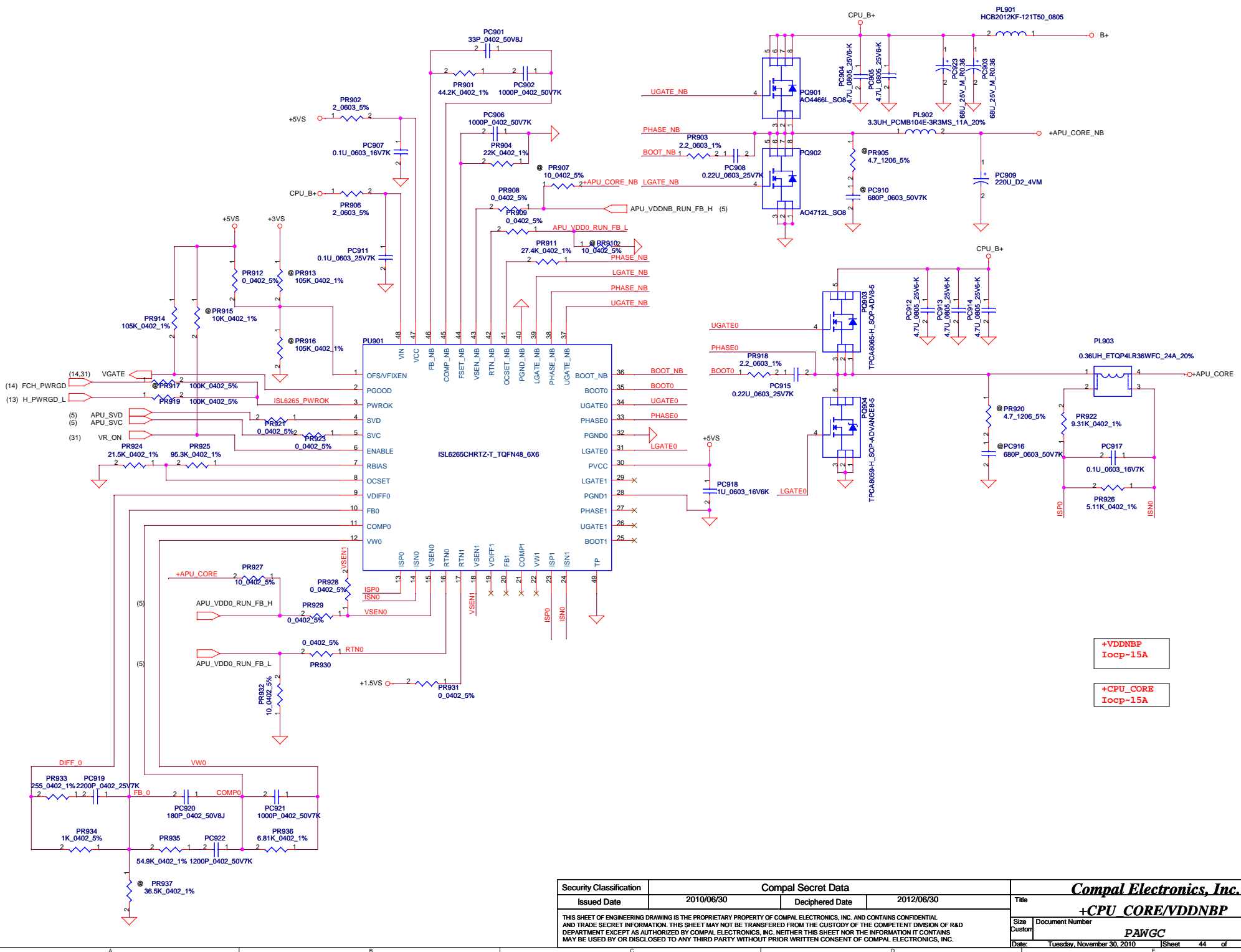
Security Classification	Compal Secret Data			<b>Compal Electronics, Inc.</b> <b>0.75VP/1.8VP</b>		
Issued Date	2010/06/30	Deciphered Date	2012/06/30			
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VGA_PWRSEL0	VGA_PWRSEL1	Robson XT
GPU_VID0	GPU_VID1	Core Voltage Level
1	1	0.9V
1	0	0.95V
0	0	1.12 V



VGA_PCIE	1.0V	1.1 V
PR828	4.53K	3K



+VDDNB  
Iocp-15A

+CPU\_CORE  
Iocp-15A

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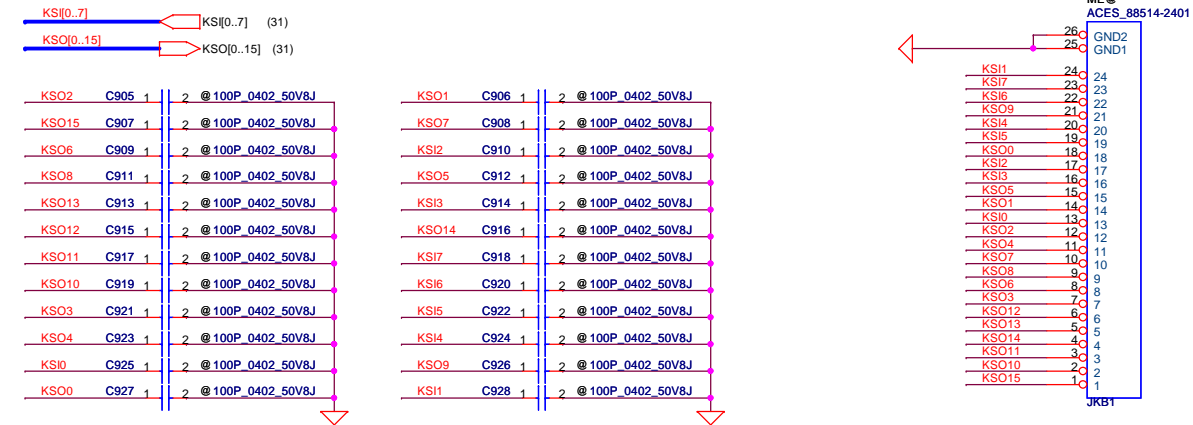
Title			
<b>Compal Electronics, Inc.</b>			
<b>+CPU CORE/VDDNB</b>			
Size	Document Number	Rev	
Custort	PAWGC	0.1	
Date:	Tuesday, November 30, 2010	Sheet	44 of 47

# Version Change List (P. I. R. List) for Power Circuit

Page #	Title	Date	Request Owner	Issue Description	Solution Description
	power sequence	2010/07/30	HW		PR701 change to 0 ohm and PC704 non mount.
	Add PU802 for AMD's request	2010/09/21	AMD		
Add PL302, PC324 and PC325 for EMC Solution.		2010/10/04	EMC		change PJ301 to PL302.
	Add PC422 for EMC Solution.	2010/10/06	EMC		
	Add PQ204 for EM6.0 battery learning function.	2010/11/12	PWR		

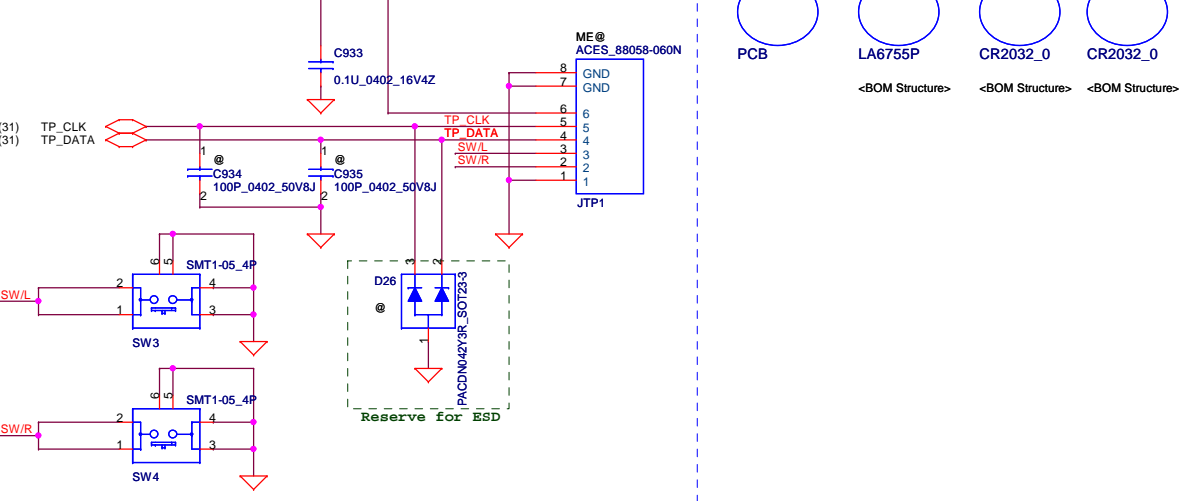
Security Classification	Compal Secret Data			<b>Compal Electronics, Inc.</b>		
Issued Date	2010/06/30	Deciphered Date	2012/06/30	Title <b>Power PIR</b>		
<small>THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&amp;D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.</small>				Size	Document Number	Rev
				Custom	LA6755P/TP	0.1
				Date:	Tuesday, November 30, 2010	Sheet

# INT\_KBD Conn.

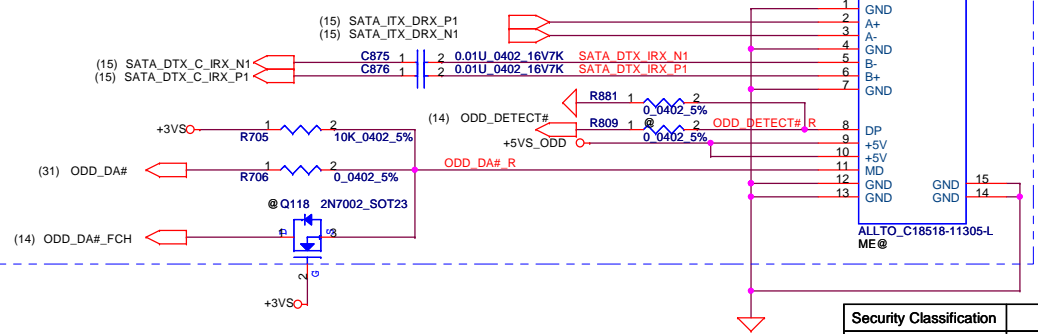


CONN PIN define need double check

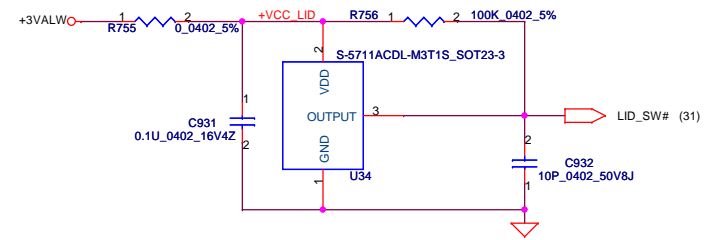
# To TP/B Conn.



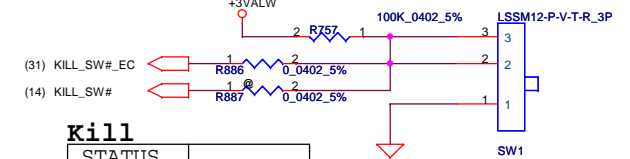
# SATA ODD Conn.



# Lid Switch



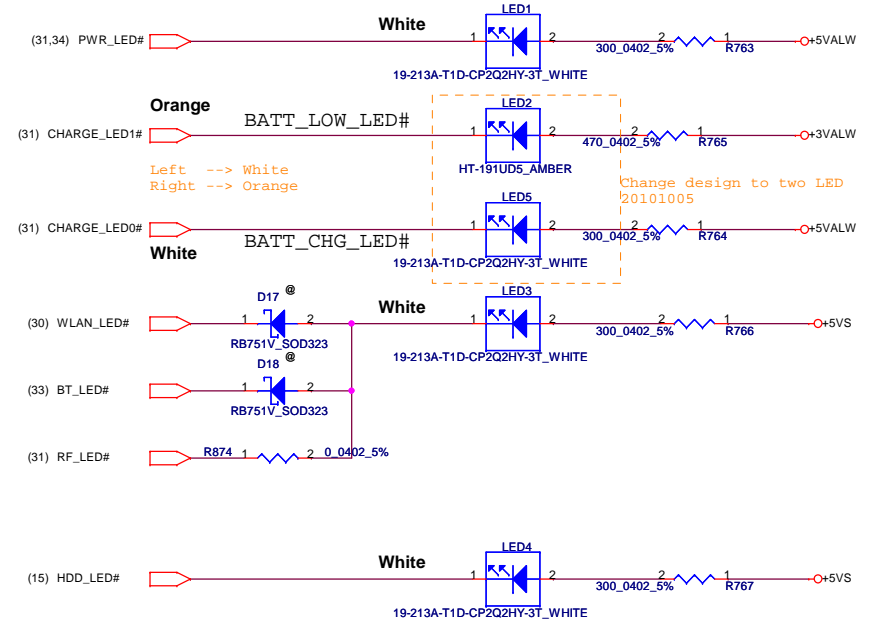
# Kill Switch



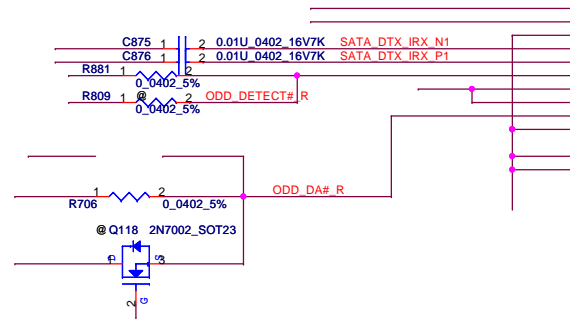
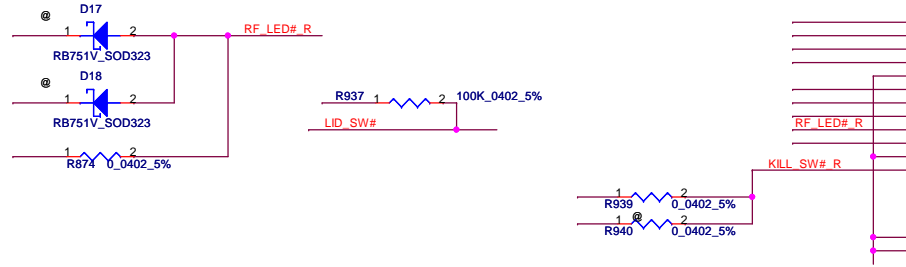
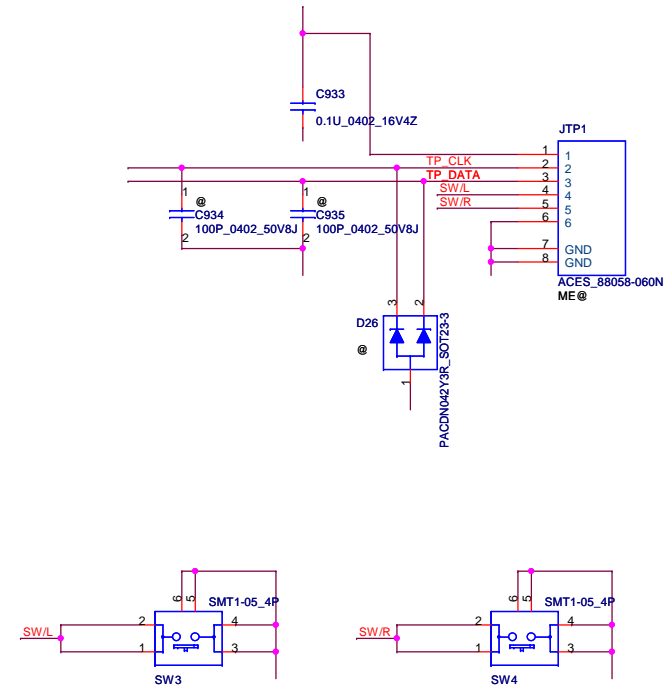
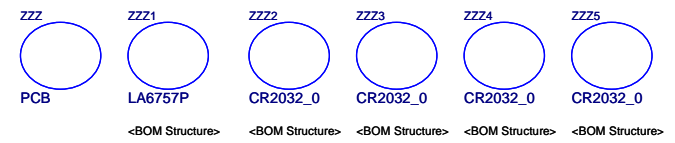
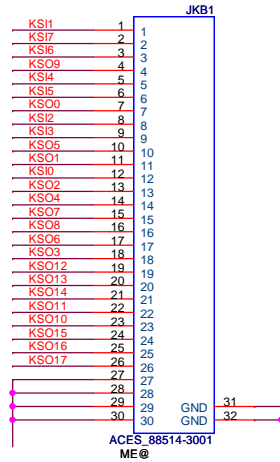
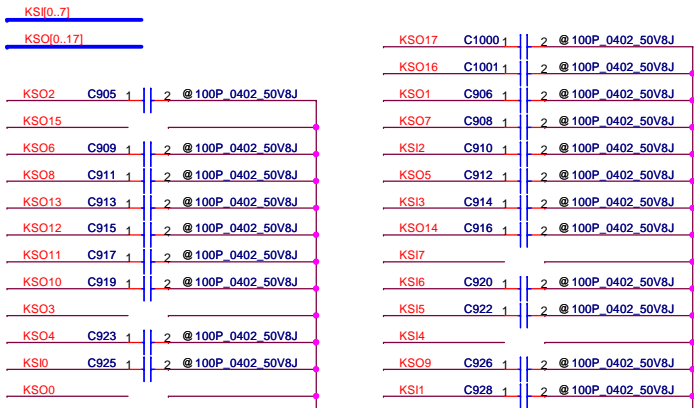
**Kill**

STATUS	
1, 2 (LOW)	OFF
2, 3 (HI)	ON

# LED



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Security Classification		Compal Secret Data		<b>Compal Electronics, Inc.</b>	
Issued Date	2010/06/30	Deciphered Date	2012/06/30	Title <b>15" ONLY</b>	
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				<b>LA6757P</b>	
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PHASE	PAGE	Modification list	PURPOSE
0.2	P08	C643 change to OS-CON type	For cost down purpose
0.2	P10	pop R490, unpop R491	LVDS PWM controls by EC
0.2	P10	Add CE_EN @ JLVDS1.16 and U33.98	For color engine function
0.2	P10	R488 pull-up to +5VALW	For C38 module design
0.2	P10	Add R938	For CMOS cost down purpose
0.2	P12	JCRT1 change foot-print from DC060003000 to DC060004800	Foot-print is wrong
0.2	P14	SATA_DET# change from U26.AE19 to U26.AB21	For corresponding SATA port assigned
0.2	P16	Delete R635	Our codec consumes +3V
0.2	P18	Add R936	For VGA_PWRGD reservation
0.2	P20	Q69 ~ Q72 change to N-MOS	Follow BACO suggestion SCH
0.2	P21	R840 pull-up change to +5VALW and R857 change to 20K ohms	For +3VGS sequence design
0.2	P21	Delete Q122, Add U47, C999, R944	For +1.0VGS DC power design
0.2	P23	L27 change to 0 ohms	For new reference circuit
0.2	P23	Delete GND connection of U8.N11 and U8.N12	For new reference circuit
0.2	P21	R344 change to 20K ohms	Prevent Q74 damage
0.2	P28	J7 foot-print update	Base on DFX request
0.2	P28	Add net CLK_PCI_DB_R and unpop R854	for EMI concern
0.2	P28	Modify PC_Beep circuit	Base on vender suggestion
0.2	P23	Delete C421, C422, C431, C432, C433	For new reference circuit
0.2	P31	R734 pull-high change to +5VALW	For USB ports ACIN leakage
0.2	P31	Add BATT_SEL_EC at U33.103	For Battery selection reservation
0.2	P33	Add R941	For further cost down purpose
0.2	P33	Add R942, R943, C998	For SATA_DET# function design
0.2	P28	Delete C851, C855	For useless AGND bridge
0.2	P34	Change JP7 to JPWRB1 and JP8 to JCR1	For standard naming
0.2	P34	Del U45, R890 ~ R899, J12, CHR_ON# (U33.70)	Deleting USB charge function
0.2	P35	Delete C974	Deleting unnecessary part for +1.IVS
0.2	P19	Add R945, R946	For HDMI Audio strap
0.2	P13	Delete T79, T80	For layout space needed for SATA calibration
0.2	P28	Add R947, R948	For EMI solution reservation base on vender suggetion
0.2	P28	Delete C857, R694	To delete redundant part base on vender suggestion
0.2	P28	L57 ~ L60 change to 0_0603_5%	Base on vender suggestion
0.2	P28	R672 change to 0ohm and location to be series on HDA_BITCLK_AUDIO	For EMI solution reservation base on vender suggetion
0.2	P14	Kill_SW# change from U26.G24 to U26.K1	Kill_SW# function needs event pin
0.2	P31	Add R949, C1002	Requirement of implementing SUSCLK
0.2	P28	Add R950 @ +3VS, R951 @ +LDO_OUT_3.3V, R952 @ +5VS	For customer request (PWR consumption)
0.2	P28	Add R953	For PC Beep circuit
0.2	P29	Add R954, R955	For customer request (PWR consumption)
0.2	P13	Add C1003, U48, R956, R957	For PX GPU_RST# function
0.2	P18	Delete R556, R841, R889, D28	
0.2	P05	Add R958	For enabling HDMI function
0.2	P28	Add R959	For EMI reservation
0.2	P32	Add R960 and C1004	For EMI reservation
0.2	P09	Add R961 and R962	For DDR SO-DIMMB strap pin reservation
0.2	P05	Delete T74, T75	For layout limitation
0.3	P29 P46	change +5V_ODD to +5VS_ODD	For better net name
0.3	P32	R760 change to 100ohm bead and R761 change back to 15ohm resistor	For correct EMI solution
0.3	P21	U47 change to SB00000GV00 footprint	For correct symbol
0.3	P05	R958 change to HDMI@ and R422 change to nonHDMI@	For SKU without HDMI function
0.3	P21	Add PX_MODE off page	For design correction

Change footprint  
20100812 : For cost down purpose to change parts

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PHASE	PAGE	Modification list	PURPOSE
0.2	P08	C643 change to OS-CON type	For cost down purpose
0.2	P10	pop R490, unpop R491	LVDS PWM controls by EC
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0.2	P10	Add R938	For CMOS cost down purpose
0.2	P12	JCRT1 change foot-print from DC060003000 to DC060004800	Foot-print is wrong
0.2	P14	SATA_DET# change from U26.AE19 to U26.AB21	For corresponding SATA port assigned
0.2	P16	Delete R635	Our codec consumes +3V
0.2	P18	Add R936	For VGA_PWRGD reservation
0.2	P20	Q69 ~ Q72 change to N-MOS	Follow BACO suggestion SCH
0.2	P21	R840 pull-up change to +5VALW and R857 change to 20K ohms	For +3VGS sequence design
0.2	P21	Delete Q122, Add U47, C999, R944	For +1.0VGS DC power design
0.2	P23	L27 change to 0 ohms	For new reference circuit
0.2	P23	Delete GND connection of U8.N11 and U8.N12	For new reference circuit
0.2	P21	R344 change to 20K ohms	Prevent Q74 damage
0.2	P28	J7 foot-print update	Base on DFX request
0.2	P28	Add net CLK_PCI_DB_R and unpop R854	for EMI concern
0.2	P28	Modify PC_Beep circuit	Base on vender suggestion
0.2	P23	Delete C421, C422, C431, C432, C433	For new reference circuit
0.2	P31	R734 pull-high change to +5VALW	For USB ports ACIN leakage
0.2	P31	Add BATT_SEL_EC at U33.103	For Battery selection reservation
0.2	P33	Add R941	For further cost down purpose
0.2	P33	Add R942, R943, C998	For SATA_DET# function design
0.2	P28	Delete C851, C855	For useless AGND bridge
0.2	P34	Change JP7 to JPWRB1 and JP8 to JCR1	For standard naming
0.2	P34	Del U45, R890 ~ R899, J12, CHR_ON# (U33.70)	Deleting USB charge function
0.2	P35	Delete C974	Deleting unnecessary part for +1.IVS
0.2	P19	Add R945, R946	For HDMI Audio strap
0.2	P13	Delete T79, T80	For layout space needed for SATA calibration
0.2	P28	Add R947, R948	For EMI solution reservation base on vender suggetion
0.2	P28	Delete C857, R694	To delete redundant part base on vender suggestion
0.2	P28	L57 ~ L60 change to 0_0603_5%	Base on vender suggestion
0.2	P28	R672 change to 0ohm and location to be series on HDA_BITCLK_AUDIO	For EMI solution reservation base on vender suggetion
0.2	P14	Kill_SW# change from U26.G24 to U26.K1	Kill_SW# function needs event pin
0.2	P31	Add R949, C1002	Requirement of implementing SUSCLK
0.2	P28	Add R950 @ +3VS, R951 @ +LDO_OUT_3.3V, R952 @ +5VS	For customer request (PWR consumption)
0.2	P28	Add R953	For PC Beep circuit
0.2	P29	Add R954, R955	For customer request (PWR consumption)
0.2	P13	Add C1003, U48, R956, R957	For PX GPU_RST# function
0.2	P18	Delete R556, R841, R889, D28	
0.2	P05	Add R958	For enabling HDMI function
0.2	P28	Add R959	For EMI reservation
0.2	P32	Add R960 and C1004	For EMI reservation
0.2	P09	Add R961 and R962	For DDR SO-DIMMB strap pin reservation
0.2	P05	Delete T74, T75	For layout limitation
0.2	P46	Add C1000, C1001	For 15" 30pin KB connector

15 only part

Change footprint  
20100812 : For cost down purpose to change parts

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PHASE	PAGE	Modification list	PURPOSE
0.3	P14	R603 and R604 change to pop	For SM Bus pull-high
0.3	P23	Reserve C1005	For PWR team request reserving a 330u capacitor
0.3	P33	C939 change to 5.9H OS-con	For cost saving
0.3	P33	R902 and R942 change to unpop	For eSATA function deletion
0.3	P29	U32 change PN to SA000046C00	For main source PN concern
0.3	P05	Delete JHDTI	For layout limitation
0.3	P11	Add F2 and change SM-BUS pull high net name to +5VS_HDMI_F	For safety team requirement
0.3	P21	change J3 footprint	For larger jumper footprint
0.3	P21	R856 change from 20K to 39K	For VGA power sequence
0.3	P11	Add net name +5VS_HDMI_F	For power trace indecation
0.3	P20	Change Q69 ~ Q72 PN	For design correction
0.3	P28	Add R963	For 20671-21Z update
0.3	P28	Change U31 PN to SA00003K410	For 20671-21Z PN
0.3	P20	U10.5, U46.5, and U44.5 change from +3VS to +3VGS	For BACO circuit update
0.3	P28	Delete R951	For unnecessary part deletion
0.3	P07	C623 change to unpop	Base on AMD checklist
0.3	P16	Delete C734, add C1006, C1007	For ME concern
0.3	P21	R924 cahgne pull-up from +3VS to +3VALW	For BACO design correction
0.3	P21	R925 change to pop	For BACO design correction
0.3	P14	Reserve C1008 at FCH_PWRGD	For EMI request
0.3	P14	Reserve C1009 at VGATE	For EMI request
0.3	P31	Reserve C1010 at VR_ON	For EMI request
0.3	P13	Reserve C1011 at H_PWRGD_L	For EMI request
0.3	P28	pop C849, C850, R692, R693, R696, C826	For EMI request
0.3	P27	Add C1012, C1013	For EMI request (gas discharge tube)
0.3	P27	Add D1	For EMI request (ESD diode)
0.3	P28	update R672 location	For EMI request (RC to GND for codec BIT_CLK)
0.3	P07	Delete C617	For EMI solution space needed
0.3	P28	Pop D30, D31, unpop R953	For FCH PC-beep function
0.3	P31	R751 and R752 change from 4.7K ohm to 2.2K ohm	For PWR team request
0.3	P13	C719, C720 change from 22P to 18P	For RTC design
14" only part			
0.3	P46	Change one dual-diode LED2 to two single diode LED2 and LED5	For design change
1.0	P5	unpop R415	AMD checklist update
1.0	P10	R486, R487 change pull-high to +5VS	AMD checklist update
1.0	P11	R522, R523 change from 2.2K to 2K	AMD checklist update
1.0	P12	reserve R964, R965, change R546 ~ R549 from 4.7K to 2K	AMD checklist update
1.0	P31	BATT_LEN# added to U33.38	PWR team request
1.0	P20	Delete R341	For design update
1.0	P21	Delete R837, R832, R836	For design update
1.0	P28	Delete R947, R948, R950, R952	For design update
1.0	P29	Delete R955, R954, R810	For design update
1.0	P30	unpop C887, C888	For design update
1.0	P25	unpop C494, C484, C498, C482, C490	For design update

Change footprint  
20100812 : For cost down purpose to change parts

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PHASE	PAGE	Modification list	PURPOSE
0.3	P29 P46	change +5V_ODD to +5VS_ODD	For better net name
0.3	P32	R760 change to 100ohm bead and R761 change back to 15ohm resistor	For correct EMI solution
0.3	P21	U47 change to SB00000GV00 footprint	For correct symbol
0.3	P05	R958 change to HDMI@ and R422 change to nonHDMI@	For SKU without HDMI function
0.3	P21	Add PX_MODE off page	For design correction
0.3	P14	R603 and R604 change to pop	For SM Bus pull-high
0.3	P23	Reserve C1005	For PWR team request reserving a 330u capacitor
0.3	P33	C939 change to 5.9H OS-con	For cost saving
0.3	P33	R902 and R942 change to unpop	For eSATA function deletion
0.3	P29	U32 change FN to SA000046C00	For main source FN concern
0.3	P05	Delete JHDTI	For layout limitation
0.3	P11	Add F2 and change SM-BUS pull high net name to +5VS_HDMI_F	For safety team requirement
0.3	P21	change J3 footprint	For larger jumper footprint
0.3	P21	R856 change from 20K to 39K	For VGA power sequence
0.3	P11	Add net name +5VS_HDMI_F	For power trace indecation
0.3	P20	Change Q69 ~ Q72 PN	For design correction
0.3	P28	Add R963	For 20671-21Z update
0.3	P28	Change U31 PN to SA00003K410	For 20671-21Z PN
0.3	P20	U10.5, U46.5, and U44.5 change from +3VS to +3VGS	For BACO circuit update
0.3	P28	Delete R951	For unnecessary part deletion
0.3	P07	C623 change to unpop	Base on AMD checklist
0.3	P16	Delete C734, add C1006, C1007	For ME concern
0.3	P21	R924 cahgne pull-up from +3VS to +3VALW	For BACO design correction
0.3	P21	R925 change to pop	For BACO design correction
0.3	P14	Reserve C1008 at FCH_PWRGD	For EMI request
0.3	P14	Reserve C1009 at VGATE	For EMI request
0.3	P31	Reserve C1010 at VR_ON	For EMI request
0.3	P13	Reserve C1011 at H_PWRGD_L	For EMI request
0.3	P28	pop C849, C850, R692, R693, R696, C826	For EMI request
0.3	P27	Add C1012, C1013	For EMI request (gas discharge tube)
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0.3	P07	Delete C617	For EMI solution space needed
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0.3	P31	R751 and R752 change from 4.7K ohm to 2.2K ohm	For PWR team request
0.3	P13	C719, C720 change from 22P to 18P	For RTC design
1.0	P5	unpop R415	AMD checklist update
1.0	P10	R486, R487 change pull-high to +5VS	AMD checklist update
1.0	P11	R522, R523 change from 2.2K to 2K	AMD checklist update
1.0	P12	Add R964, R965, change R548, R549 from 4.7K to 2K unpop R546, R547, Q89	AMD checklist update
1.0	P31	BATT_LEN# added to U33.38	PWR team request
1.0	P46	Kill_SW#_R change from JLED1.5 to JLED1.12	Design change update
1.0	P20	Delete R341	For design update
1.0	P21	Delete R837, R832, R836	For design update
1.0	P28	Delete R947, R948, R950, R952	For design update
1.0	P29	Delete R955, R954, R810	For design update
1.0	P30	unpop C887, C888	For design update
1.0	P25	unpop C494, C484, C498, C482, C490	For design update

Change footprint  
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