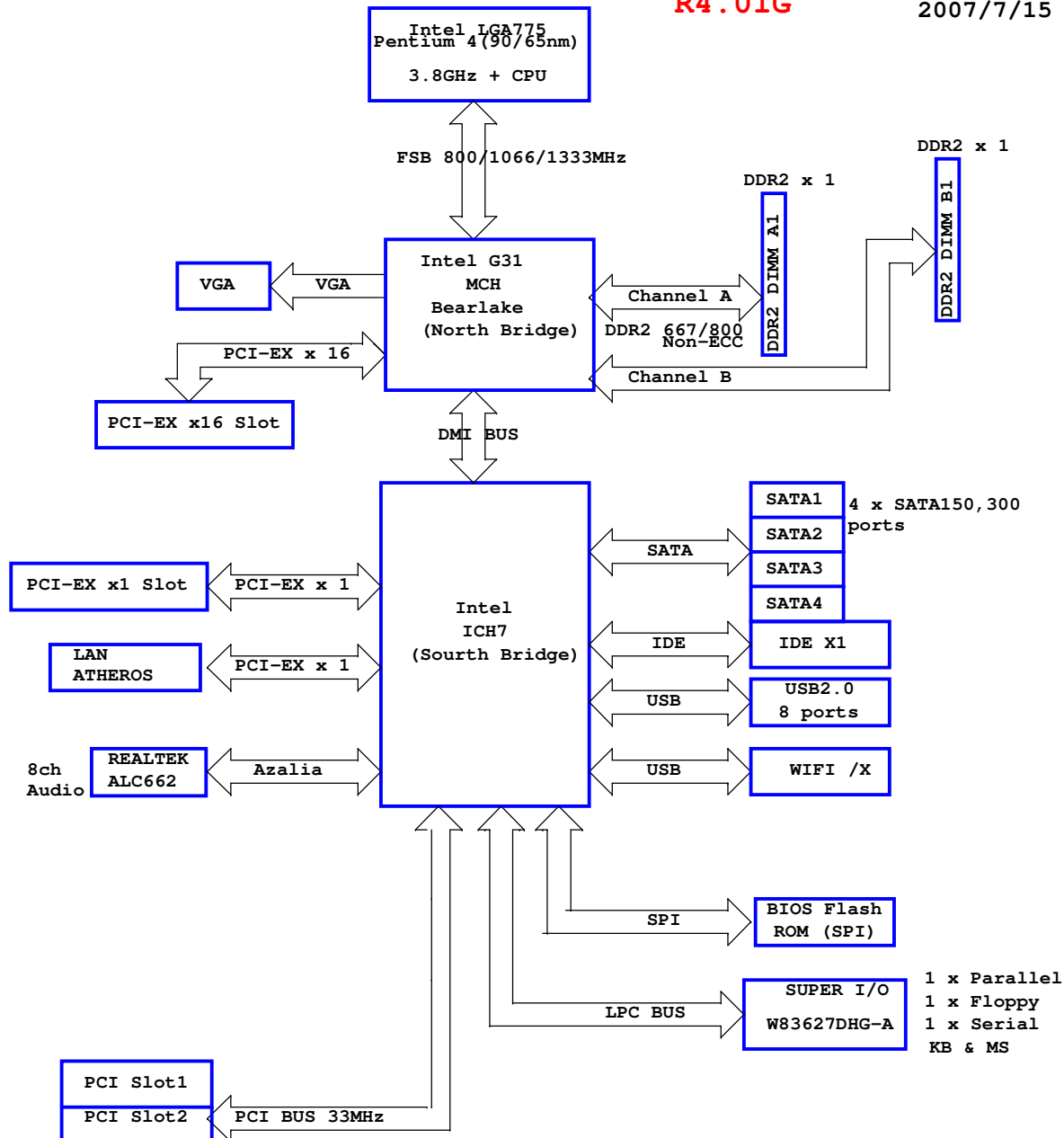


P5KPL-VM/SI

R4.01G

2007/7/15



TITLE	VERSION
01.BLOCK DIAGRAM	1.00G
02.NAMING RULE	
03.POWER SEQUENCE	
04.POWER FLOW	
05.CLOCK DIAGRAM	
06.CPU TIMING	
07.CLOCK GEN	
08.LGA775-1	
09.LGA775-2	
10.LGA775-3	
11.LGA775-4	
12.LGA775-5	
13.BROADWATER-1	1.00G
14.BROADWATER-2	
15.BROADWATER-3	
16.BROADWATER-4	
17.BROADWATER-5	
18.BROADWATER-6	
19.DDR2 A	
20.DDR2 B	
21.DDR TERM RES	
22.ASM4131	1.00G
23.PCI-E X16	1.00G
24.VGA	1.00G
25.ICH7-1	
26.ICH7-2	1.00G
27.ICH7-3	
28.ICH7-4	
29.PCI-E X1	
30.PCI SLOT 1 2	
31.AUDIO-ALC888T	
32.AZA CONNECTOR	
33.IDE AND SATA	1.00G
34.SIO W83627DHG-A	
35.I/O CONNECTOR	
36.SPI, TPM	
37.FAN CONTROL	
38.LAN ATTANSIC	
39.USB PORT,WIFI	
40.FRONT PANEL	
41.VCORE CONTROLLER	
42.VCORE DRIVER	
43.+1.8VDUAL&VTDDR	1.00G
44.+3VSB&+5V_DUAL&+3V_DUAL	1.00G
45.+1.25V_MCH&+1.5V&+1.05V	1.00G
46.VTT CPU	1.00G
47.LAN 2.5V&LAN 1.5V	1.00G
48.EMI	

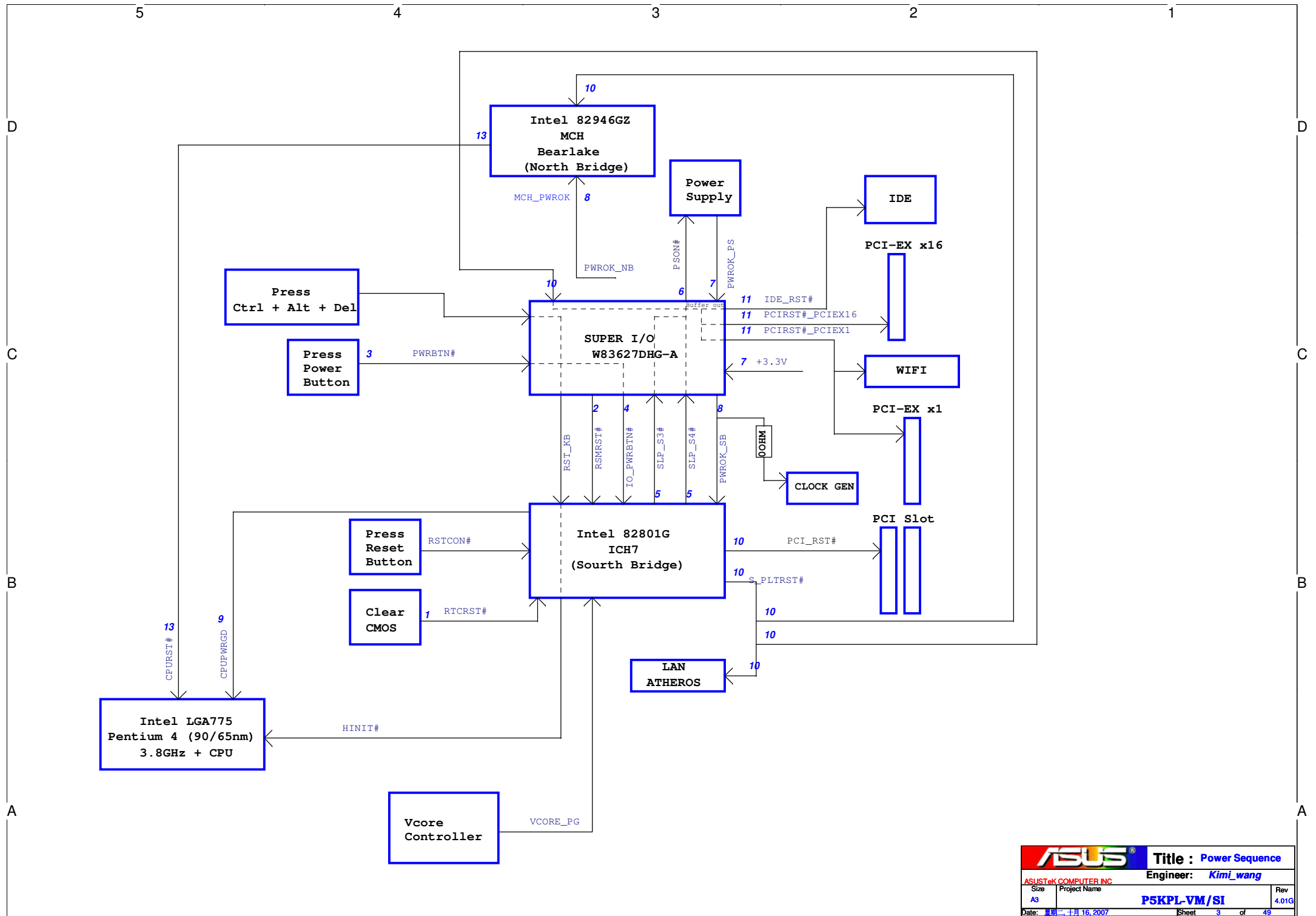
Reference Naming Rule

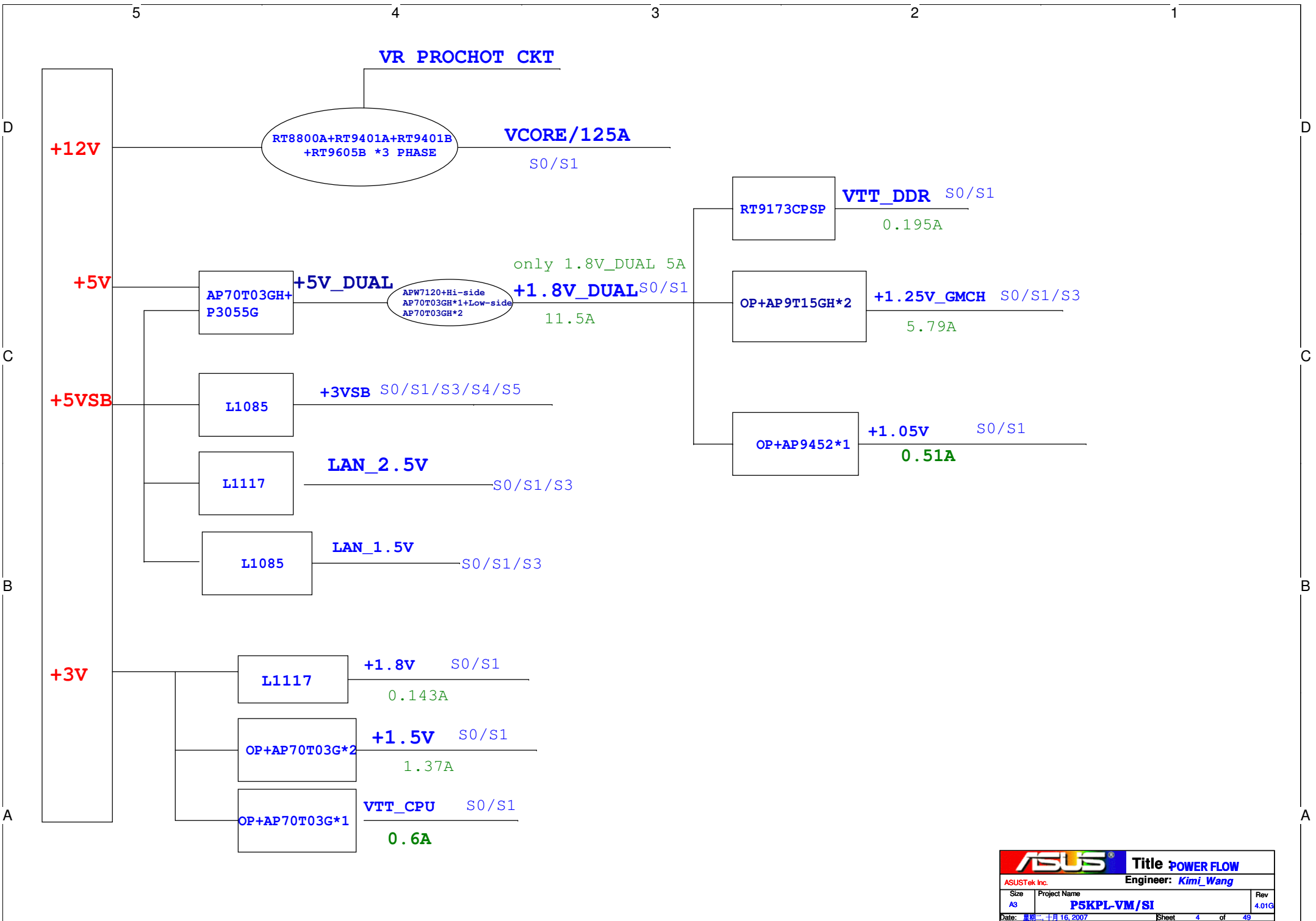
A	B	CK	D	D1	D2	E	F	G
Audio		Clock	DMI	DDR1	DDR2	EMI		
H	I	J	K	L	M	N	O	P
CPU	IDE			LAN		NB	Super I/O	PCI
Q	R	S	T	U	V	W	X16	X4
	RAID	SB	SATA	USB 2.0	VGA	H/W Monitor	PCI-E X16	PCI-E X4
X1	Y	Z						
PCI-E X1	TPM	ITP	SPI					

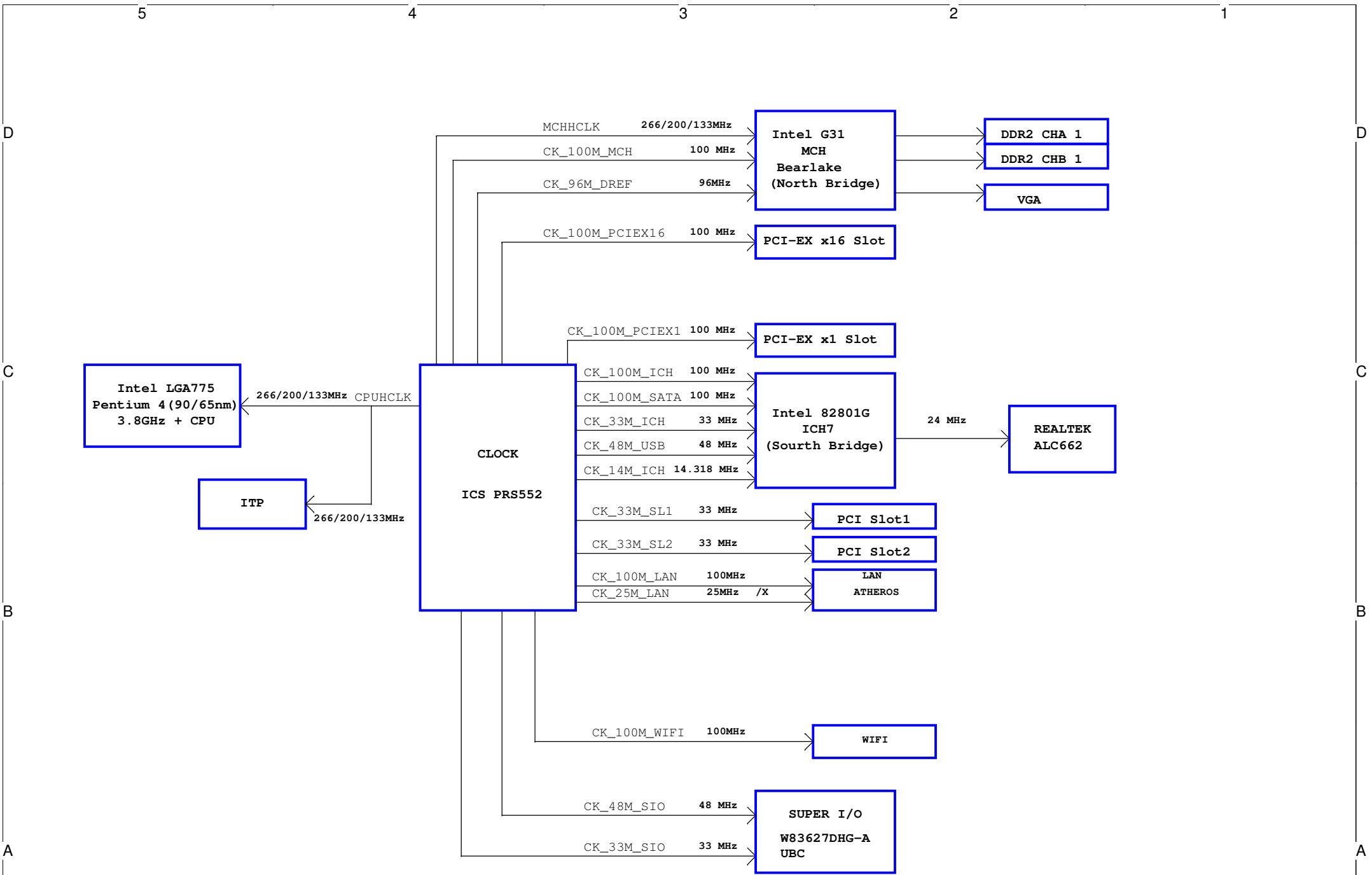
Net Naming Rules

1. When a net passes a resistor, add R_ to net name to identify the shorter route.
2. When a net passes a capacitor, add C_ to net name to identify the shorter route.
3. Use function as a net main name. If there're inflections, please add _(destination) to identify.
(e.g. R_CK_33M_PCH1, C_EXP16_TXP0, RESETCON#_SIO)

Jumper Naming Rule refer to Version 2.0.







5

4

3

2

1

D

D

C

C

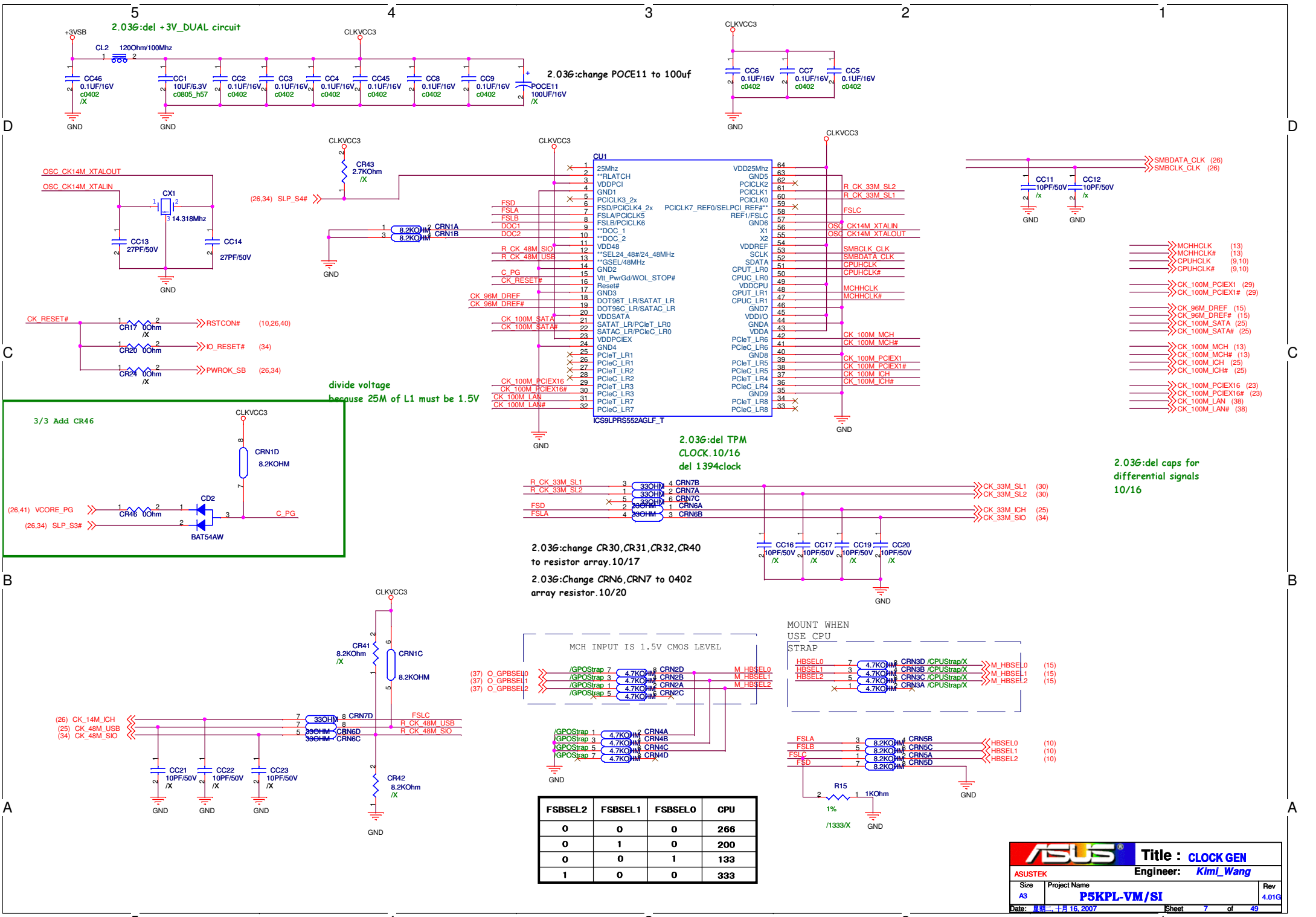
B

B

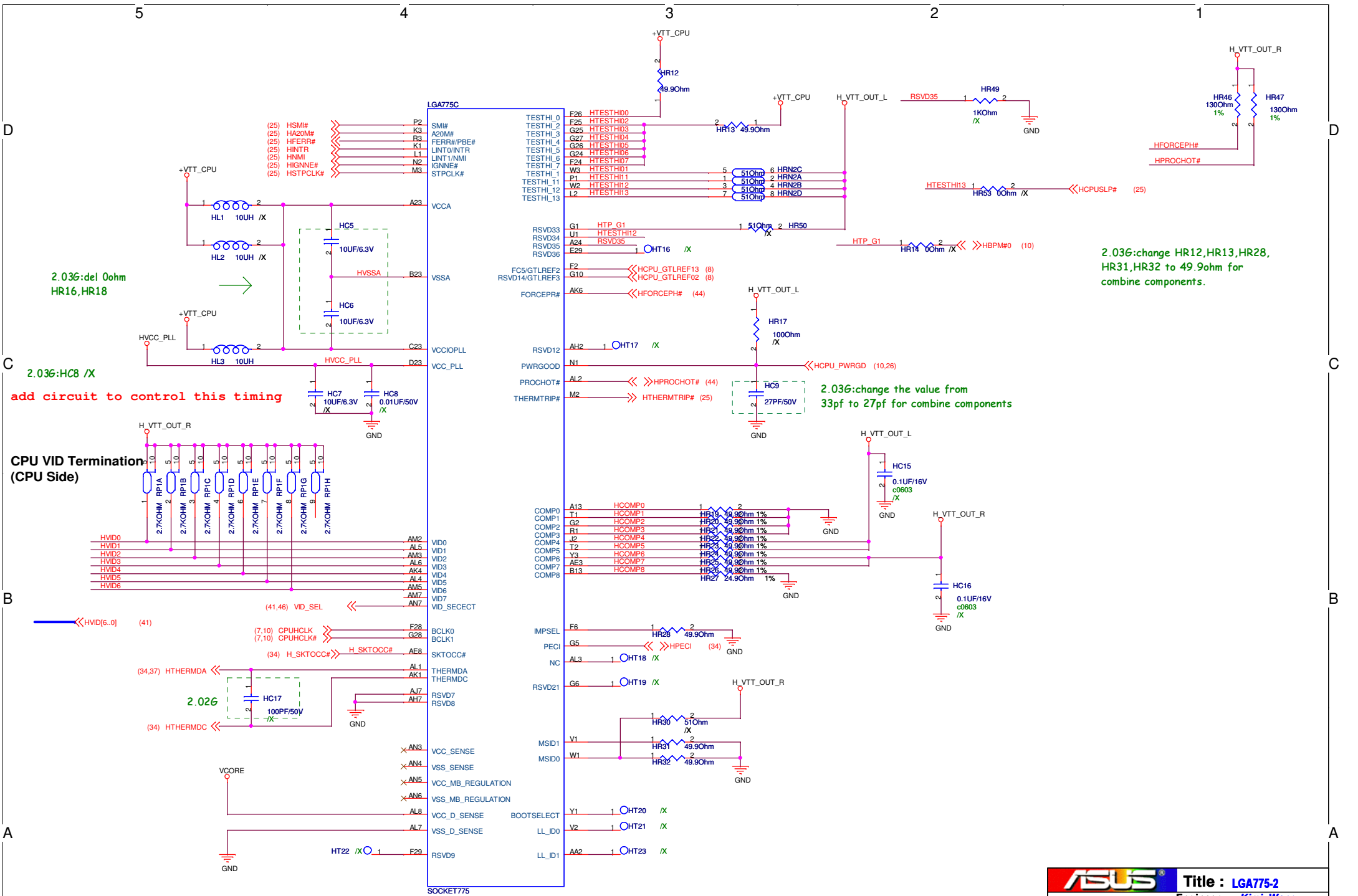
A

A

		Title : CPU Timing	
ASUSTEK		Engineer: <i>Lazy Li</i>	
Size A3	Project Name PSB-MX	Rev 4.01G	
Date: 星期二, 十月 16, 2007		Sheet	6 of 49



FSBSEL2	FSBSEL1	FSBSEL0	CPU
0	0	0	266
0	1	0	200
0	0	1	133
1	0	0	333

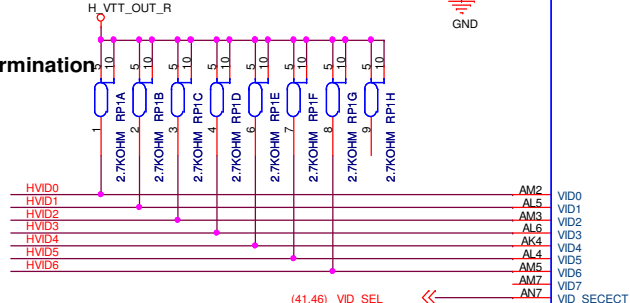


2.03G:del 0ohm
HR16,HR18

2.03G:HC8 /X

add circuit to control this timing

**CPU VID Termination
(CPU Side)**

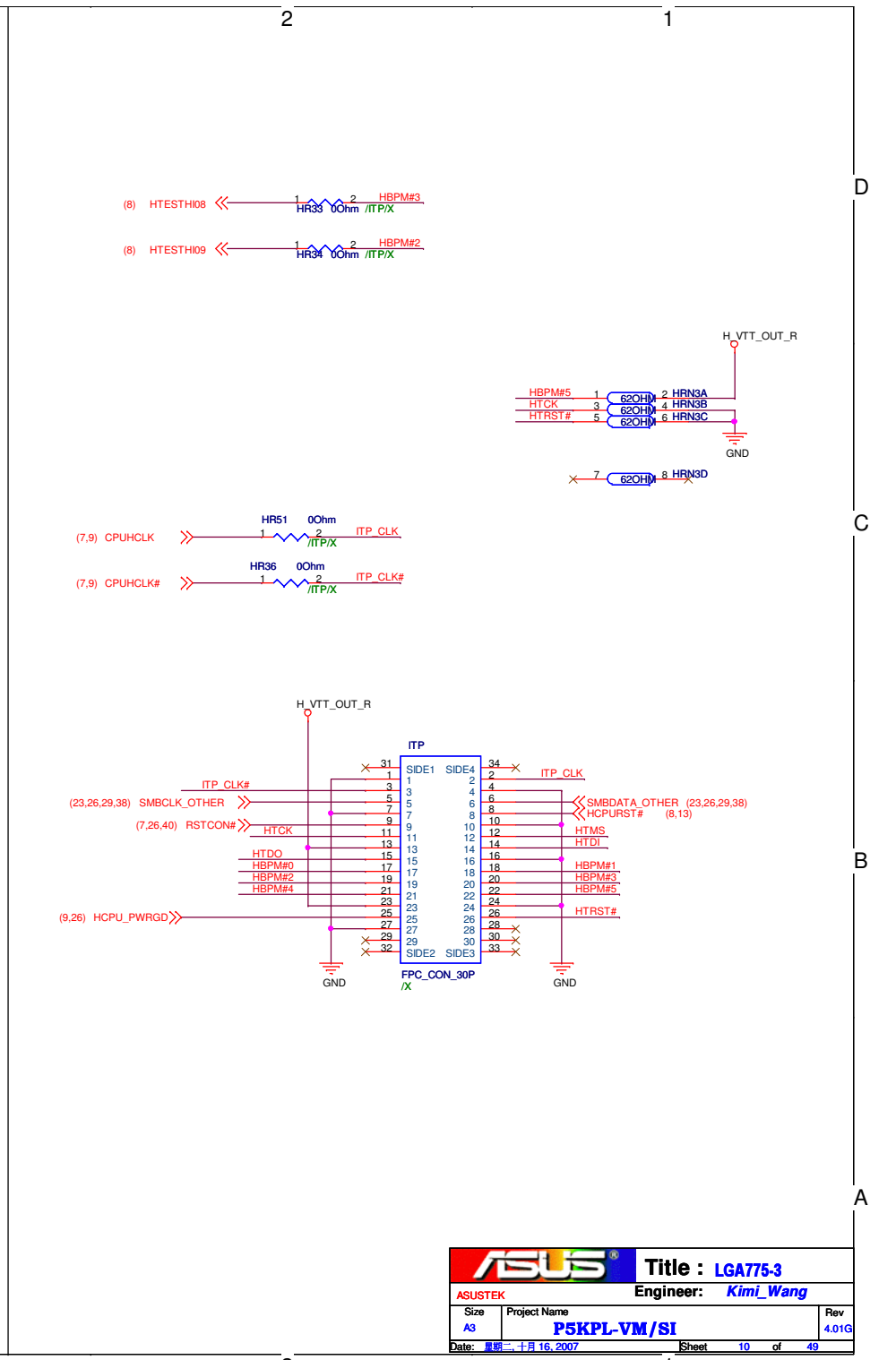
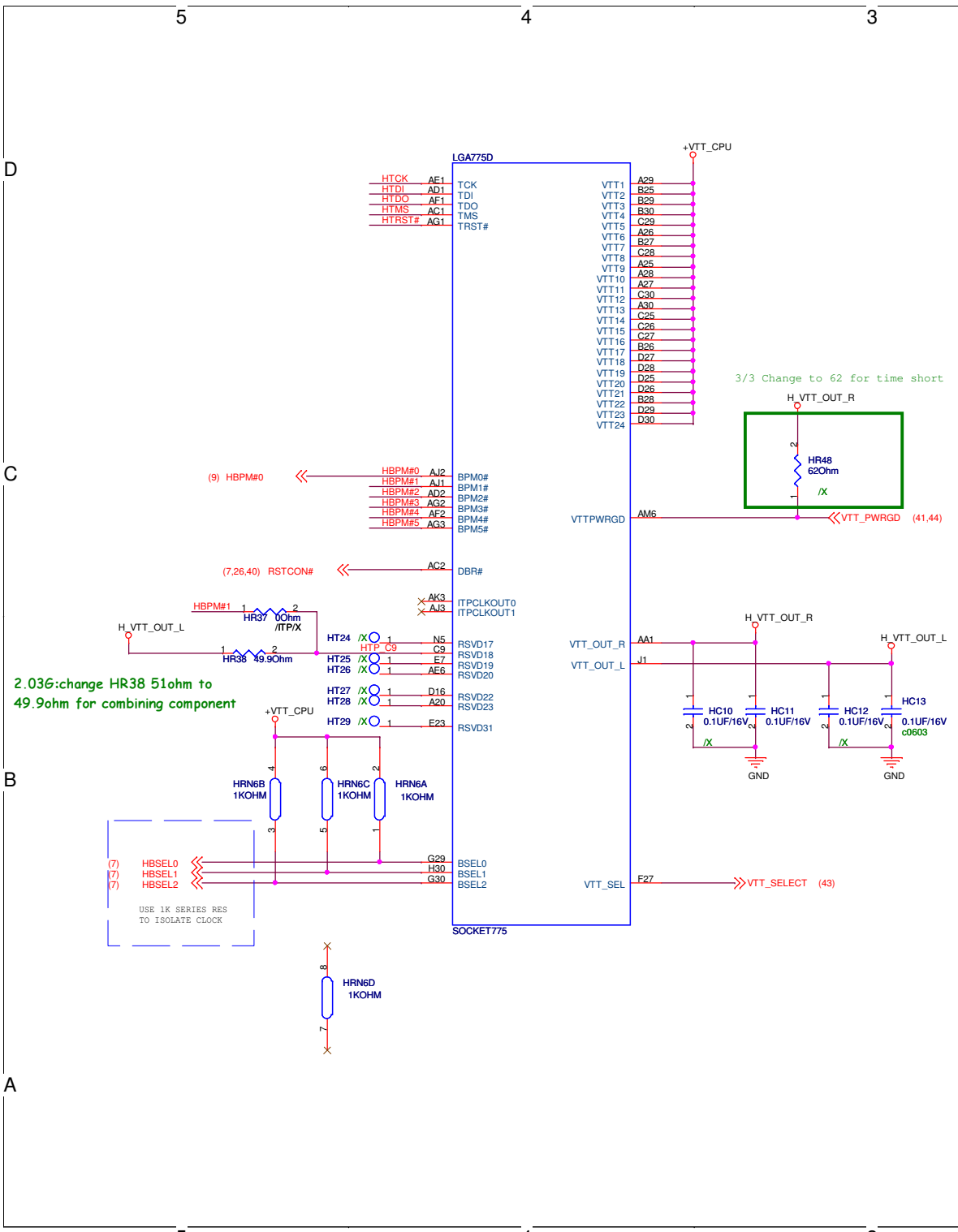


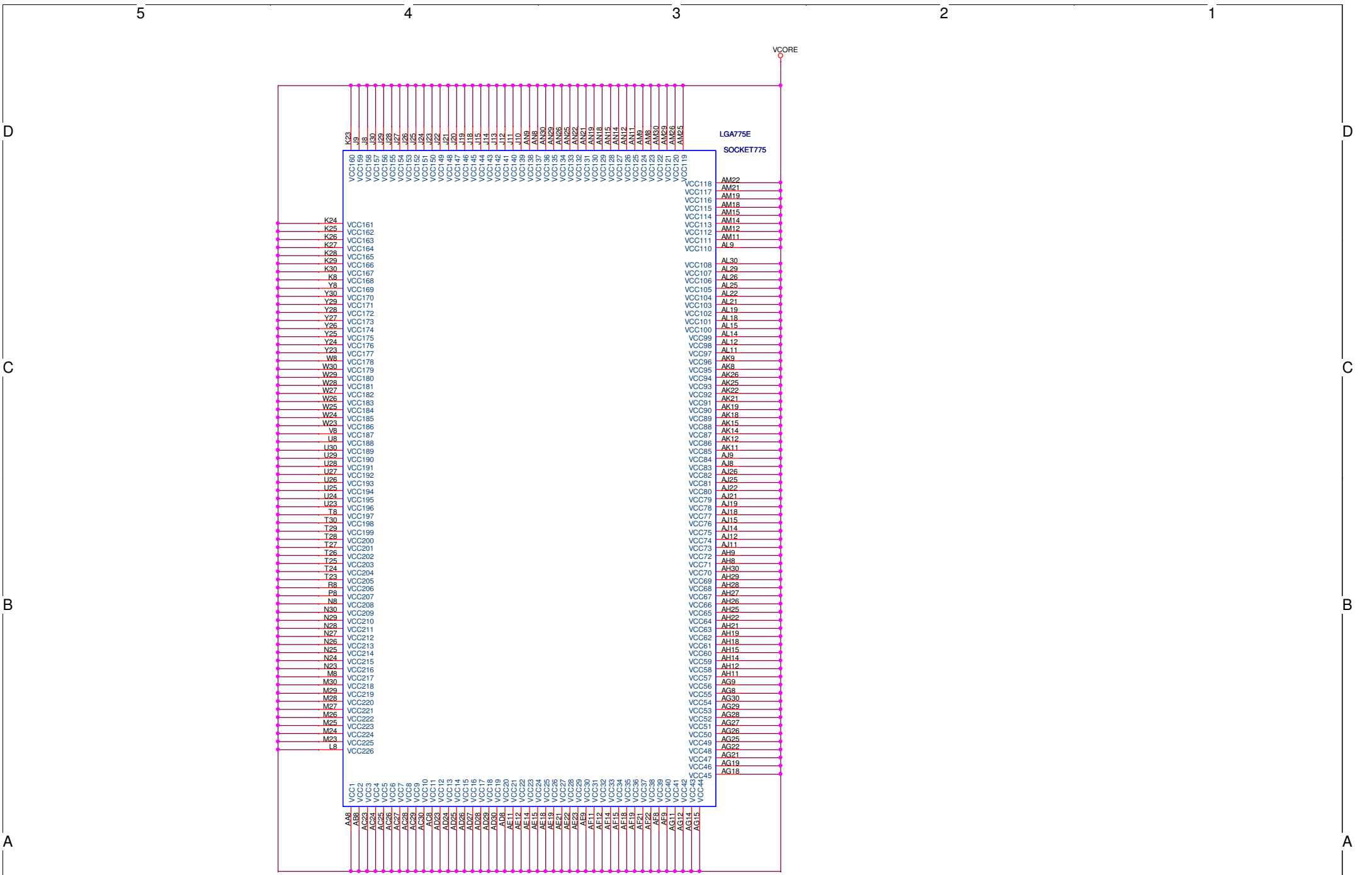
2.02G
HC17
100PF/50V

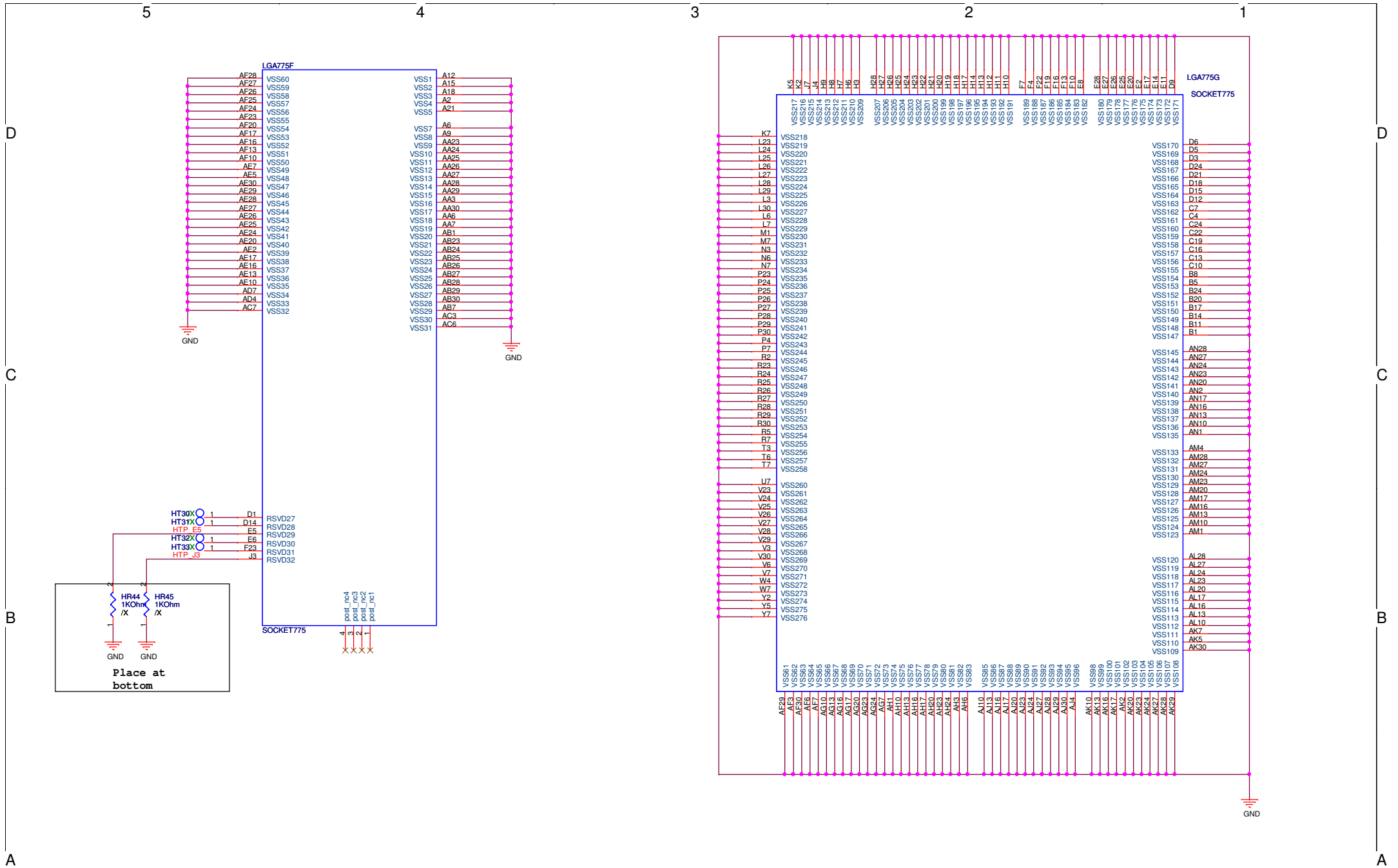
2.03G:change HR12,HR13,HR28,
HR31,HR32 to 49.9ohm for
combine components.

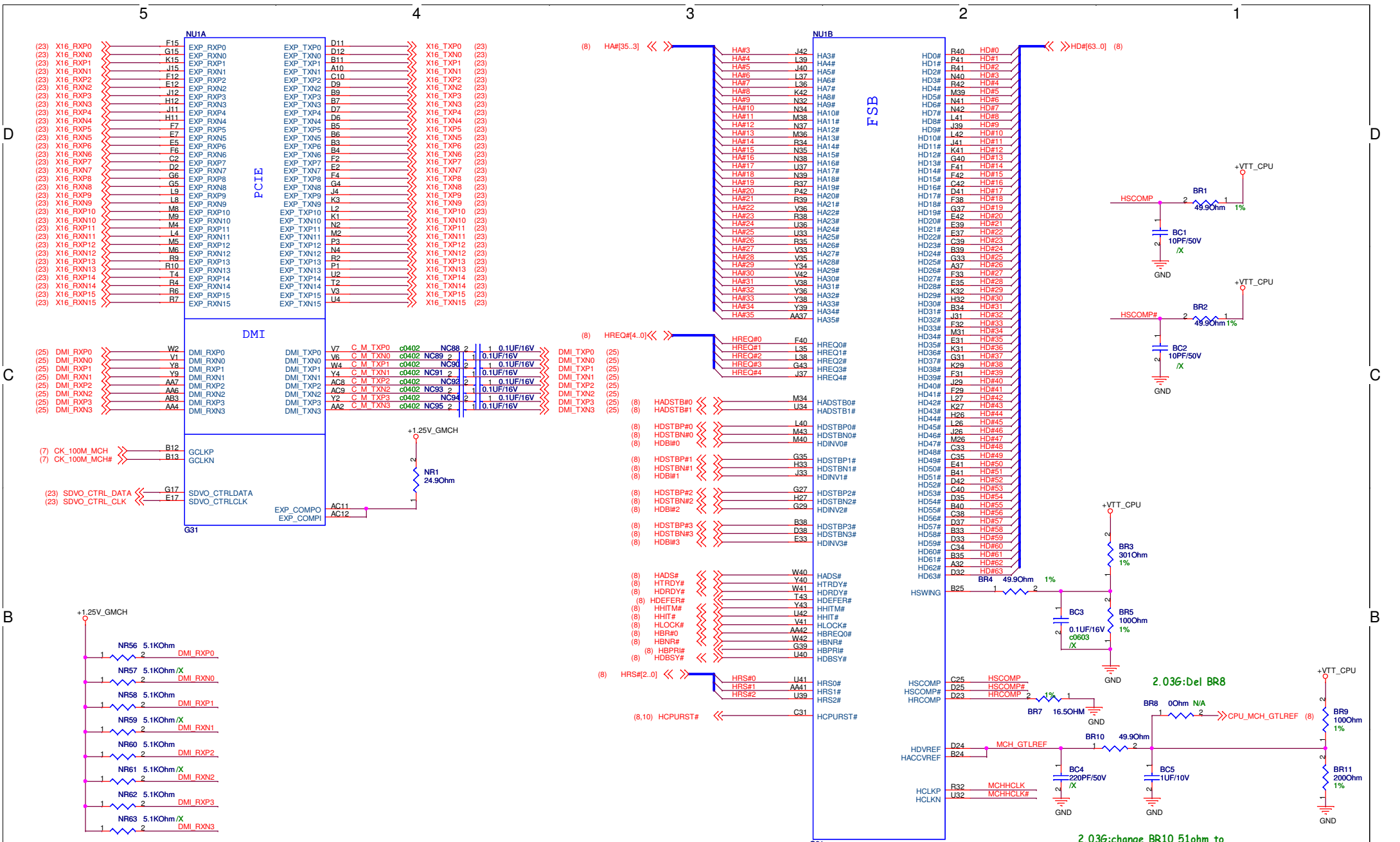
2.03G:change the value from
33pf to 27pf for combine components

ASUS		Title : LGA775-2	
ASUSTEK		Engineer: Kimi_Wang	
Size A3	Project Name P5KPL-VM/SI	Rev 4.01G	
Date: 星期二, 十月 16, 2007		Sheet 9 of 49	





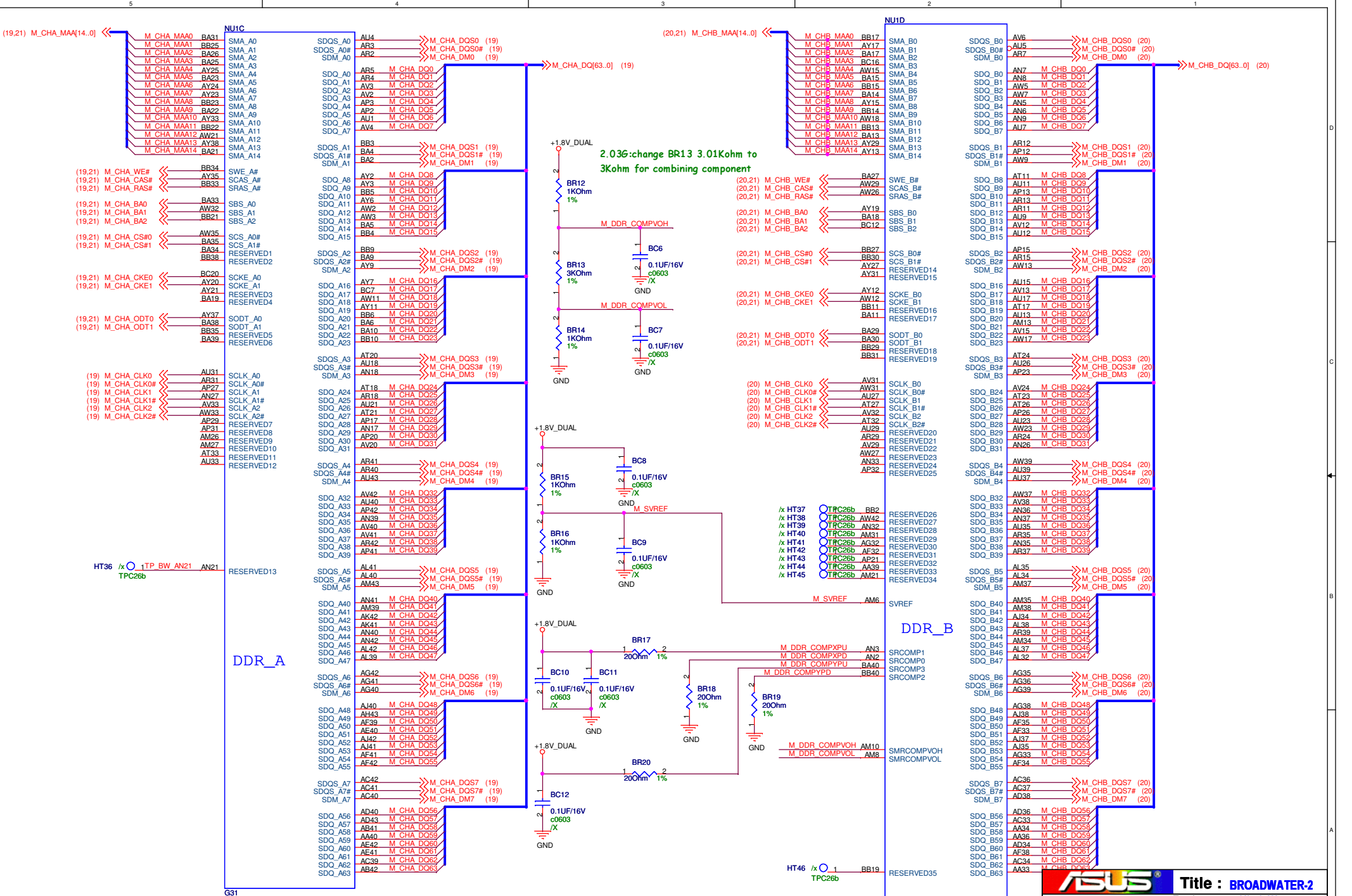




A CLOSE TO MCH

(7) MCHCLK# (7)
 (7) MCHCLK# (7)

2.036:change BR10 51ohm to 49.9ohm for combining component



- (19.21) M_CHA_MAA[14..0] ←
- M_CHA_MAA0 BA31
 - M_CHA_MAA1 BB25
 - M_CHA_MAA2 BA26
 - M_CHA_MAA3 BA25
 - M_CHA_MAA4 AY25
 - M_CHA_MAA5 BA23
 - M_CHA_MAA6 AY24
 - M_CHA_MAA7 AY23
 - M_CHA_MAA8 BB23
 - M_CHA_MAA9 BA22
 - M_CHA_MAA10 AY33
 - M_CHA_MAA11 BB22
 - M_CHA_MAA12 AW21
 - M_CHA_MAA13 AY38
 - M_CHA_MAA14 BA21
- (19.21) M_CHA_WE# ←
- BB34
 - AY35
 - BB33
- (19.21) M_CHA_CAS# ←
- BB33
 - SRAS_A#
- (19.21) M_CHA_BA0 ←
- BA33
 - AW32
 - BB21
- (19.21) M_CHA_BA1 ←
- BB21
- (19.21) M_CHA_CS#0 ←
- AW35
 - BA35
- (19.21) M_CHA_CS#1 ←
- BA34
 - BB38
- (19.21) M_CHA_CKE0 ←
- BC20
 - AY20
- (19.21) M_CHA_CKE1 ←
- AY21
 - RESERVED3
 - BA19
- (19.21) M_CHA_ODT0 ←
- AY37
- (19.21) M_CHA_ODT1 ←
- BA38
 - BB35
 - BA39
- (19) M_CHA_CLK0 ←
- AU31
- (19) M_CHA_CLK0# ←
- AP31
- (19) M_CHA_CLK1 ←
- AP27
- (19) M_CHA_CLK1# ←
- AY33
- (19) M_CHA_CLK2 ←
- AW33
- (19) M_CHA_CLK2# ←
- AP23
 - AP31
 - AM26
 - AM27
 - RESERVED10
 - AT33
 - RESERVED11
 - AU33
- HT36 /x O_1TP_BW_AN21 AN21
- TPC26b

- NU1C
- SDQS_A0 AU4
 - SDQS_A0# AR3
 - SDQS_A0# AR2
 - SDQS_A0# AR5
 - SDQ_A0 AR4
 - SDQ_A1 AV2
 - SDQ_A2 AV2
 - SDQ_A3 AP3
 - SDQ_A4 AP2
 - SDQ_A5 AU1
 - SDQ_A6 AV4
 - SDQ_A7
 - SDQS_A1 BB3
 - SDQS_A1# BA4
 - SDM_A1 BA2
 - SDQ_A8 AY2
 - SDQ_A9 AY3
 - SDQ_A10 BB5
 - SDQ_A11 AY6
 - SDQ_A12 AW2
 - SDQ_A13 AW3
 - SDQ_A14 BA5
 - SDQ_A15 BB4
 - SDQS_A2 BB9
 - SDQS_A2# BA9
 - SDM_A2 AY9
 - SDQ_A16 AY7
 - SDQ_A17 BC7
 - SDQ_A18 AW11
 - SDQ_A19 BB6
 - SDQ_A20 BA6
 - SDQ_A21 BA10
 - SDQ_A22 BA10
 - SDQ_A23 BB10
 - SDQS_A3 AT20
 - SDQS_A3# AU18
 - SDM_A3 AN18
 - SDQ_A24 AT18
 - SDQ_A25 AR18
 - SDQ_A26 AU21
 - SDQ_A27 AT21
 - SDQ_A28 AP17
 - SDQ_A29 AN17
 - SDQ_A30 AP20
 - SDQ_A31 AV20
 - SDQS_A4 AR41
 - SDQS_A4# AR40
 - SDM_A4 AU43
 - SDQ_A32 AV42
 - SDQ_A33 AU40
 - SDQ_A34 AP42
 - SDQ_A35 AN39
 - SDQ_A36 AV40
 - SDQ_A37 AV41
 - SDQ_A38 AR42
 - SDQ_A39 AP41
 - SDQS_A5 AL41
 - SDQS_A5# AL40
 - SDM_A5 AM43
 - SDQ_A40 AN41
 - SDQ_A41 AM39
 - SDQ_A42 AK42
 - SDQ_A43 AK41
 - SDQ_A44 AN40
 - SDQ_A45 AN42
 - SDQ_A46 AL42
 - SDQ_A47 AL39
 - SDQS_A6 AG42
 - SDQS_A6# AG41
 - SDM_A6 AG40
 - SDQ_A48 AJ40
 - SDQ_A49 AH43
 - SDQ_A50 AF39
 - SDQ_A51 AF40
 - SDQ_A52 AJ42
 - SDQ_A53 AJ41
 - SDQ_A54 AF41
 - SDQ_A55 AF42
 - SDQS_A7 AC42
 - SDQS_A7# AC41
 - SDM_A7 AC40
 - SDQ_A56 AD40
 - SDQ_A57 AD43
 - SDQ_A58 AB41
 - SDQ_A59 AA40
 - SDQ_A60 AE42
 - SDQ_A61 AE41
 - SDQ_A62 AC39
 - SDQ_A63 AB42
- 2.03G:change BR13 3.01Kohm to 3Kohm for combining component
- M_DDR_COMPVHOH
- M_DDR_COMPVOL
- M_VREF
- M_SVREF
- M_DDR_COMPXPU
- M_DDR_COMPYPU
- M_DDR_COMPYPM
- M_VREF
- M_SVREF
- M_DDR_COMPVHOH
- M_DDR_COMPVOL

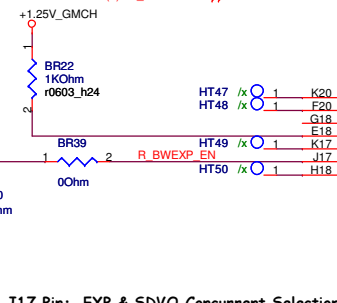
- (20.21) M_CHB_MAA[14..0] ←
- M_CHB_MAA0 BB17
 - M_CHB_MAA1 AY17
 - M_CHB_MAA2 BA17
 - M_CHB_MAA3 BC16
 - M_CHB_MAA4 AW15
 - M_CHB_MAA5 BA15
 - M_CHB_MAA6 BB15
 - M_CHB_MAA7 BA14
 - M_CHB_MAA8 AY15
 - M_CHB_MAA9 BB14
 - M_CHB_MAA10 AW18
 - M_CHB_MAA11 BB13
 - M_CHB_MAA12 BA13
 - M_CHB_MAA13 AY23
 - M_CHB_MAA14 AY13
- (20.21) M_CHB_WE# ←
- BA27
 - AW29
 - AW26
- (20.21) M_CHB_CAS# ←
- AW26
 - SRAS_B#
- (20.21) M_CHB_BA0 ←
- AY19
 - BB18
 - BC12
- (20.21) M_CHB_CS#0 ←
- BB27
 - BB30
 - AY27
 - AY31
- (20.21) M_CHB_CKE0 ←
- AY12
 - AW12
 - BB11
- (20.21) M_CHB_CKE1 ←
- BA29
 - BA30
 - BB29
- (20.21) M_CHB_ODT0 ←
- BA29
 - BA30
 - BB29
- (20.21) M_CHB_ODT1 ←
- BB31
- (20) M_CHB_CLK0 ←
- AW31
- (20) M_CHB_CLK0# ←
- AW31
- (20) M_CHB_CLK1 ←
- AT27
- (20) M_CHB_CLK1# ←
- AT27
- (20) M_CHB_CLK2 ←
- AV32
- (20) M_CHB_CLK2# ←
- AT32
 - AW23
 - AB29
 - AV29
 - AW27
 - AN33
 - AF32
- M_VREF
- M_SVREF
- M_DDR_COMPXPU
- M_DDR_COMPYPU
- M_DDR_COMPYPM
- M_VREF
- M_SVREF
- M_DDR_COMPVHOH
- M_DDR_COMPVOL

- NU1D
- SMA_B0 AV6
 - SMA_B1 AV5
 - SMA_B2 AR7
 - SMA_B3
 - SMA_B4
 - SMA_B5
 - SMA_B6
 - SMA_B7
 - SMA_B8
 - SMA_B9
 - SMA_B10
 - SMA_B11
 - SMA_B12
 - SMA_B13
 - SMA_B14
 - SDQS_B0 AN7
 - SDQS_B0# AN8
 - SDM_B0 AN5
 - SDQ_B0 AN7
 - SDQ_B1 AN8
 - SDQ_B2 AN5
 - SDQ_B3 AN7
 - SDQ_B4 AN5
 - SDQ_B5 AN6
 - SDQ_B6 AN9
 - SDQ_B7 AU7
 - SDQS_B1 AR12
 - SDQS_B1# AP12
 - SDM_B1 AW9
 - SDQ_B8 AT11
 - SDQ_B9 AU11
 - SDQ_B10 AP13
 - SDQ_B11 AR13
 - SDQ_B12 AR11
 - SDQ_B13 AU9
 - SDQ_B14 AV12
 - SDQ_B15 AU12
 - SDQS_B2 AP15
 - SDQS_B2# AR15
 - SDM_B2 AW13
 - SDQ_B16 AU15
 - SDQ_B17 AV13
 - SDQ_B18 AT17
 - SDQ_B19 AU13
 - SDQ_B20 AM13
 - SDQ_B21 AV15
 - SDQ_B22 AW17
 - SDQ_B23
 - SDQS_B3 AT24
 - SDQS_B3# AU26
 - SDM_B3 AP23
 - SDQ_B24 AV24
 - SDQ_B25 AT23
 - SDQ_B26 AT26
 - SDQ_B27 AP26
 - SDQ_B28 AU23
 - SDQ_B29 AW23
 - SDQ_B30 AR24
 - SDQ_B31 AN26
 - SDQS_B4 AW39
 - SDQS_B4# AU39
 - SDM_B4 AU37
 - SDQ_B32 AW37
 - SDQ_B33 AV38
 - SDQ_B34 AN37
 - SDQ_B35 AU35
 - SDQ_B36 AR35
 - SDQ_B37 AN35
 - SDQ_B38 AR37
 - SDQ_B39
 - SDQS_B5 AL35
 - SDQS_B5# AL34
 - SDM_B5 AM37
 - SDQ_B40 AM35
 - SDQ_B41 AM38
 - SDQ_B42 AJ34
 - SDQ_B43 AL38
 - SDQ_B44 AR39
 - SDQ_B45 AM34
 - SDQ_B46 AL37
 - SDQ_B47 AL32
 - SDQS_B6 AG35
 - SDQS_B6# AG36
 - SDM_B6 AG39
 - SDQ_B48 AG38
 - SDQ_B49 AJ38
 - SDQ_B50 AF35
 - SDQ_B51 AF33
 - SDQ_B52 AJ35
 - SDQ_B53 AG33
 - SDQ_B54 AF34
 - SDQ_B55
 - SDQS_B7 AC36
 - SDQS_B7# AC37
 - SDM_B7 AD38
 - SDQ_B56 AD36
 - SDQ_B57 AC33
 - SDQ_B58 AA34
 - SDQ_B59 AA36
 - SDQ_B60 AD34
 - SDQ_B61 AF38
 - SDQ_B62 AC34
 - SDQ_B63 AA33
- (20) M_CHB_DQS0 (20)
- (20) M_CHB_DQS0# (20)
- (20) M_CHB_DM0 (20)
- M_CHB_DQ[63..0] (20)
- DDR_B
- SVREF
- SMRCOMPVHOH
- SMRCOMPVOL

pin G18: CRB:NC

pin E18:0:BTX
1:ATX

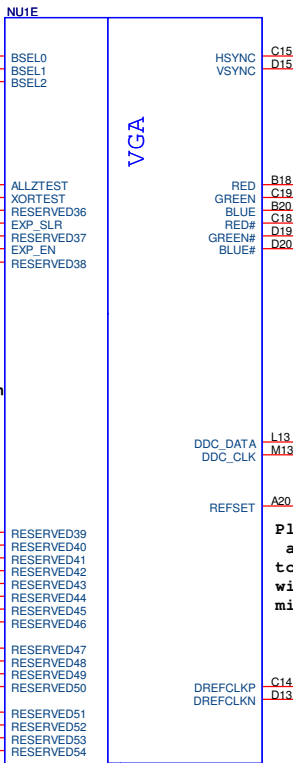
(23) BWEXP_EN
David Dai modify



J17 Pin: EXP & SDVO Concurrent Selection

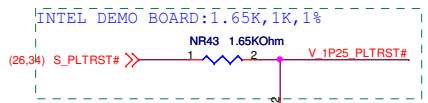
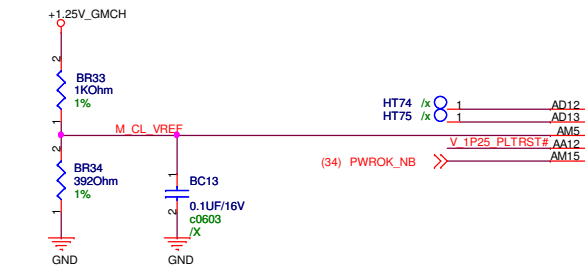
- 0 Only SDVO or PCI EXP Operational
- 1 SDVO and PCI EXP operating via PCI EXP-G port

- HT51 /x 1 L17
- HT52 /x 1 N17
- HT53 /x 1 N18
- HT54 /x 1 N15
- HT55 /x 1 M20
- HT56 /x 1 L15
- HT57 /x 1 L18
- HT58 /x 1 M18

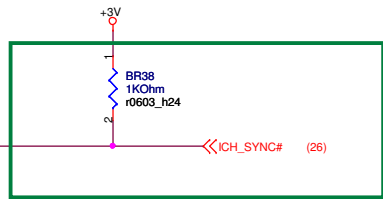
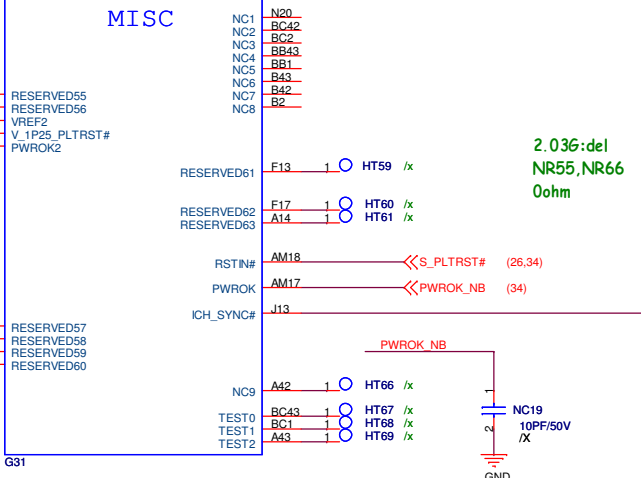


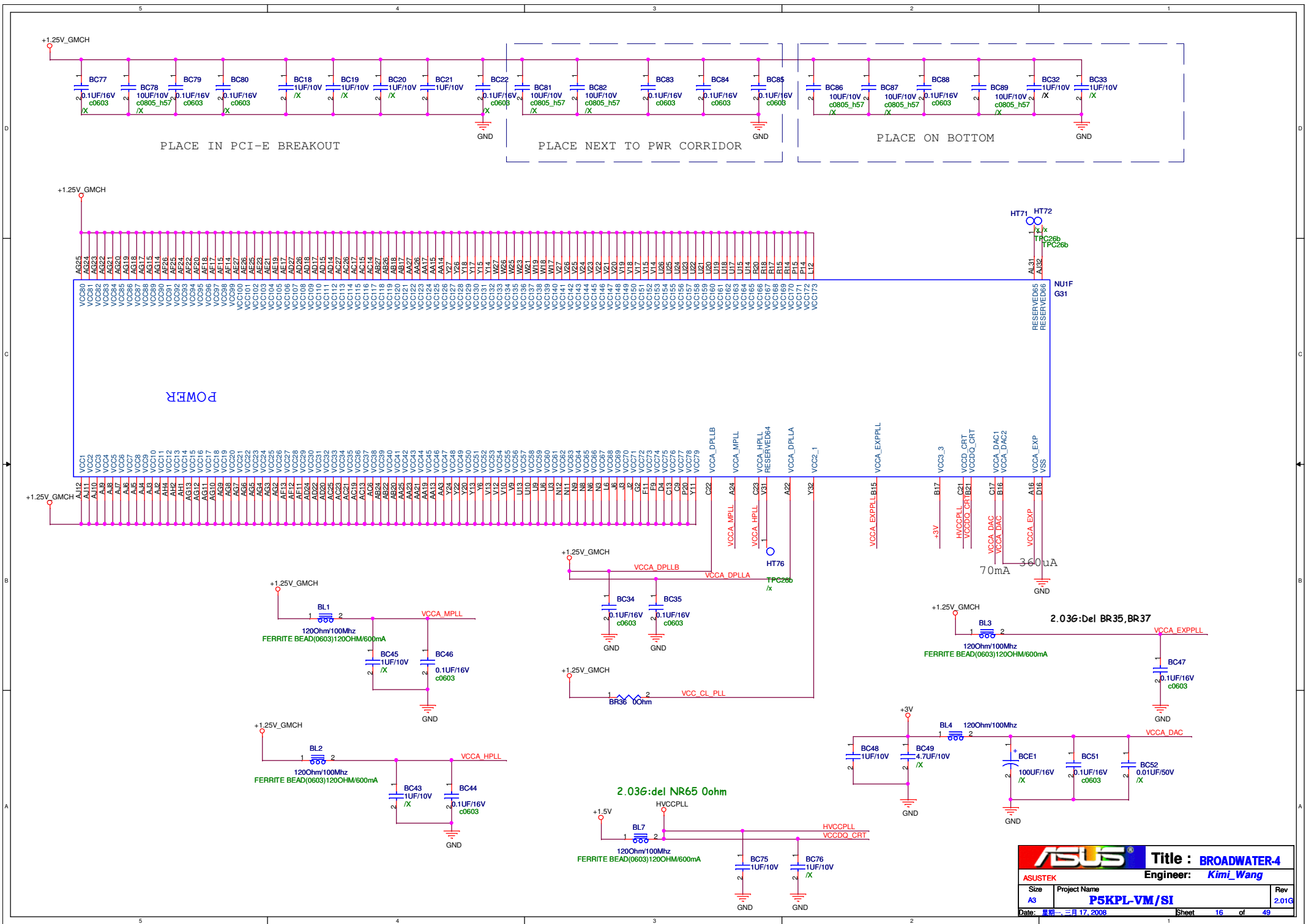
Placed NR64 as close to the GMCH within 500 mils.

MISC

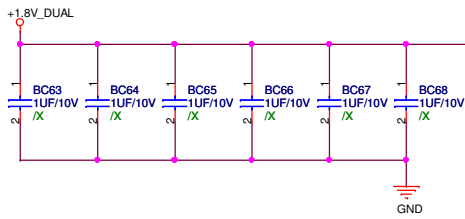
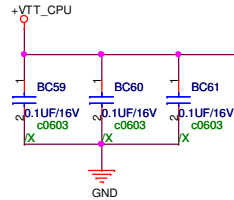
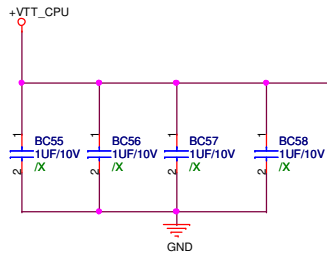


2.03G:change NR43 1.62Kohm to 1.65Kohm for combining component

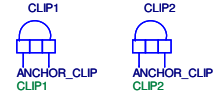
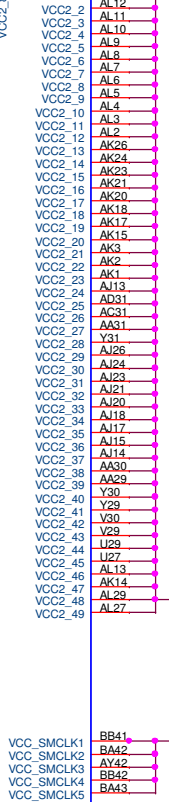
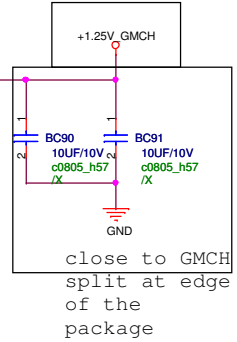
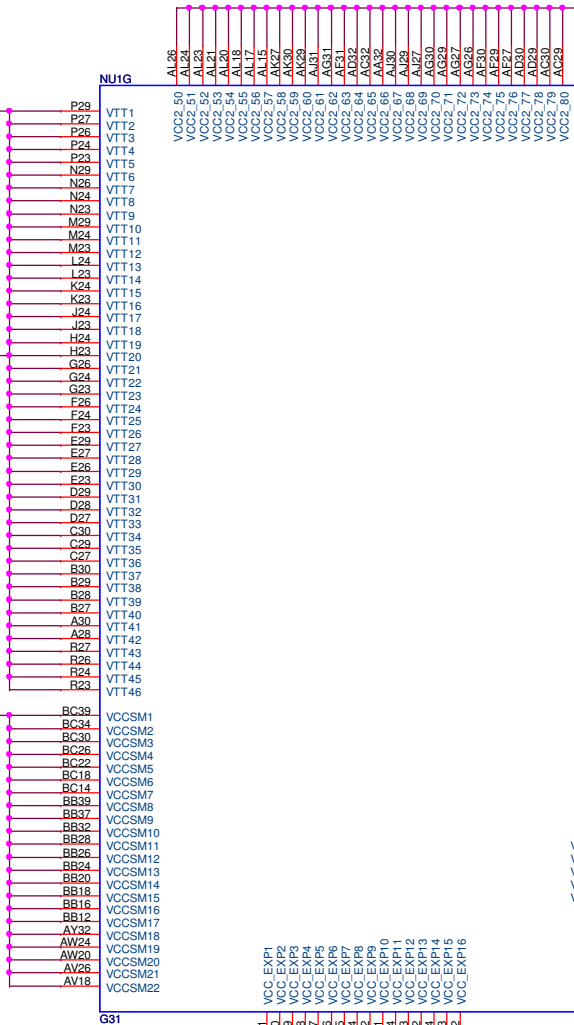
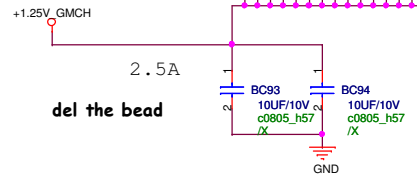
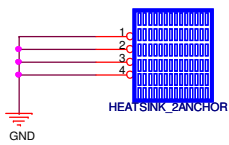


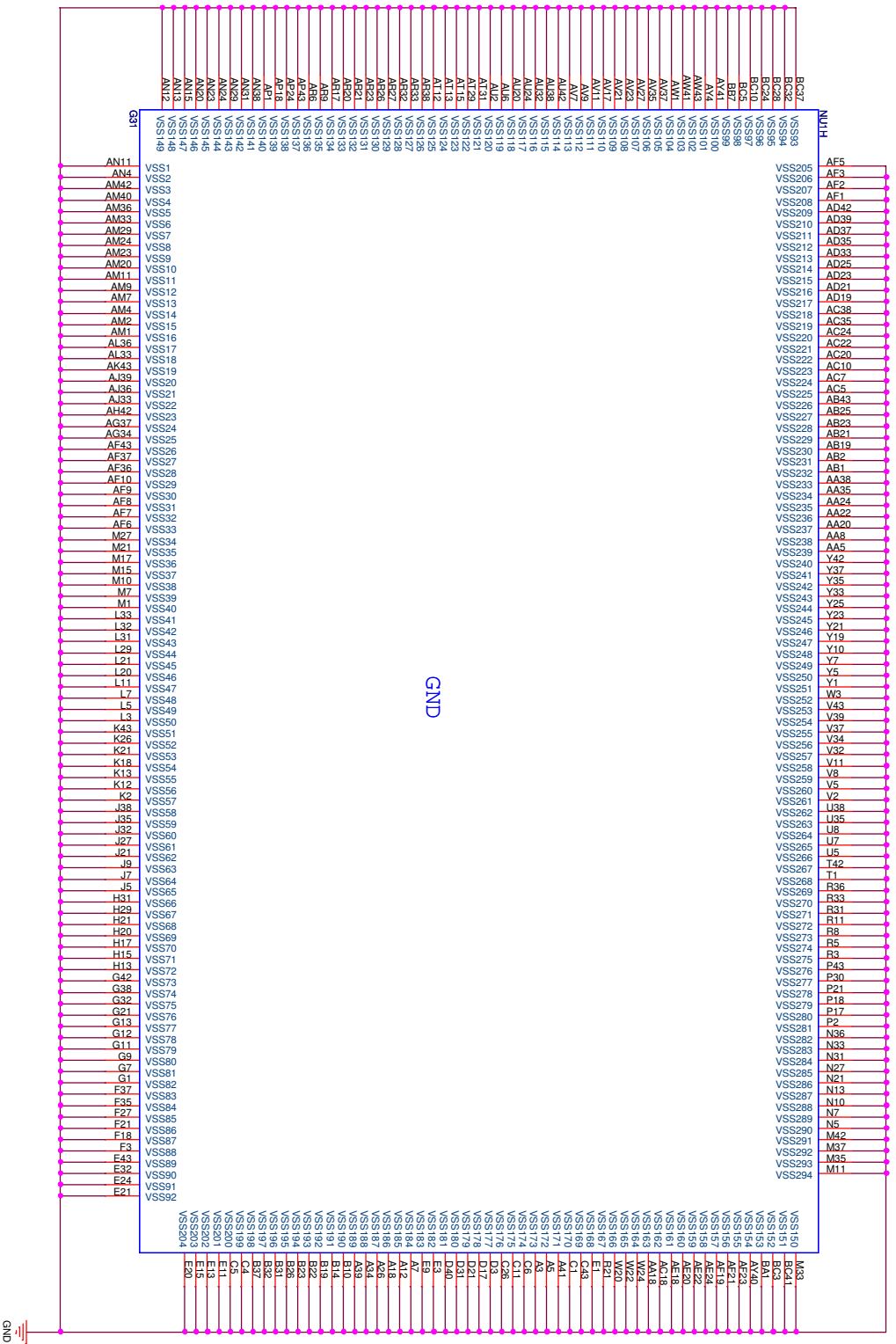


ASUS		Title : BROADWATER-4	
ASUSTEK	Engineer: Kimi_Wang		
Size A3	Project Name PSKPL-VM/SI	Rev 2.01G	
Date: 2008-03-17	Sheet 16	of 49	



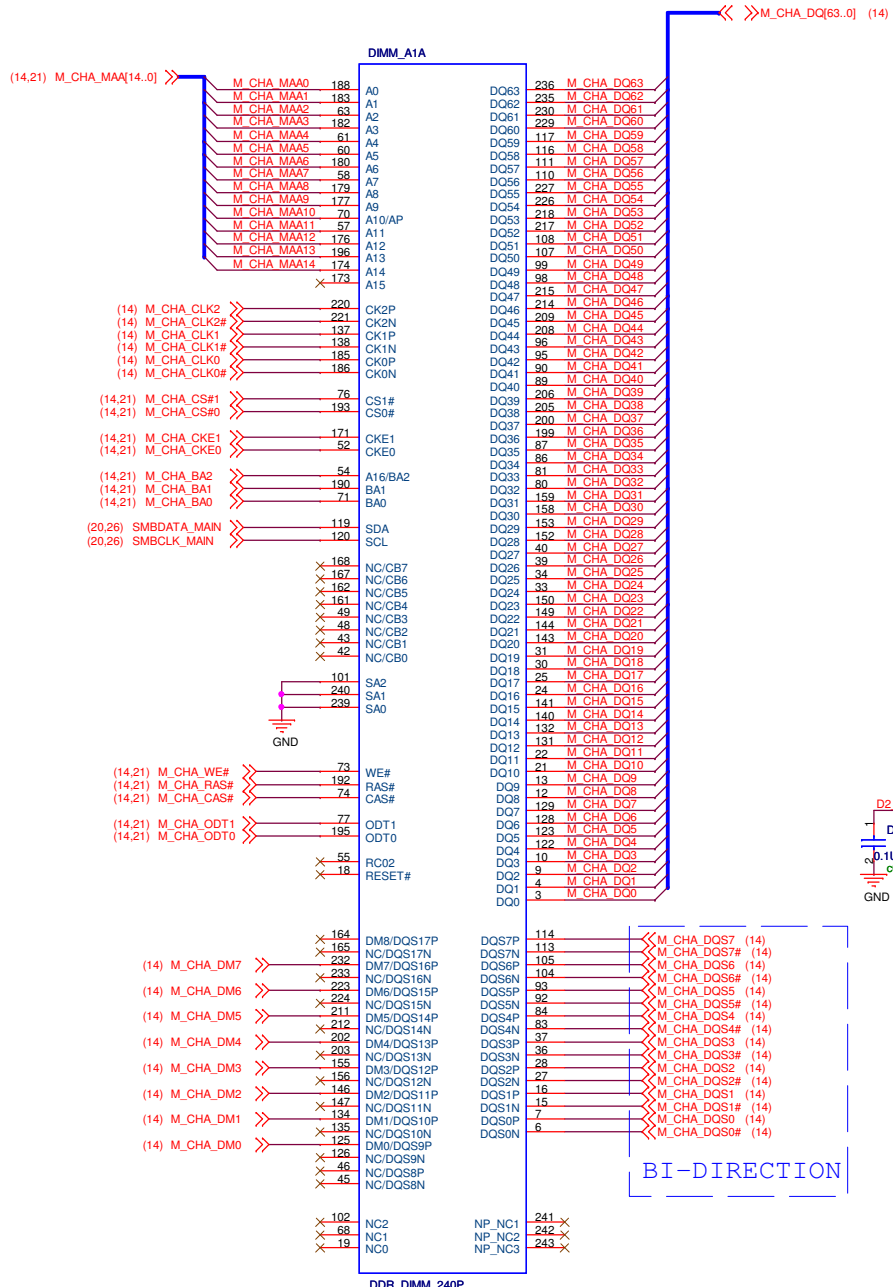
HEATSINK1





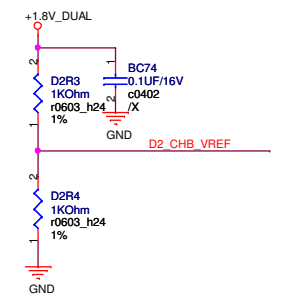
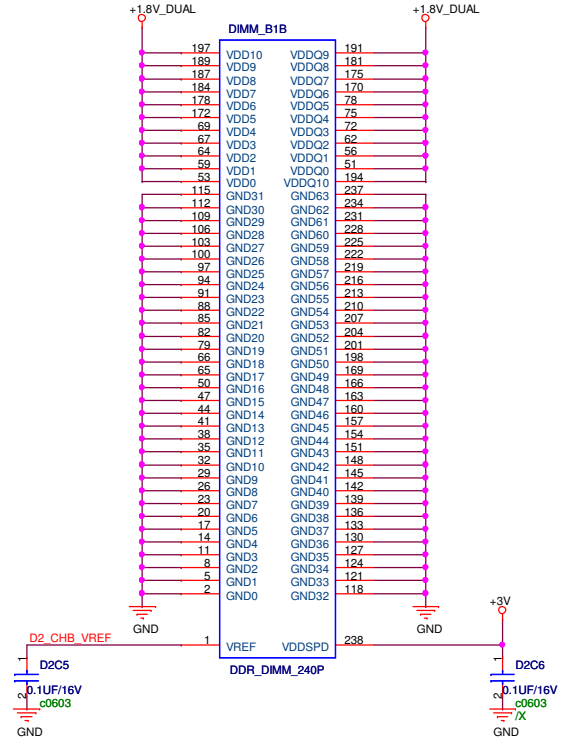
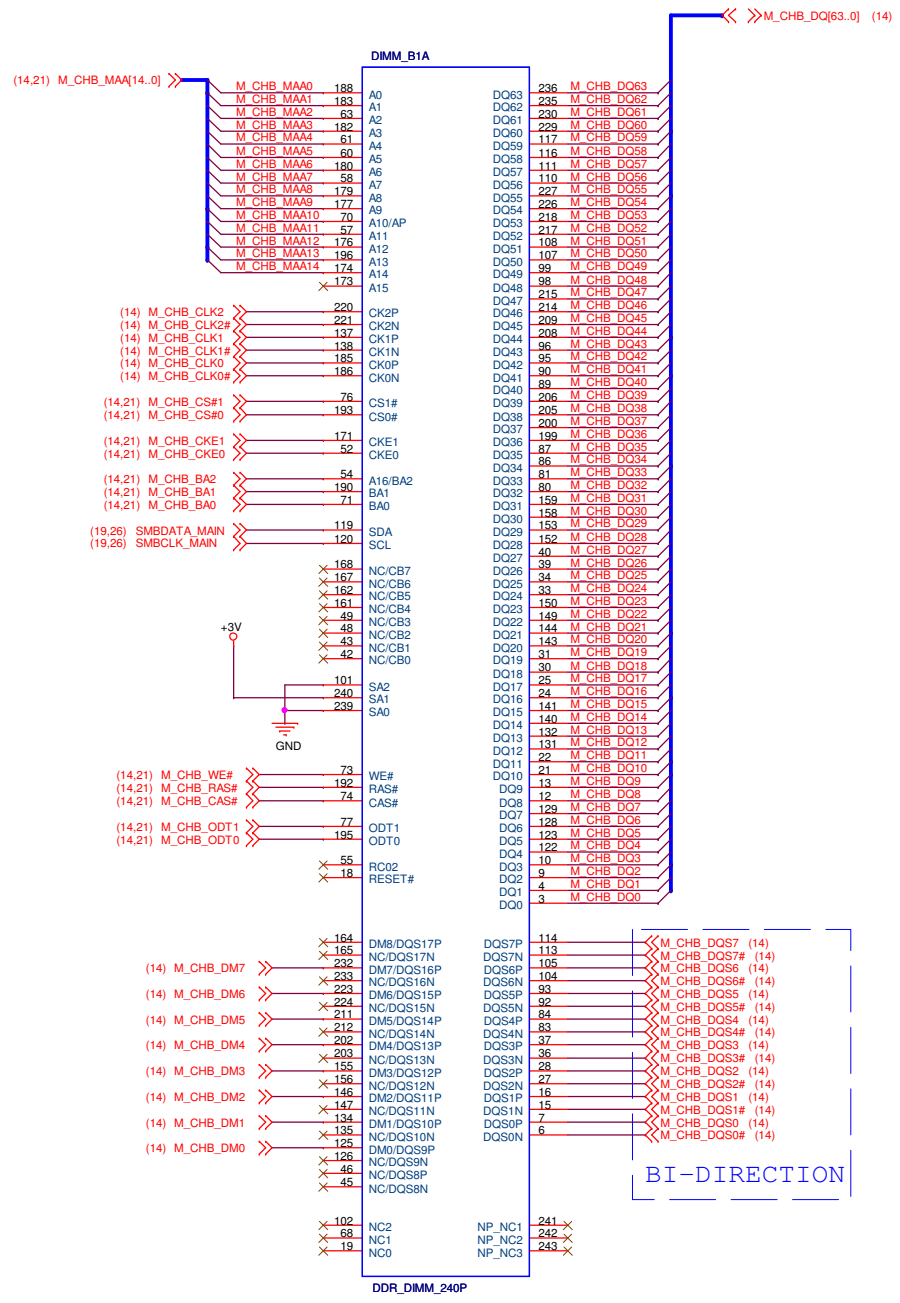
GND

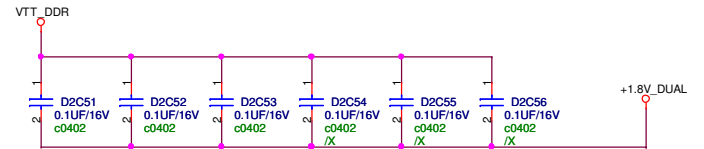
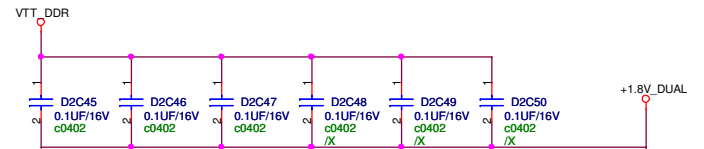
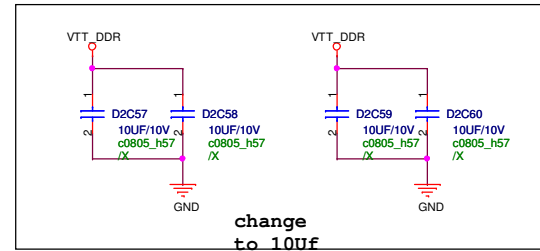
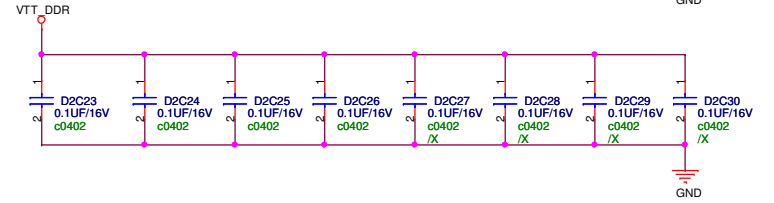
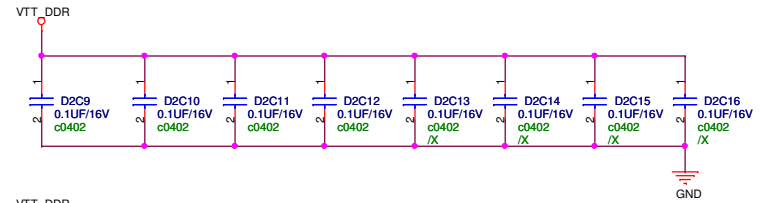
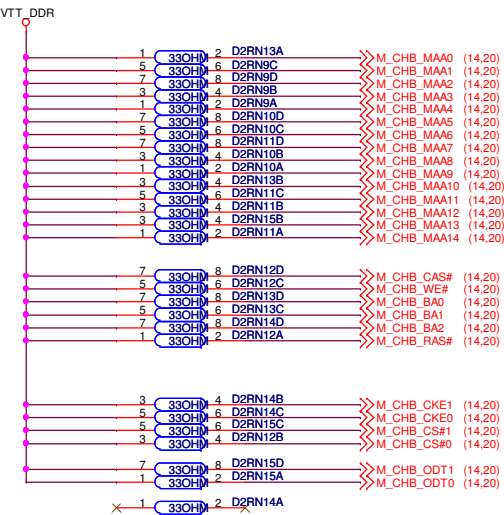
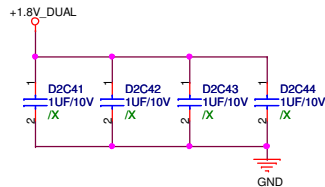
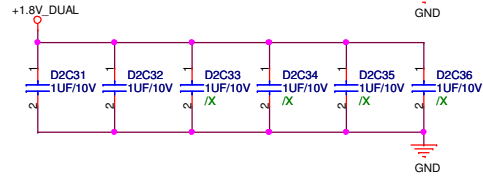
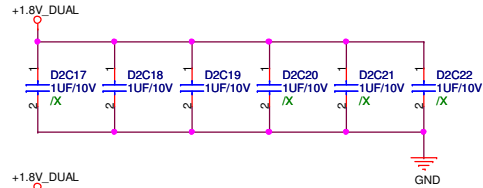
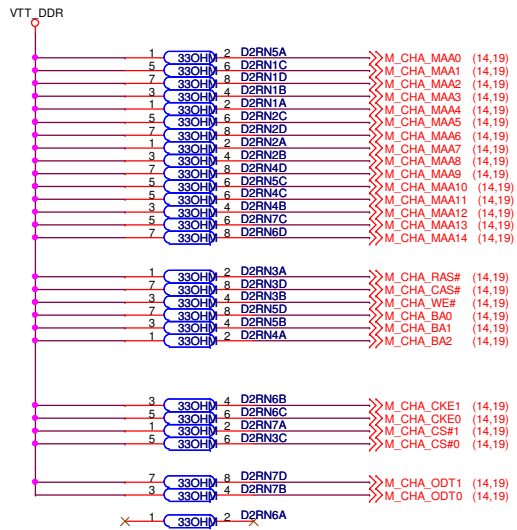
		Title : BROADWATER-6	
		Engineer: Kiml_Wang	
ASUSTEK	Project Name	PSKPL-VM/SI	
Site	Rev	Drawn: MR. SAHIL	Sheet: 18 of 48
A3	2.01G		



BI-DIRECTION

ASUS Title : **DDR2 A**
 ASUSTEK Engineer: **Kimi Wang**
 Size A3 Project Name **PSKPL-VM/SI** Rev 2.01G
 Date: 星期二, 十月 16, 2007 Sheet 19 of 49





5

4

3

2

1

D

D

C

C

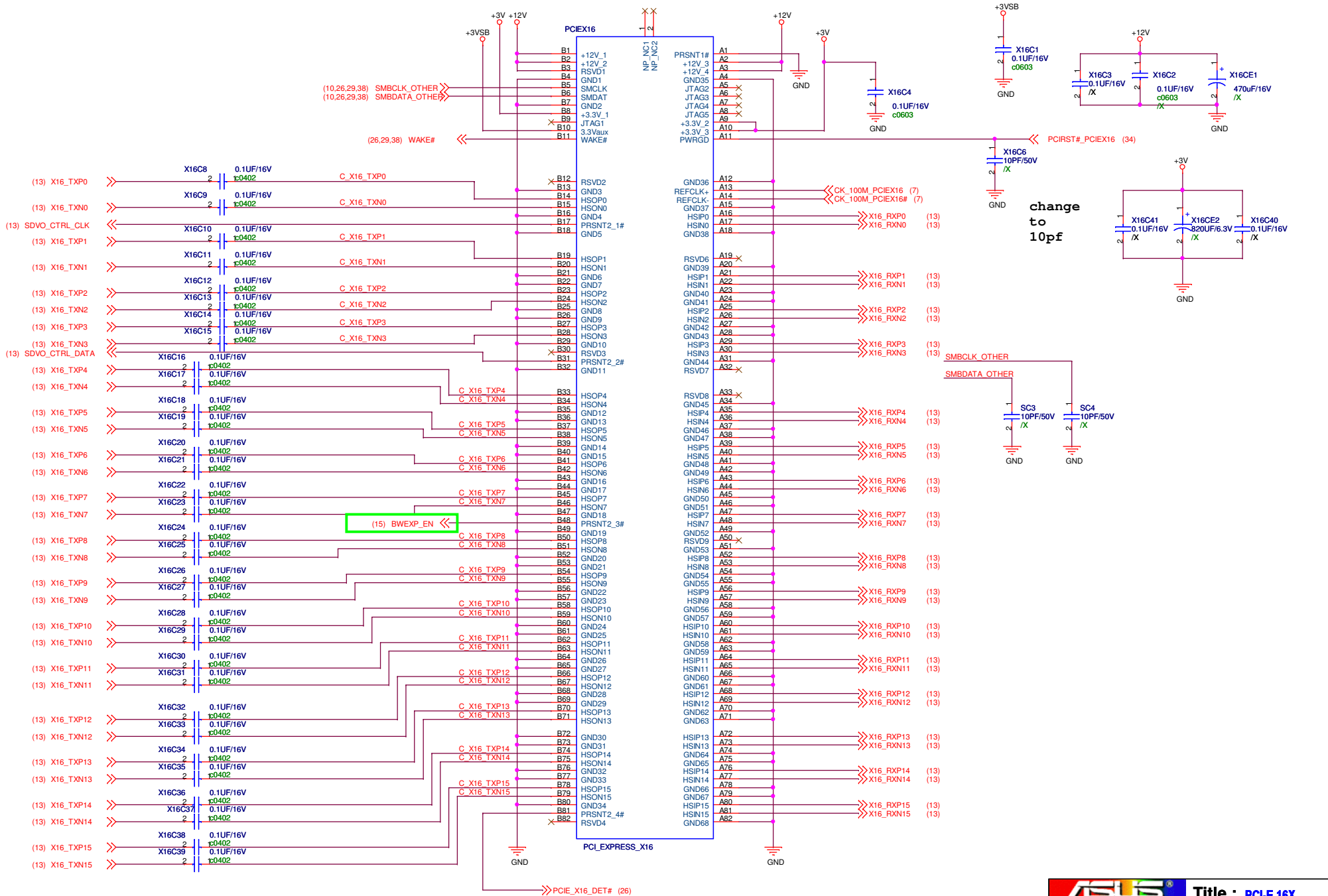
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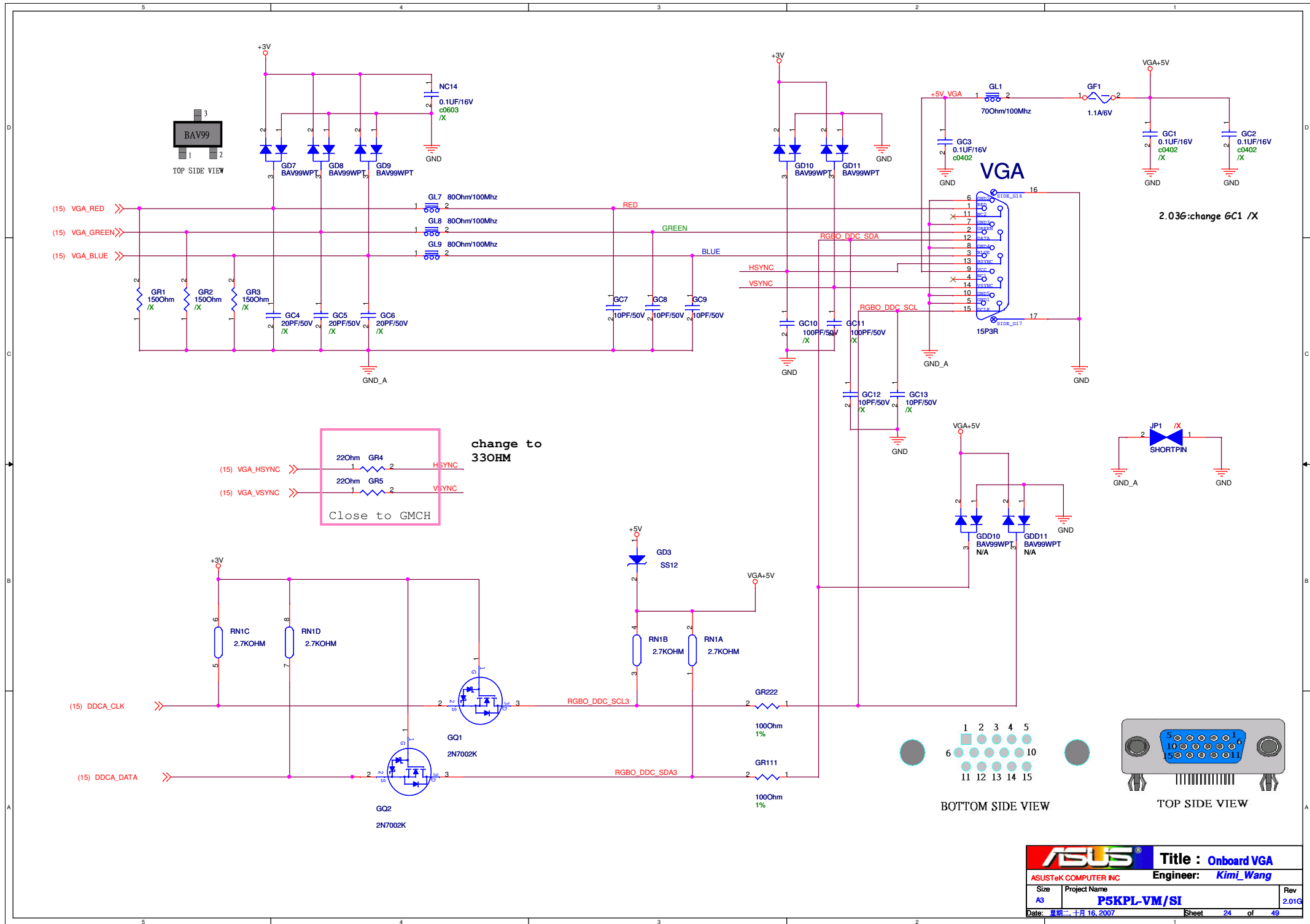
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A

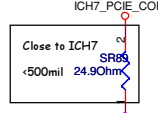
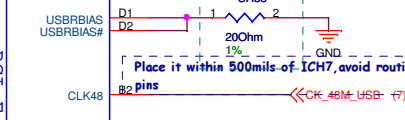
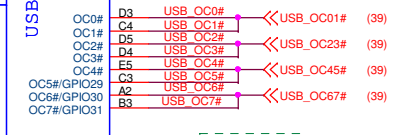
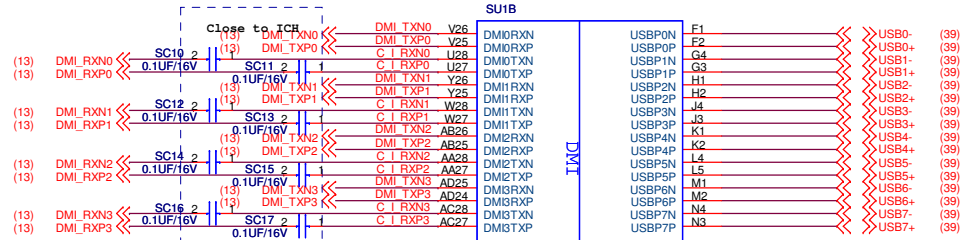
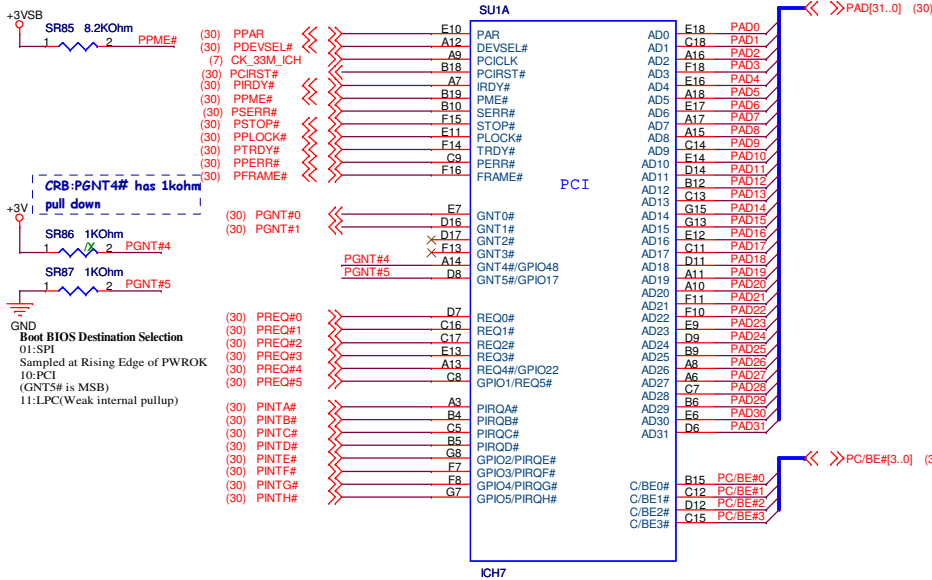
A

		Title :ASM4131	
<small>ASUS</small>		Engineer: Kimi_Wang	
Size	Project Name		Rev
A3	PSKPL-VM/SI		2.01G
Date: 星期二, 十月 16, 2007	Sheet	22	of 49

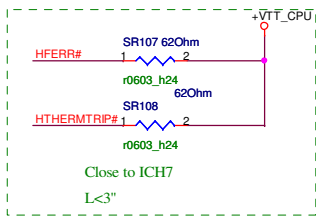
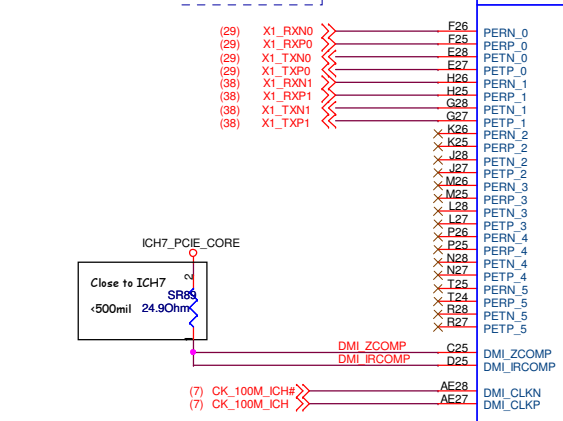
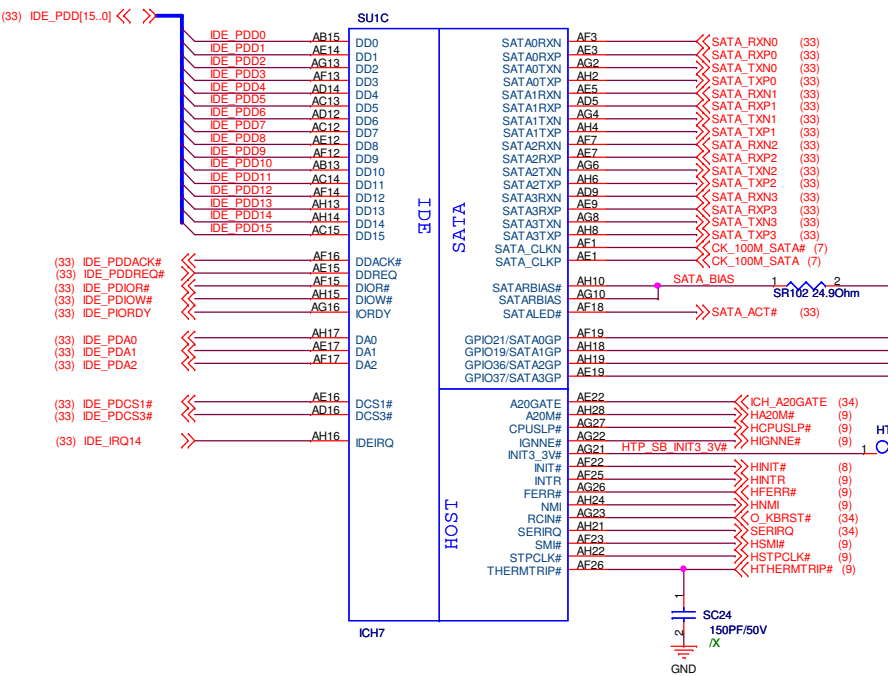


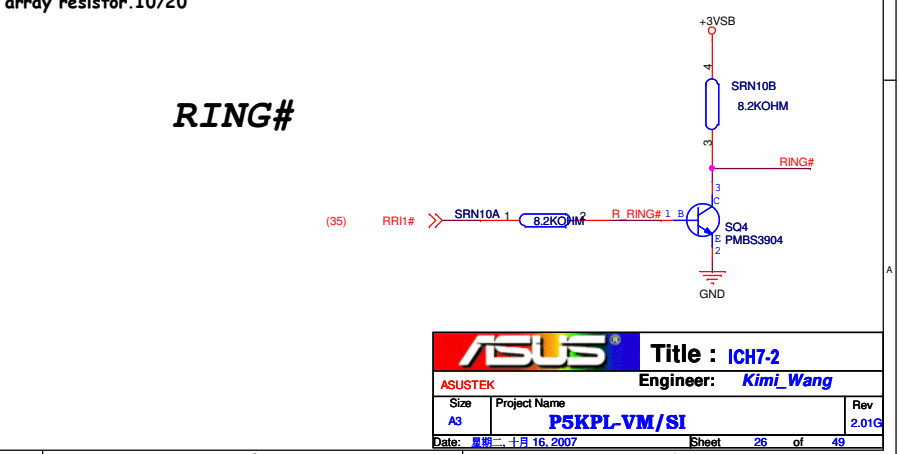
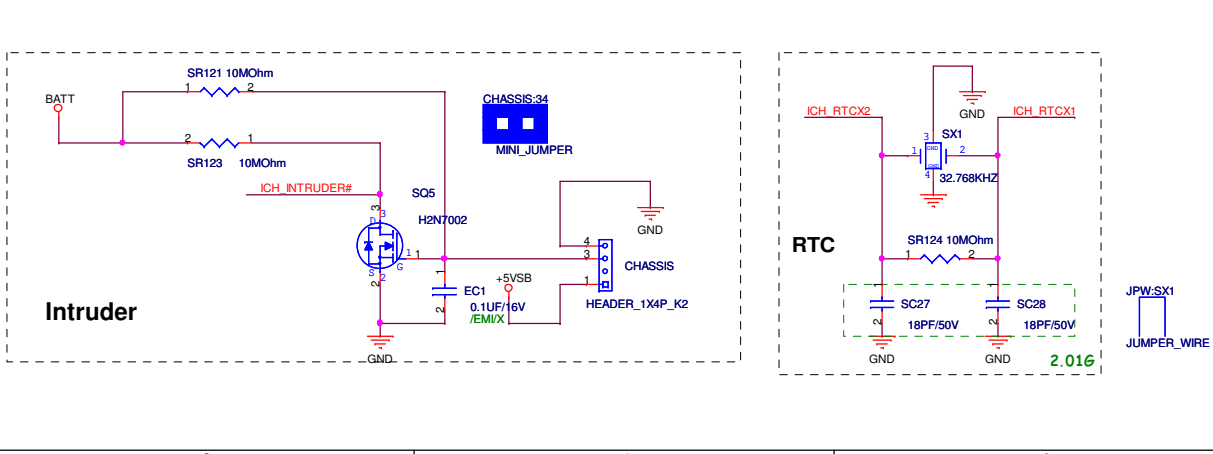
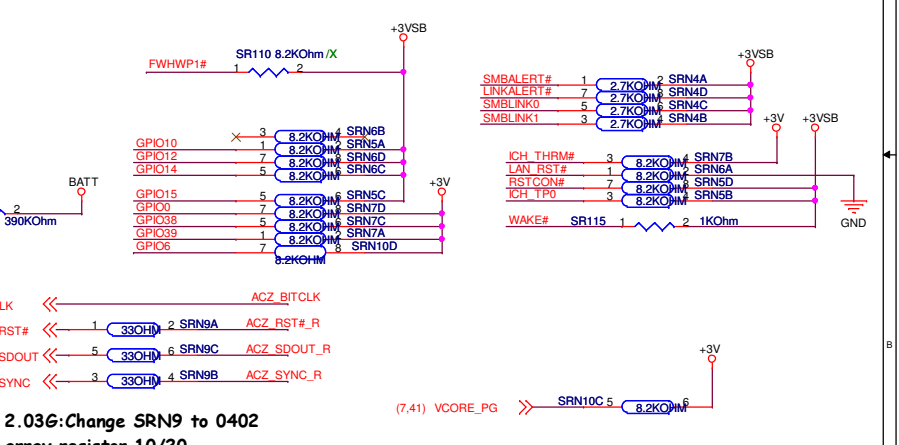
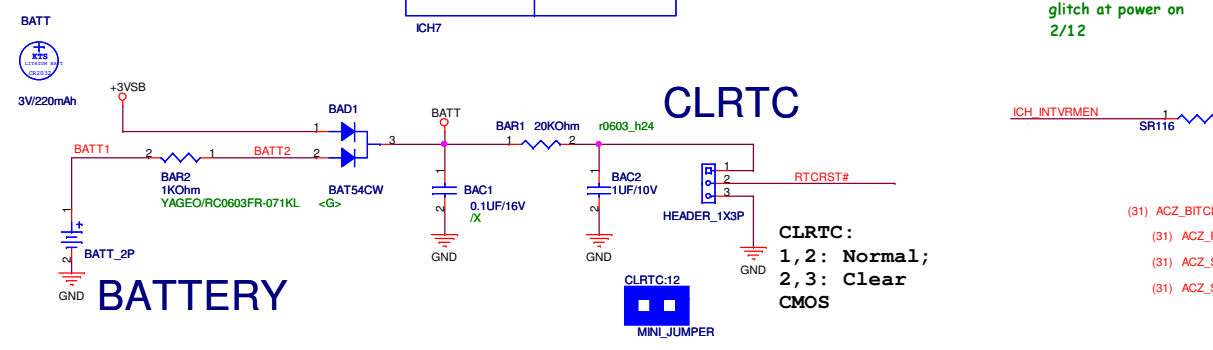
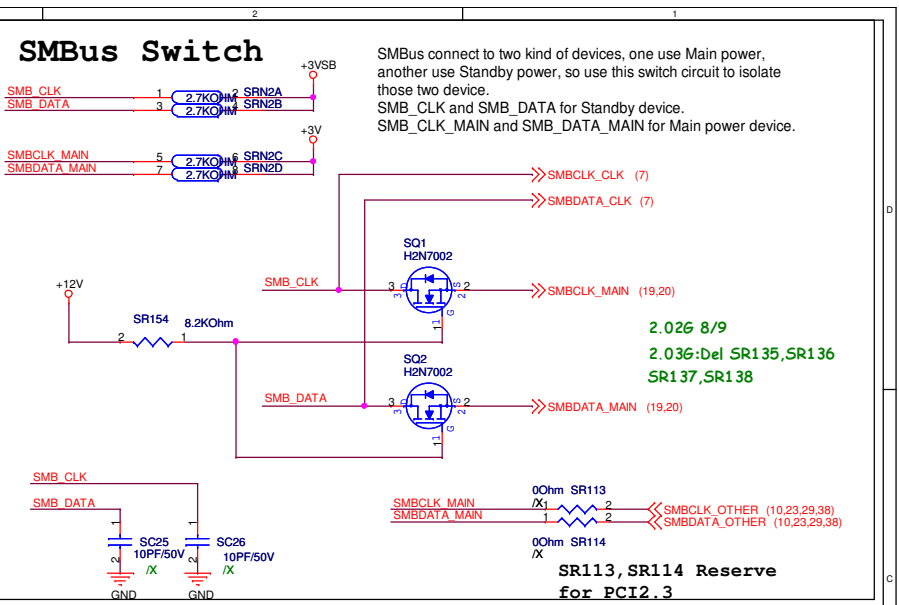
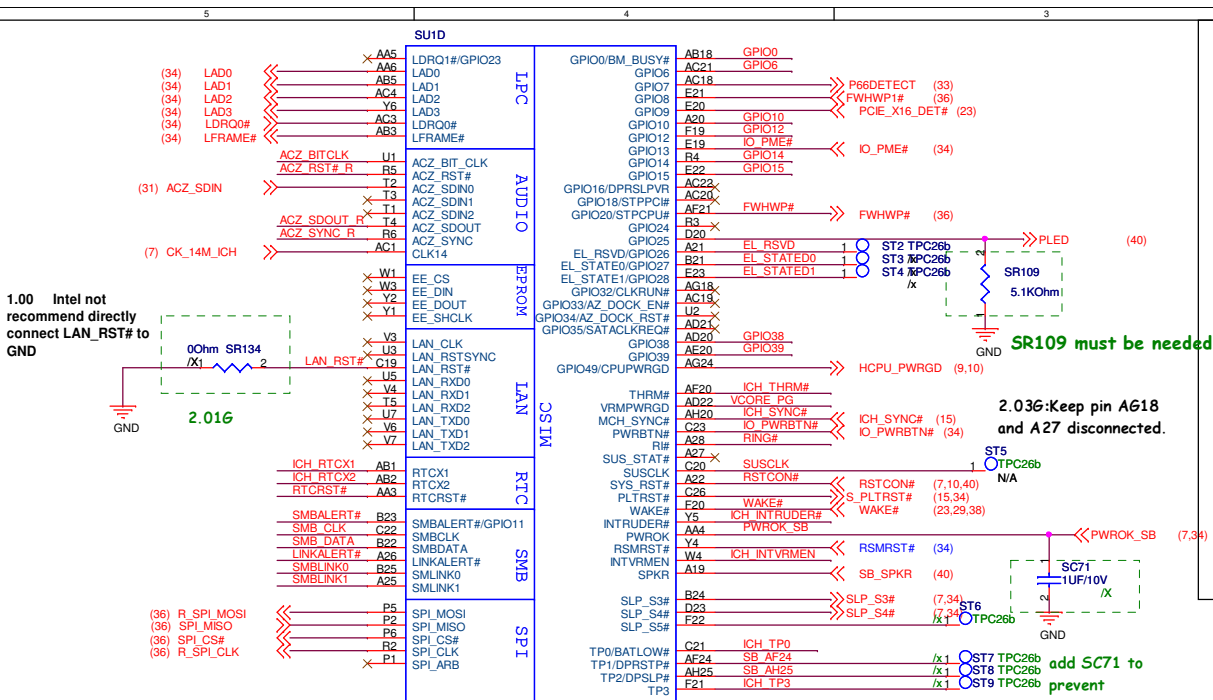


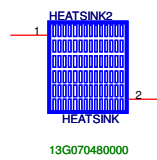
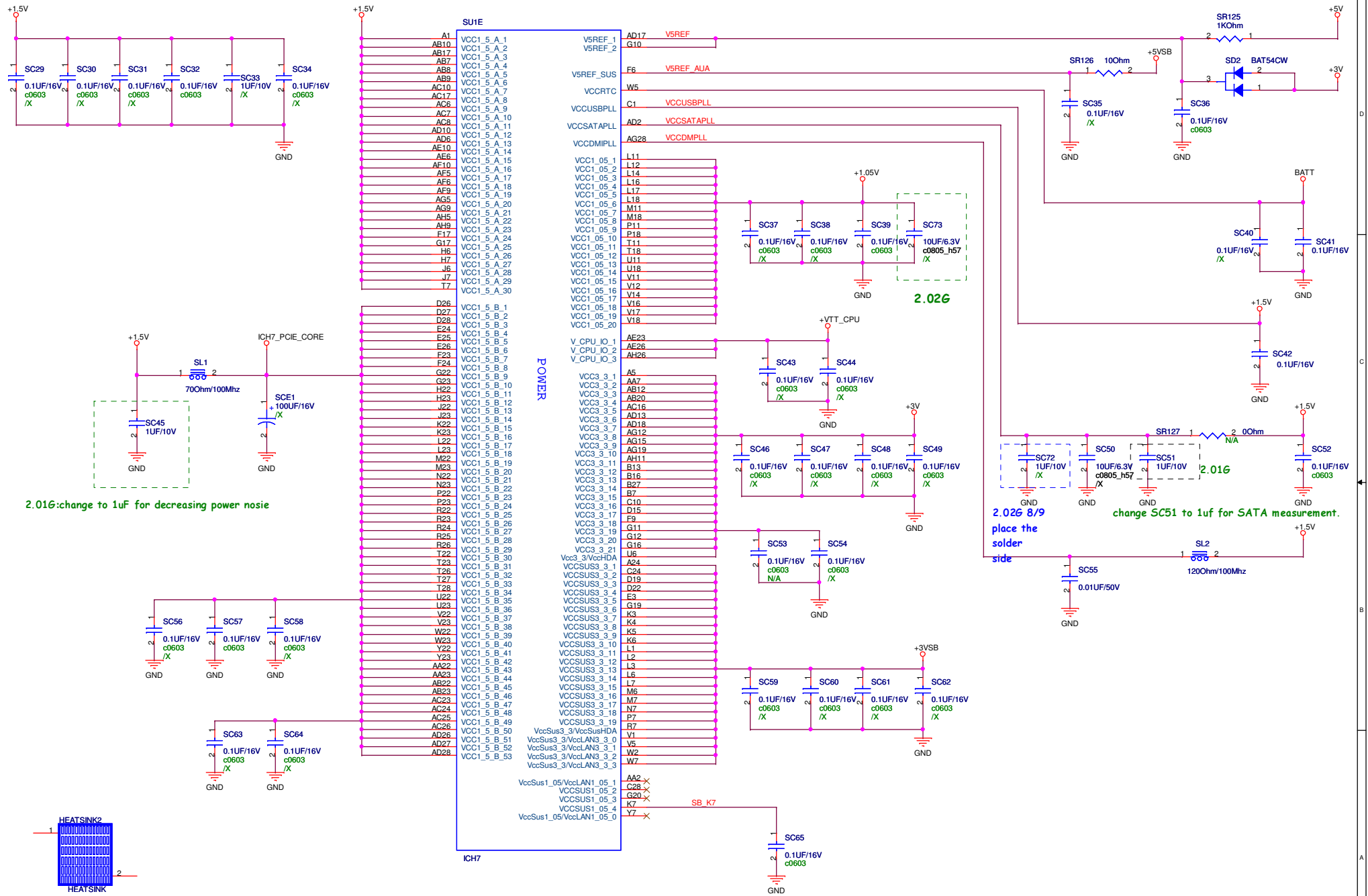
ICH7 will not driver PME# high, but it will be pull up to +3VSB by an internal pull-up resistor

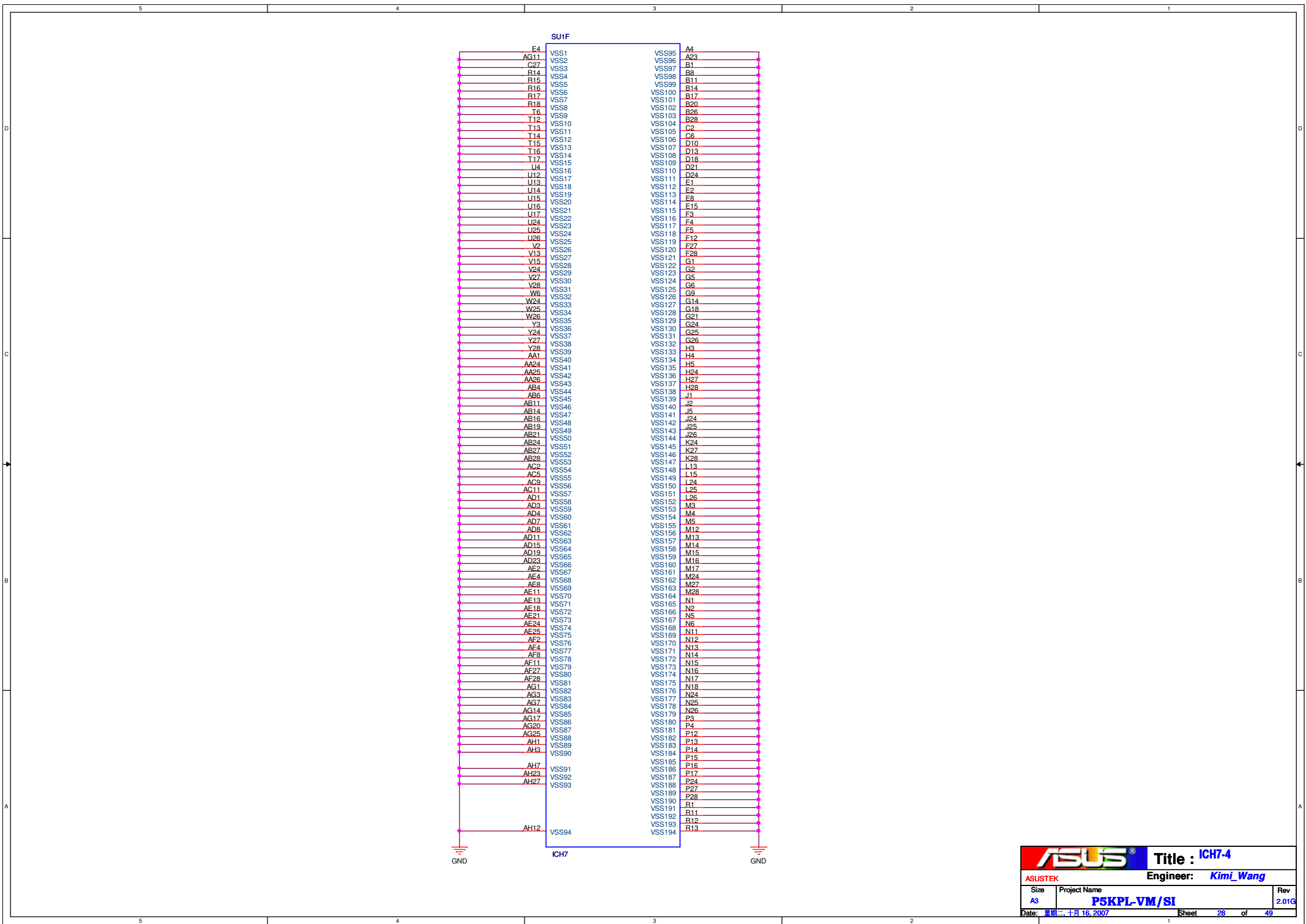


change SR88 to 20.5ohm for testing eyepattern
2.03G:change SR88 to 20ohm for combining component



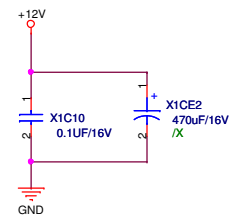
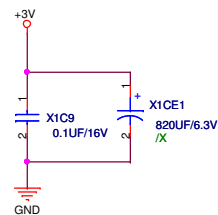
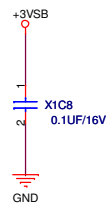
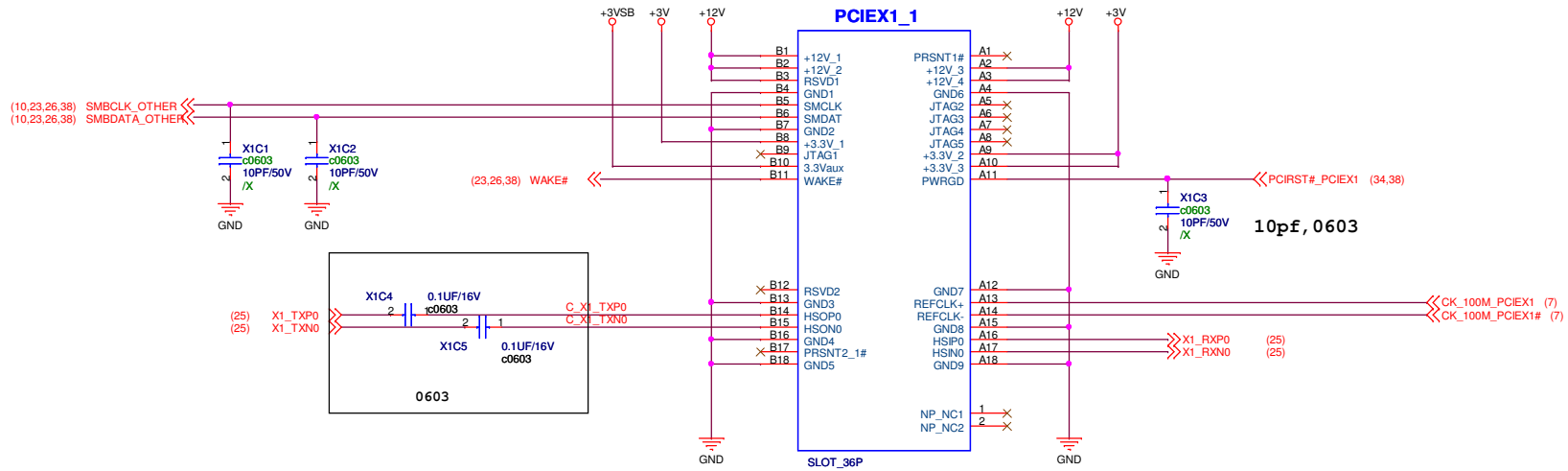


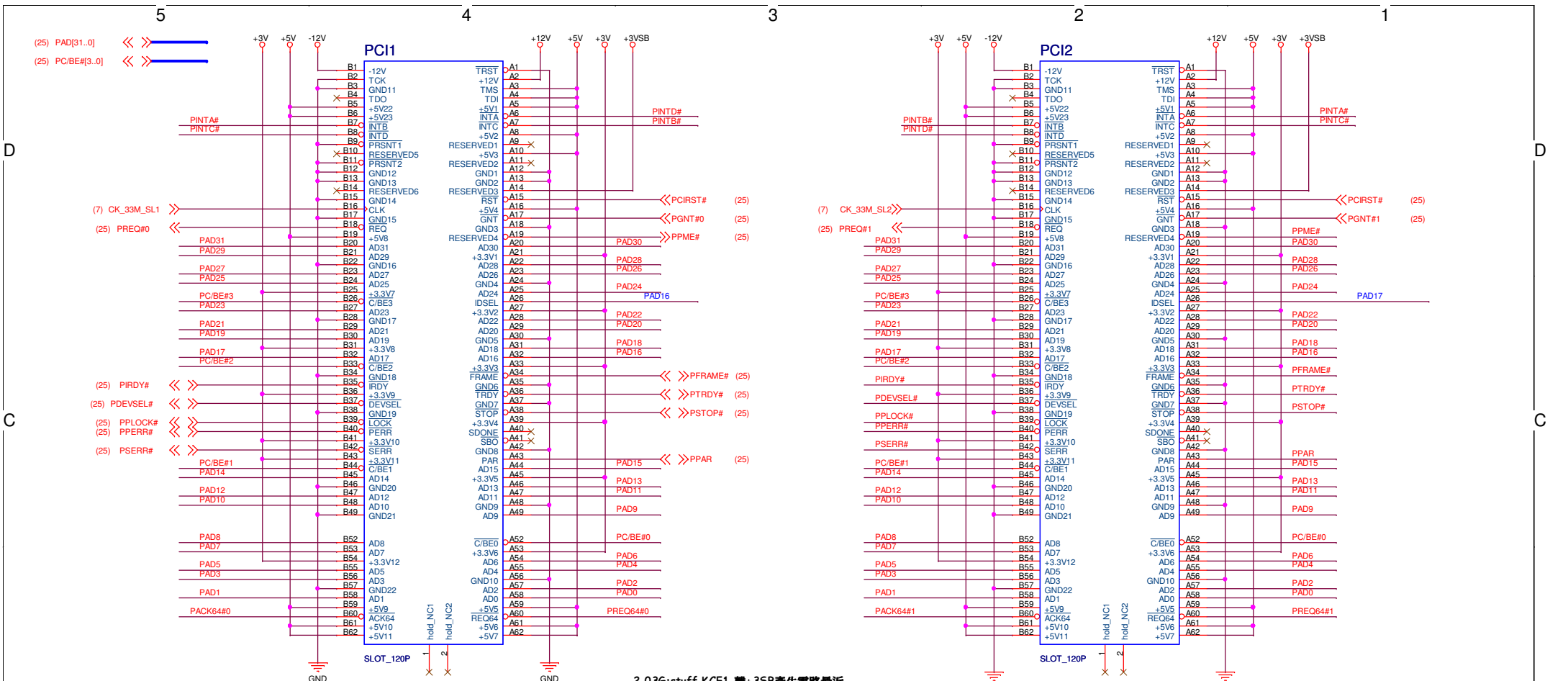




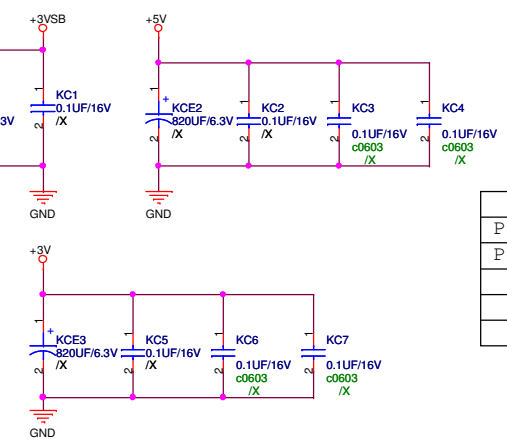
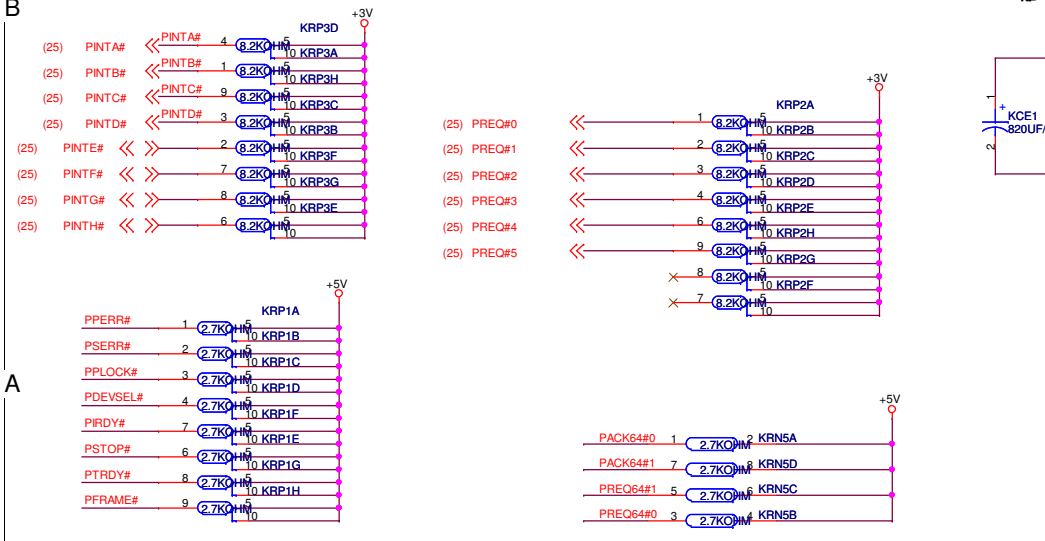
Left Pin Label	Right Pin Label
E4	A4
AG11	A23
C27	B1
R14	B8
R15	B11
R16	B14
R17	B17
R18	B20
T6	B26
T12	B28
T13	C2
T14	C6
T15	D10
T16	D13
T17	D18
U4	D21
U12	D24
U13	E1
U14	E2
U15	E8
U16	F3
U17	F4
U24	F5
U25	F12
U26	F27
V2	F28
V13	G1
V15	G2
V24	G5
V27	G6
V28	G9
W2	G14
W24	G18
W25	G21
W26	G24
Y3	G25
Y24	G26
Y27	H3
Y28	H4
AA1	H5
AA24	H24
AA25	H27
AA26	H28
AB4	J1
AB6	J2
AB11	J5
AB14	J24
AB16	J25
AB19	J26
AB21	K24
AB24	K27
AB27	K28
AC2	L13
AC5	L15
AC9	L24
AC11	L25
AD1	L26
AD3	M3
AD4	M4
AD7	M5
AD8	M12
AD11	M13
AD15	M14
AD19	M15
AD23	M16
AE2	M17
AE4	M24
AE5	M27
AE11	M28
AE13	N1
AE18	N2
AE21	N5
AE24	N6
AE25	N11
AF2	N12
AF4	N13
AF8	N14
AF11	N15
AF27	N16
AF28	N17
AG1	N18
AG3	N24
AG7	N25
AG14	N26
AG17	P3
AG20	P4
AG25	P12
AH1	P13
AH3	P14
AH7	P15
AH23	P16
AH27	P17
	P24
	P27
	P28
	R1
	R11
	R12
	R13
AH12	

ASUS		Title : ICH7-4	
ASUSTEK		Engineer: <i>Kimi_Wang</i>	
Size	Project Name	Rev	
A3	PSKPL-VM/SI	2.01G	
Date:	星期二, 十月 16, 2007	Sheet	28 of 49





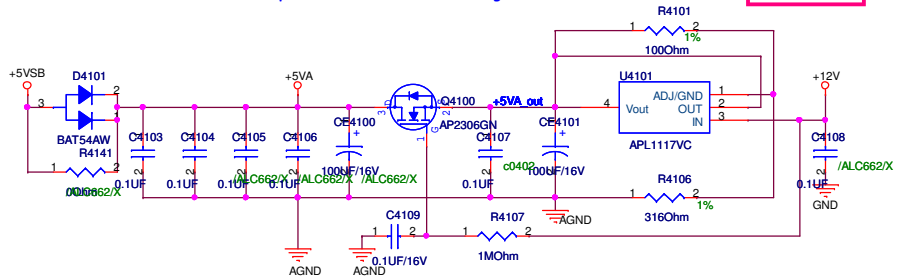
2.03G:stuff KCE1 繼+35B產生電路最近.



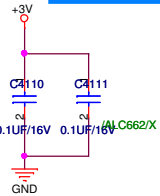
DEVICE	REQ#	GNT#	INTERRUPT	ID_SEL
PCI SLOT 1	0	0	DABC	AD_16
PCI SLOT 2	1	1	ABCD	AD_17

You must mount at least one DIP capacitor on +5VSB, or the regulator will be destroyed.

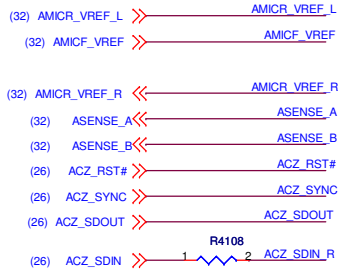
AVDD



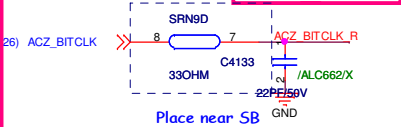
DVDD



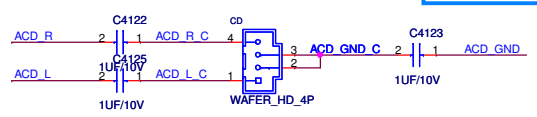
OFF PAGE



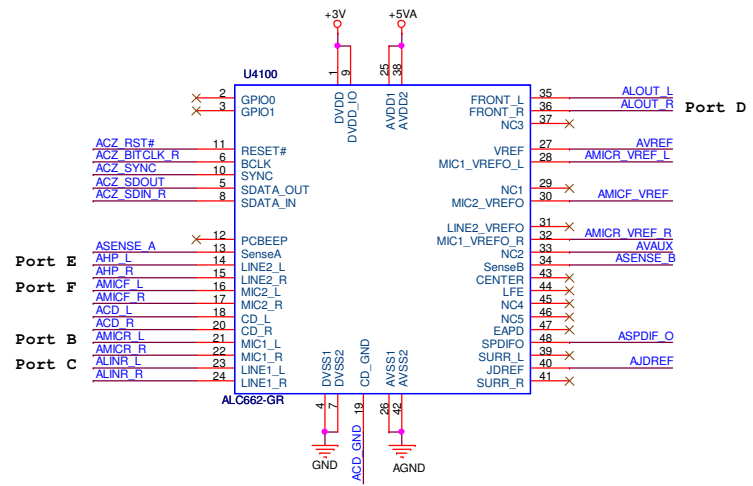
BIT CLK



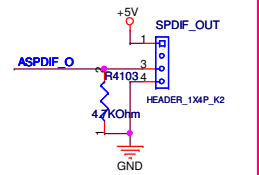
CD-IN



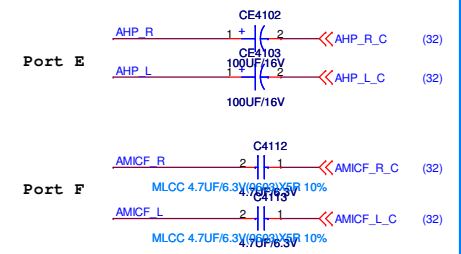
CODEC ALC662



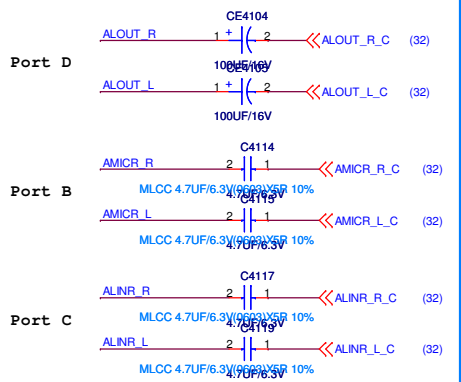
SPDIF OUT



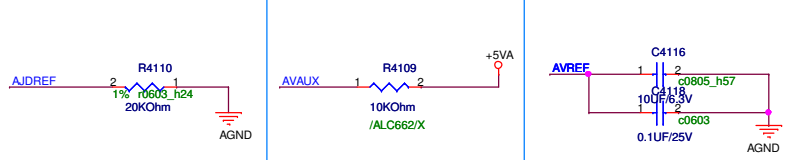
FRONT PANEL AUDIO



REAR PANEL AUDIO



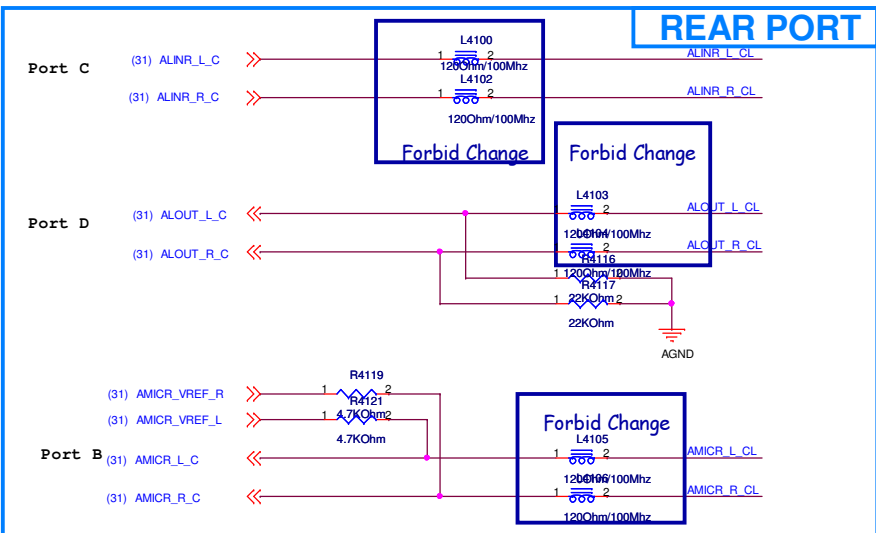
REF & FILTERS



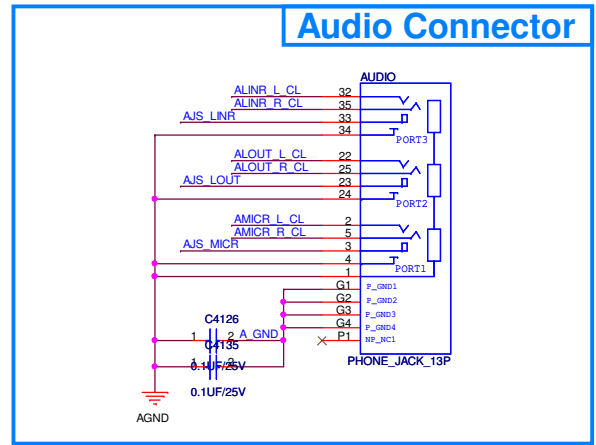
DEMO CIRCUIT

M2	ALC662
AZALIA	ALC662
REV.	1.01

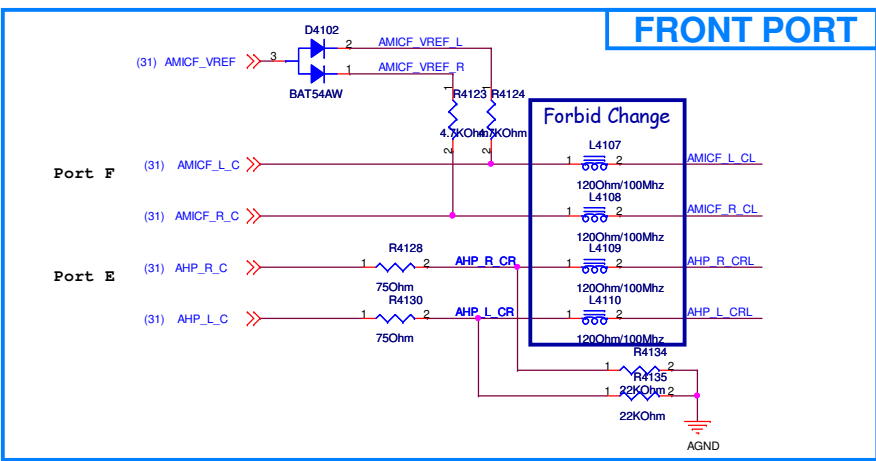
REAR PORT



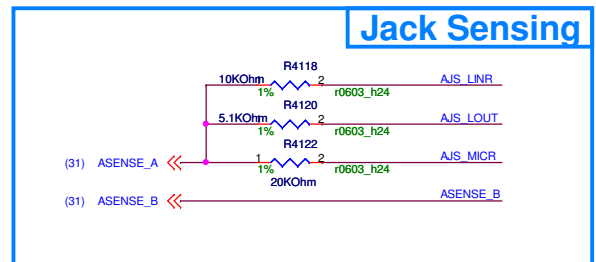
Audio Connector



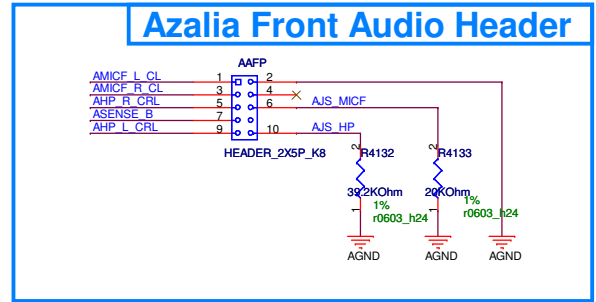
FRONT PORT



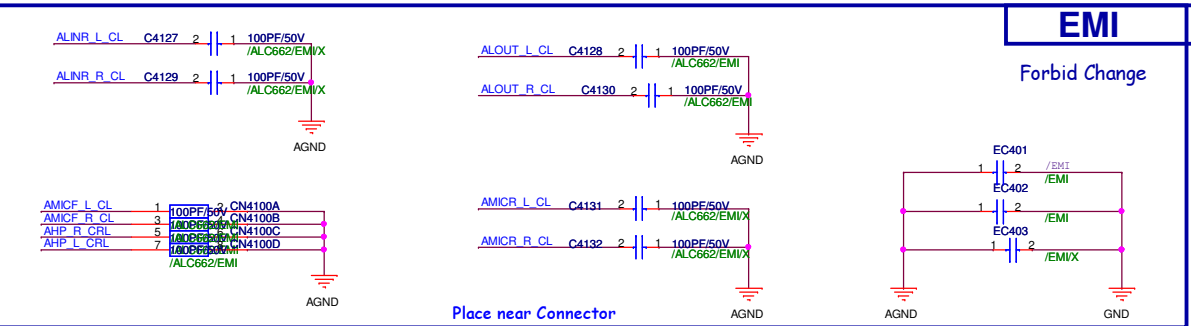
Jack Sensing



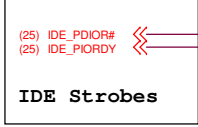
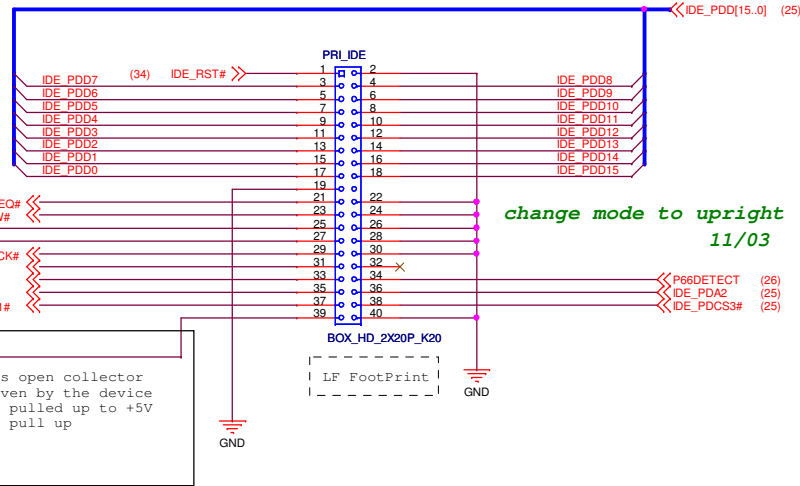
Azalia Front Audio Header



EMI

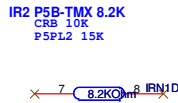
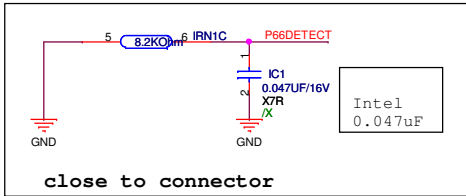
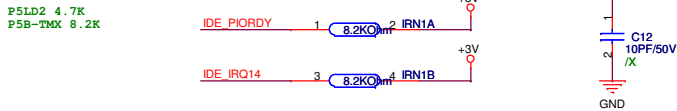


IDE

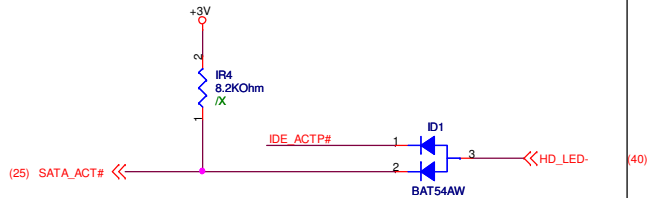


IDE ACTP#
This pin is open collector output driven by the device. Device has pulled up to +5V. MB need no pull up.

[IR1] Demo Circuit use 4.7k

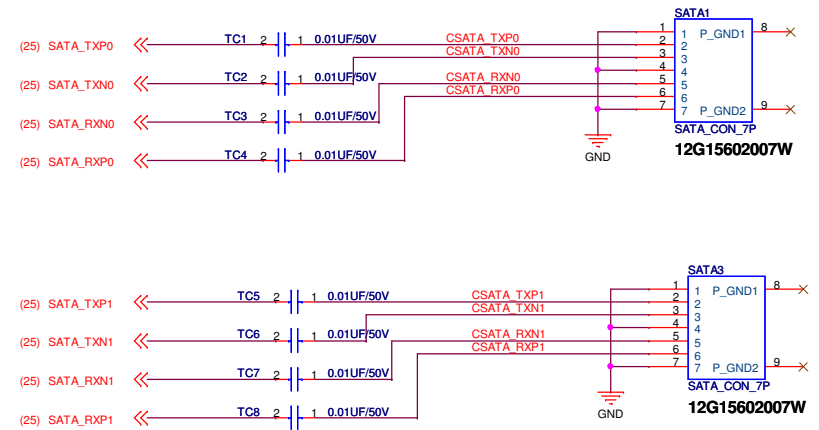


IDE & SATA LED

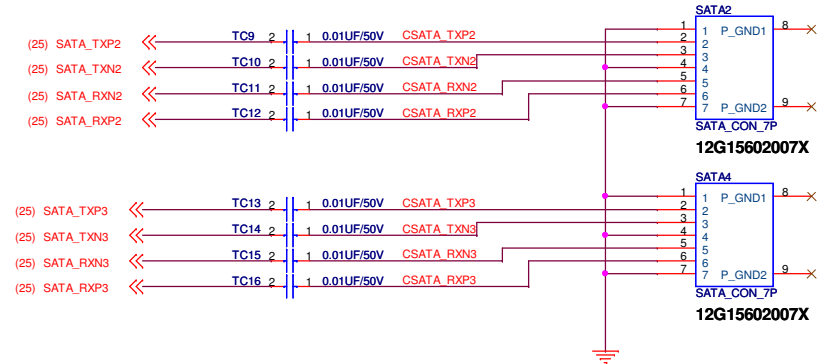


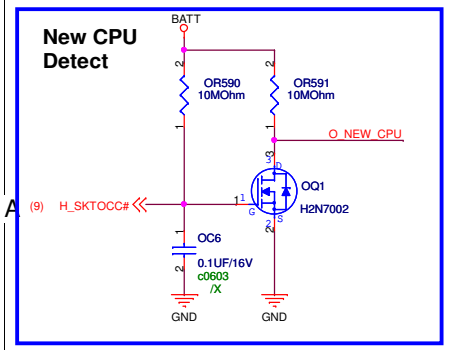
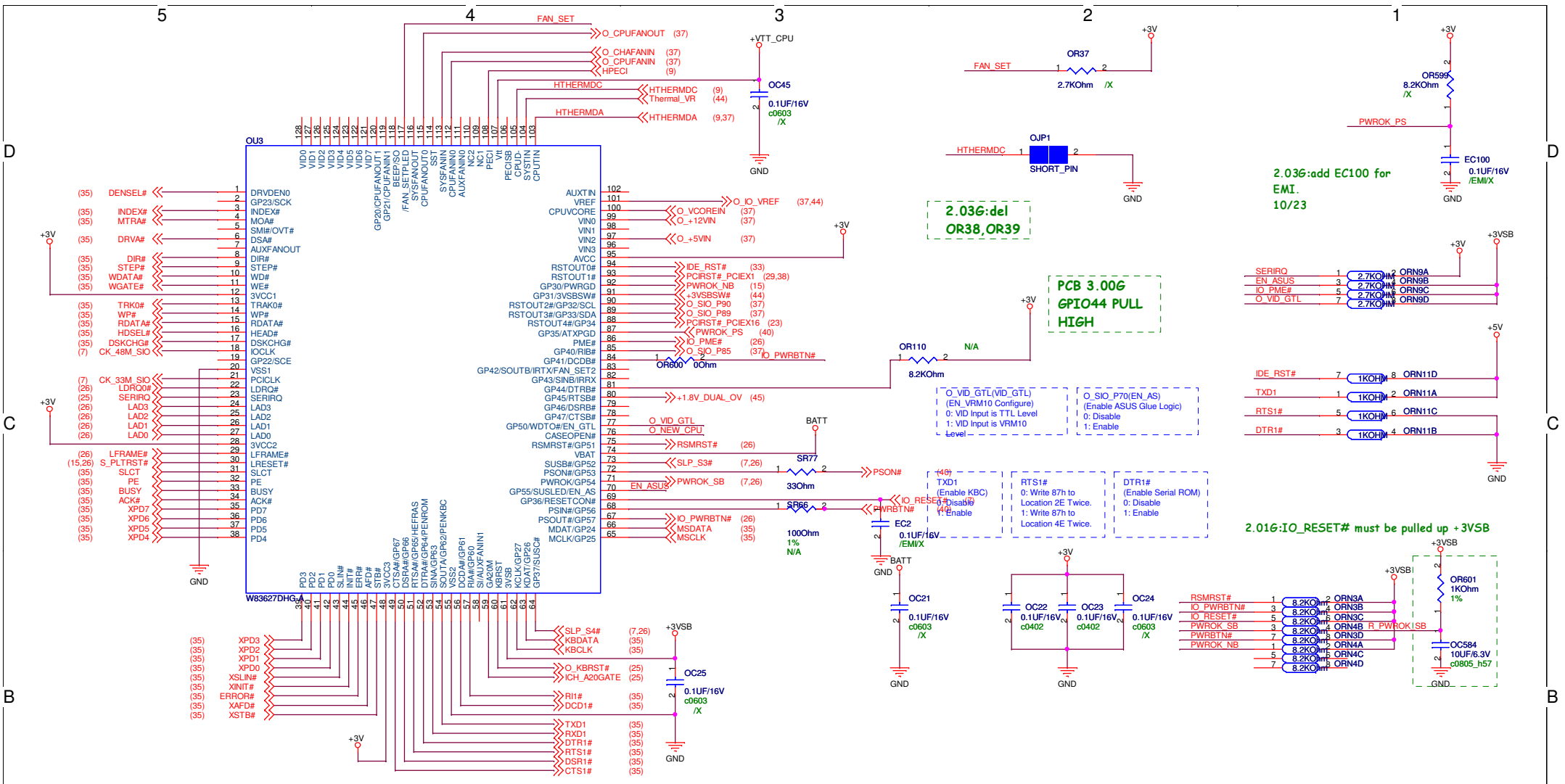
Serial ATA

Color: RED

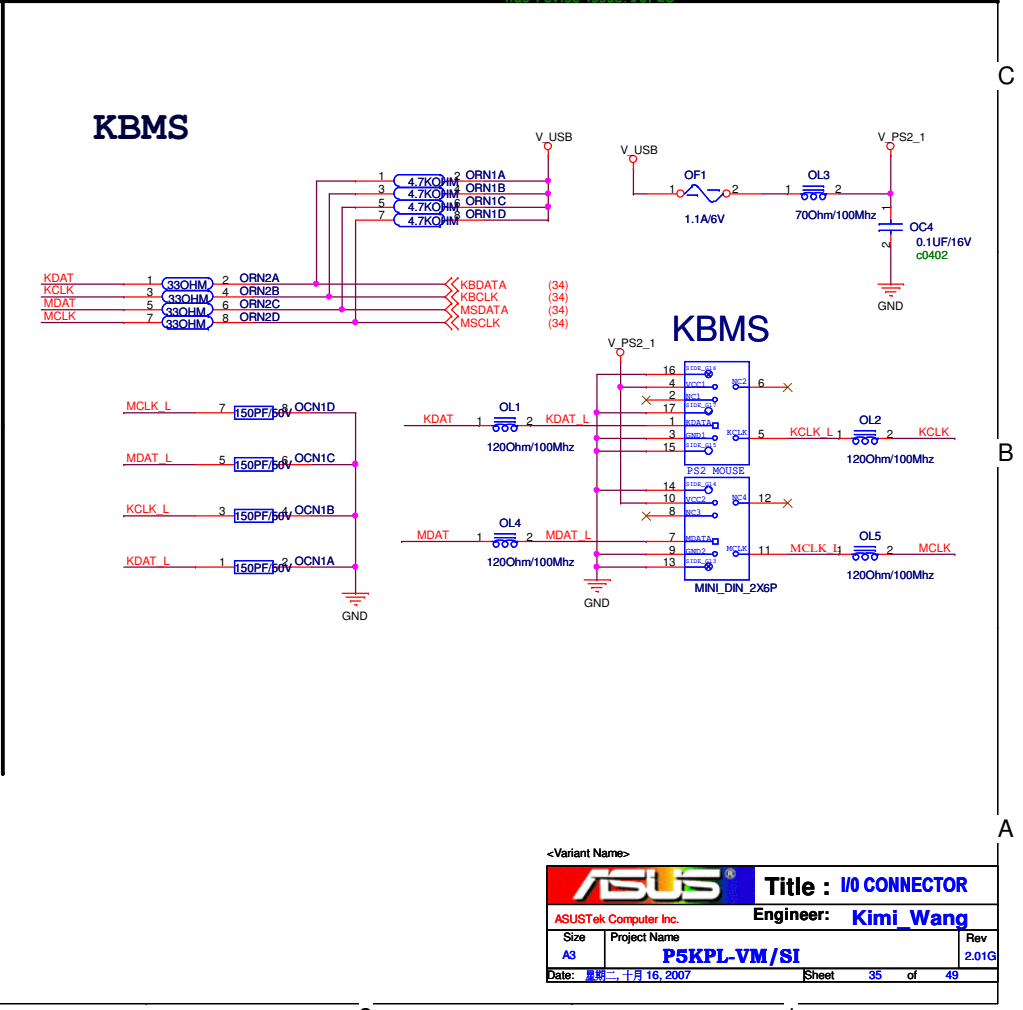
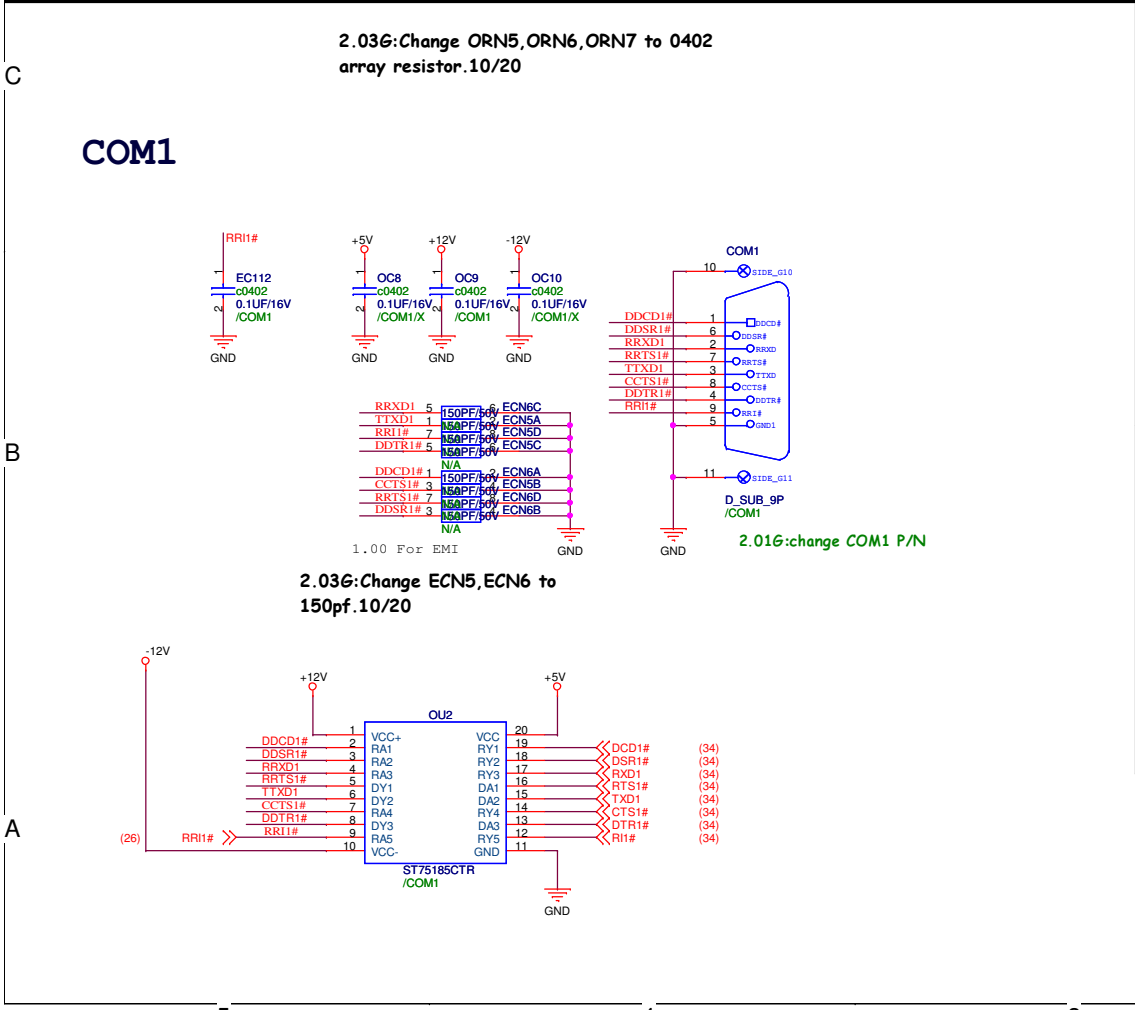
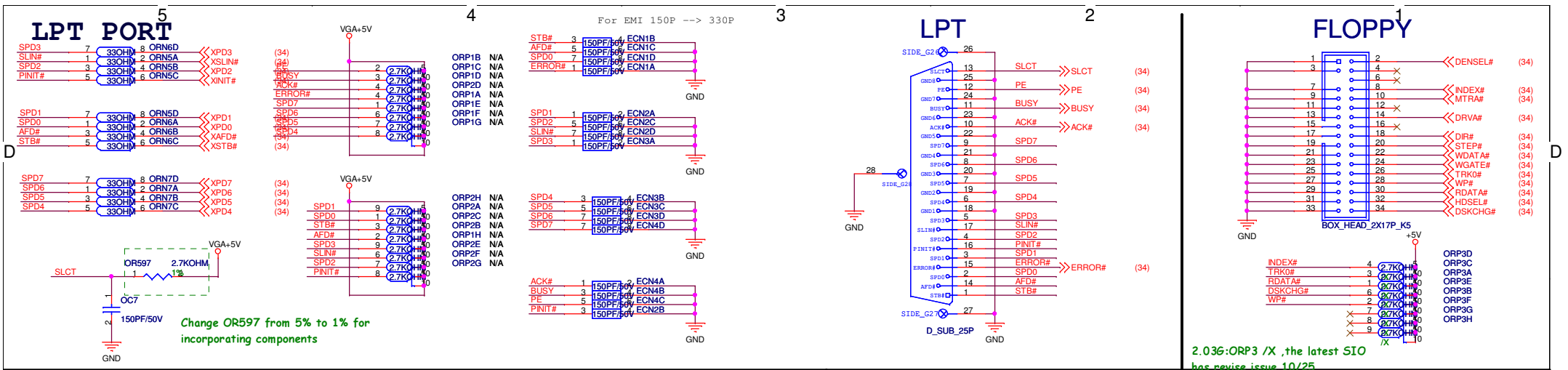


Color: BLACK



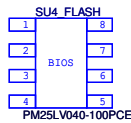
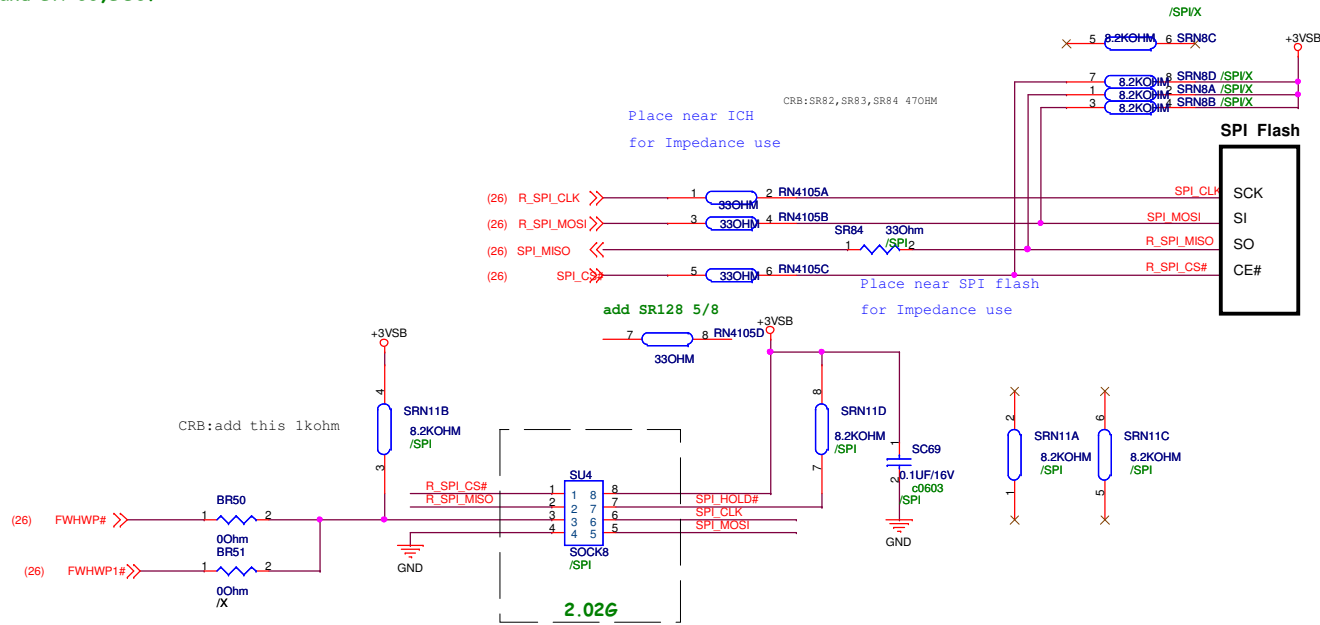


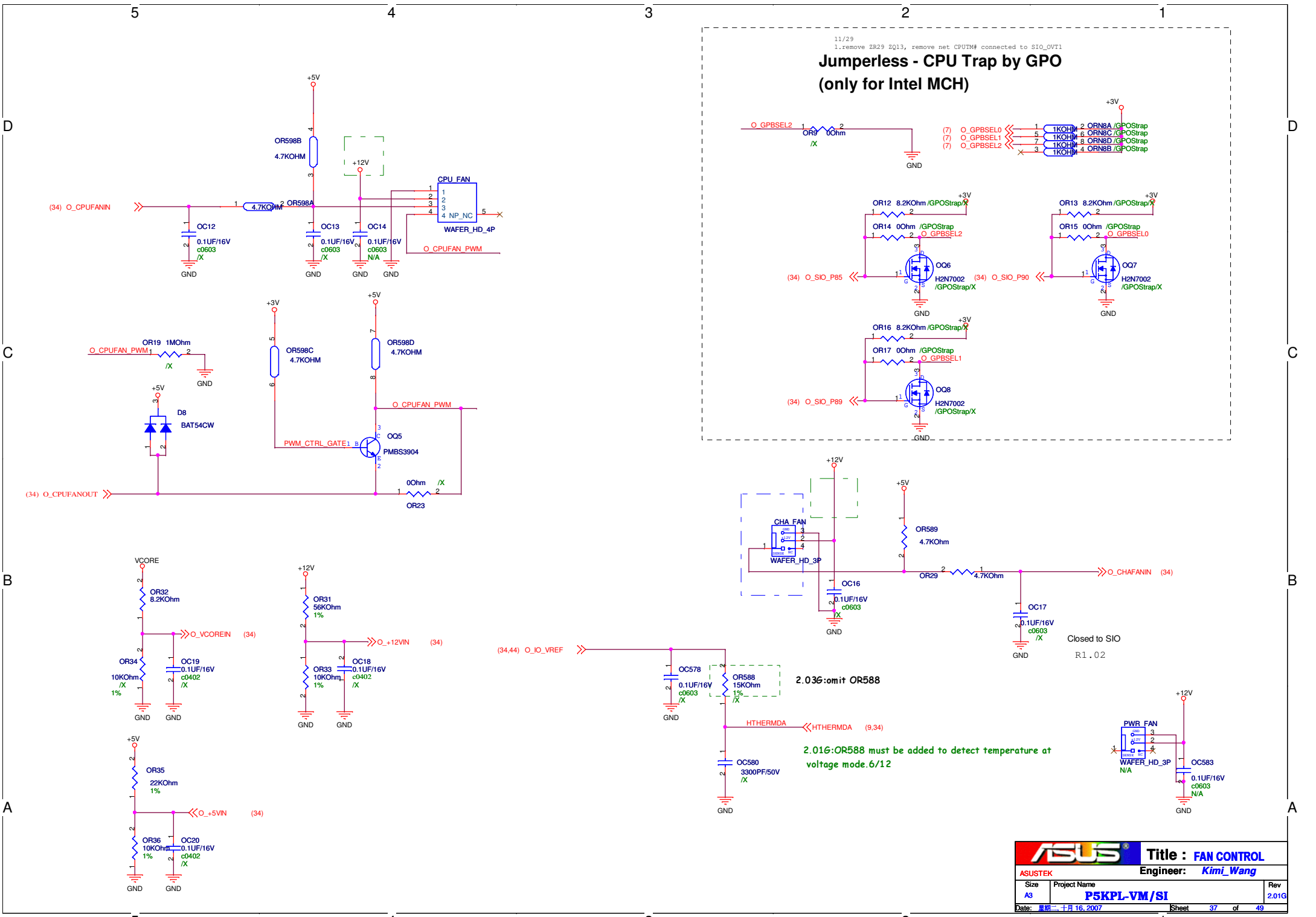
2.03G:del SST circuit



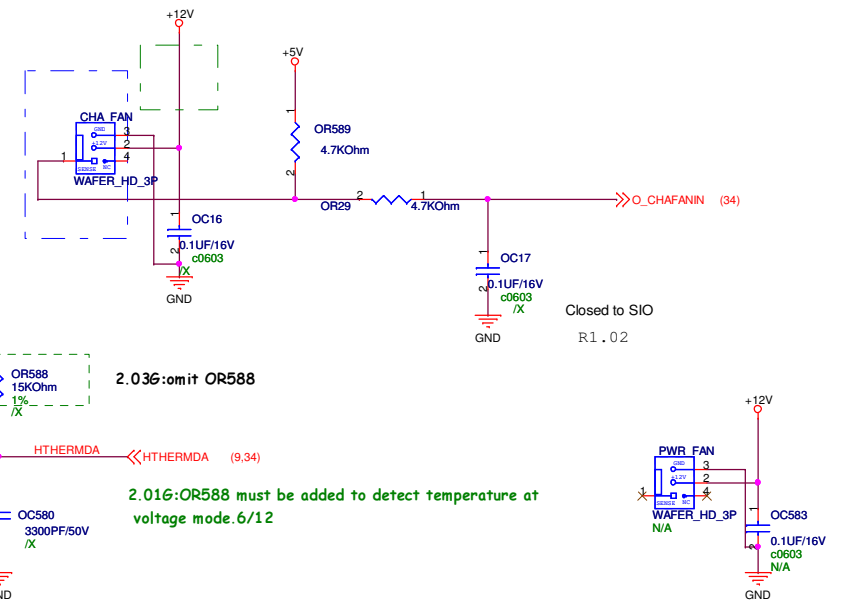
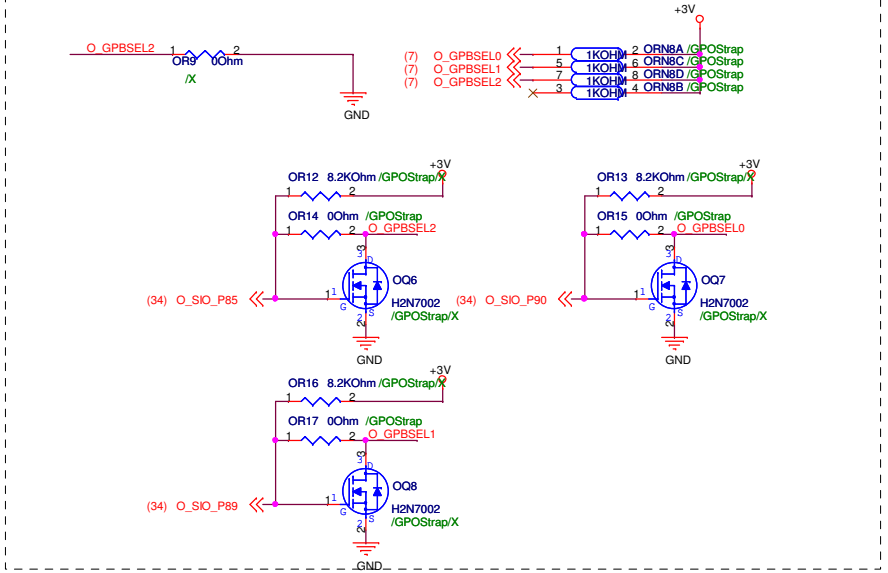
SPI Flash

2.03G: Del SPI_J1 and TPM
and SR133, SD3.

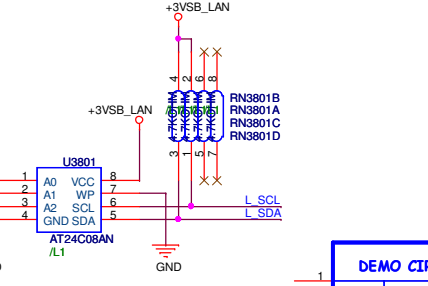
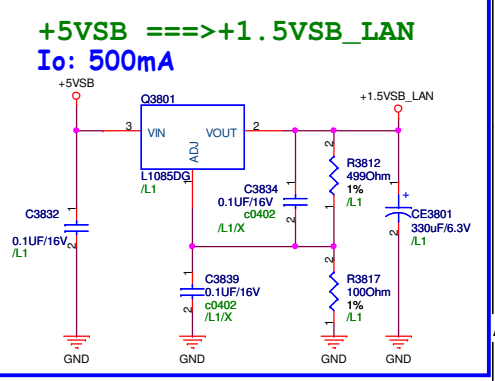
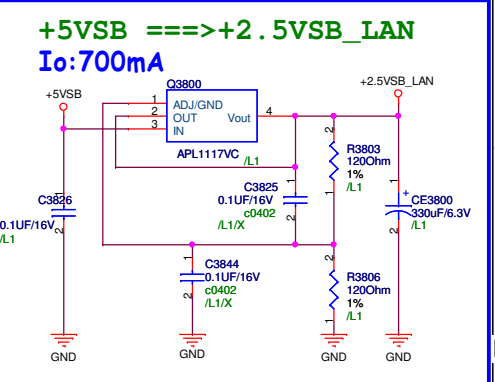
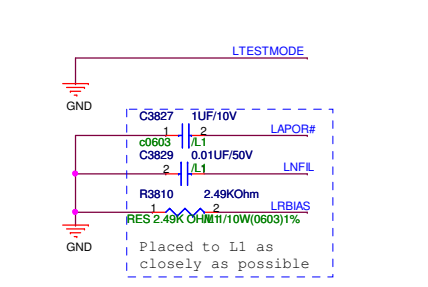
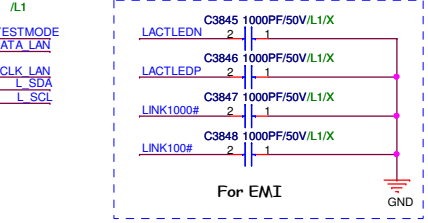
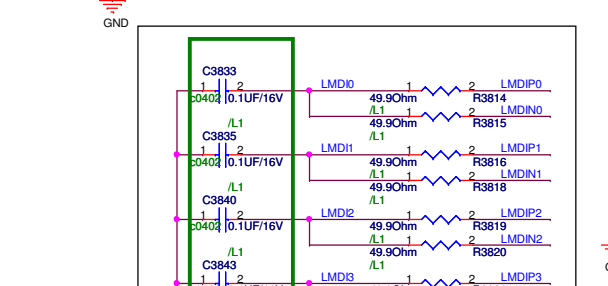
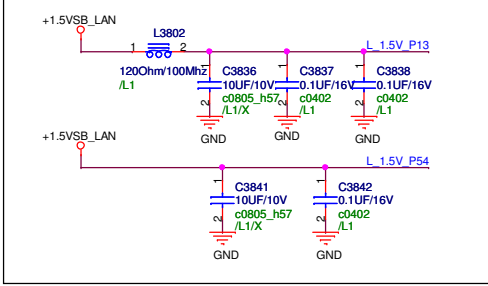
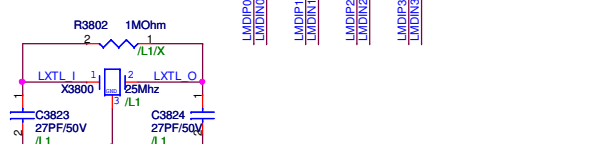
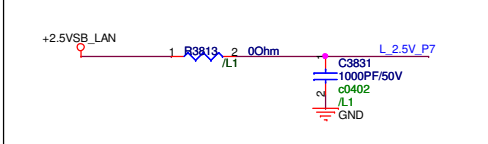
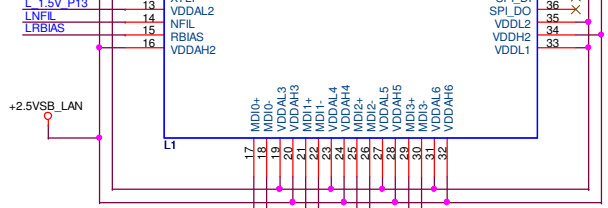
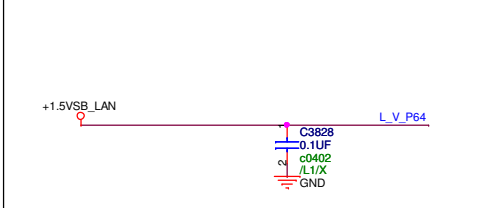
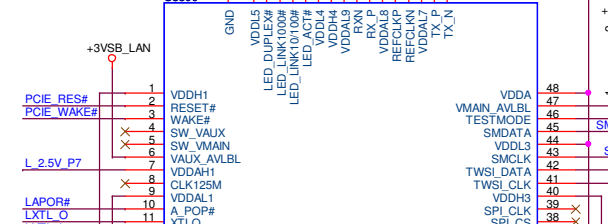
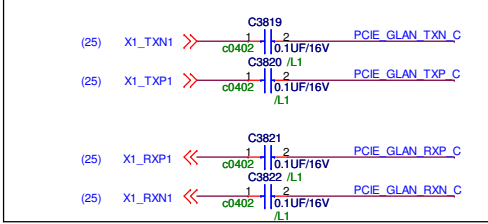
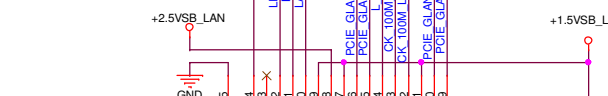
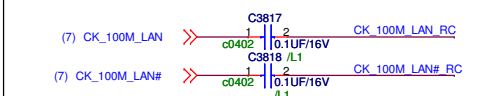
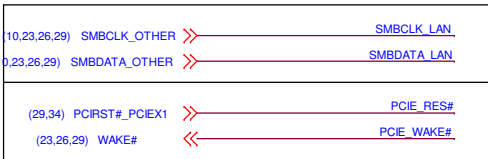
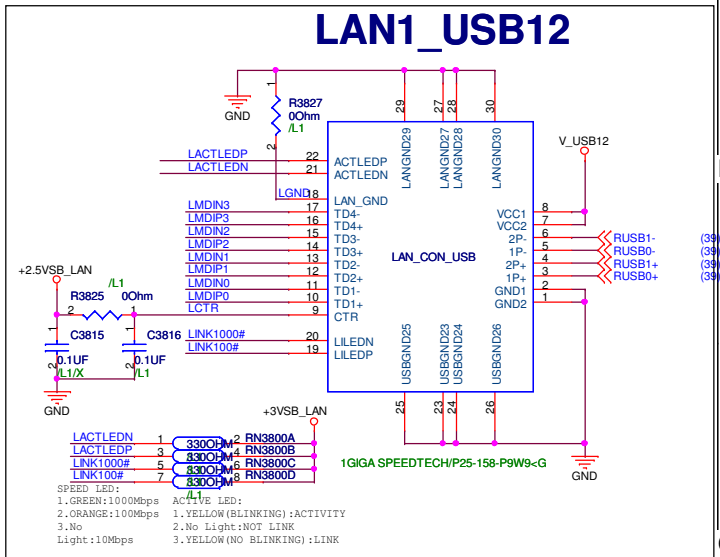
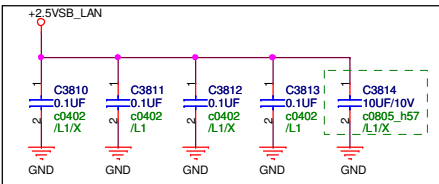
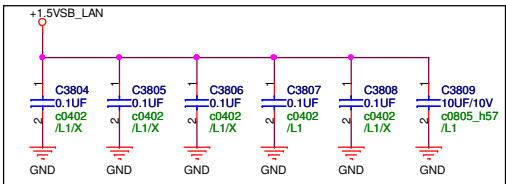
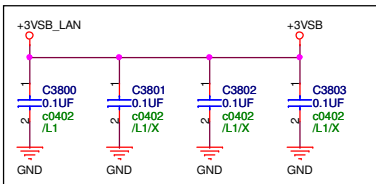


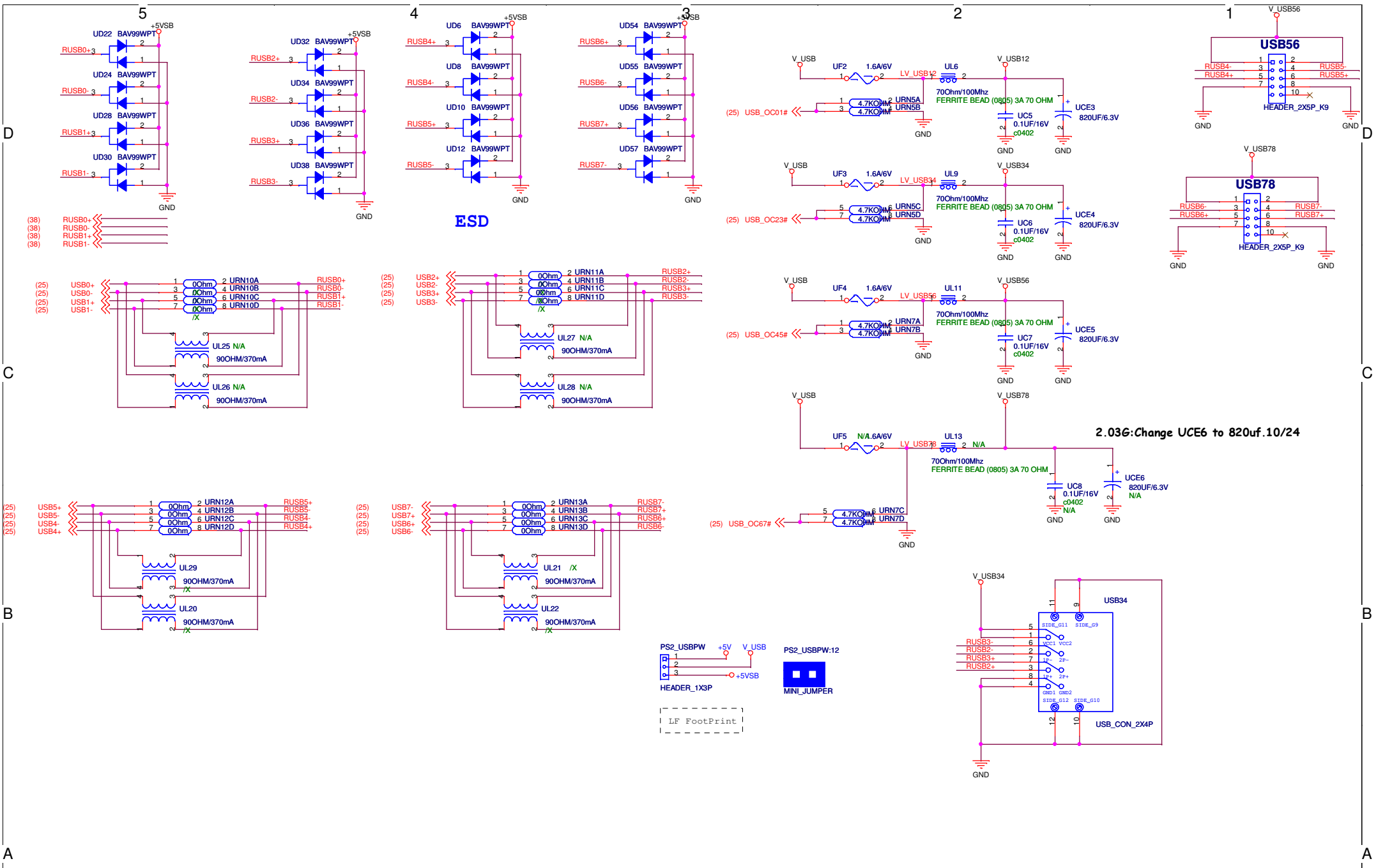


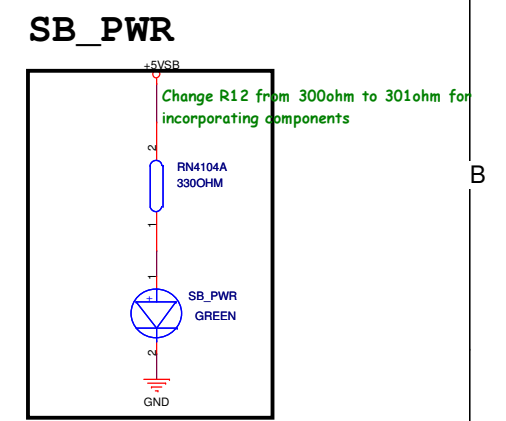
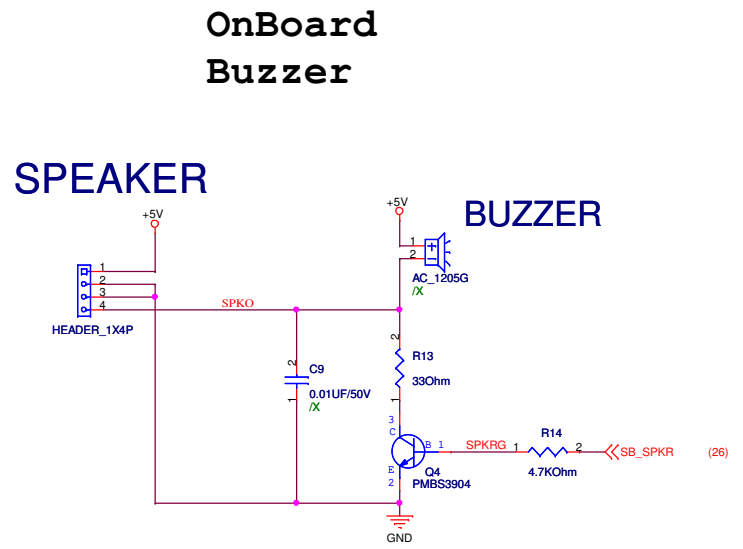
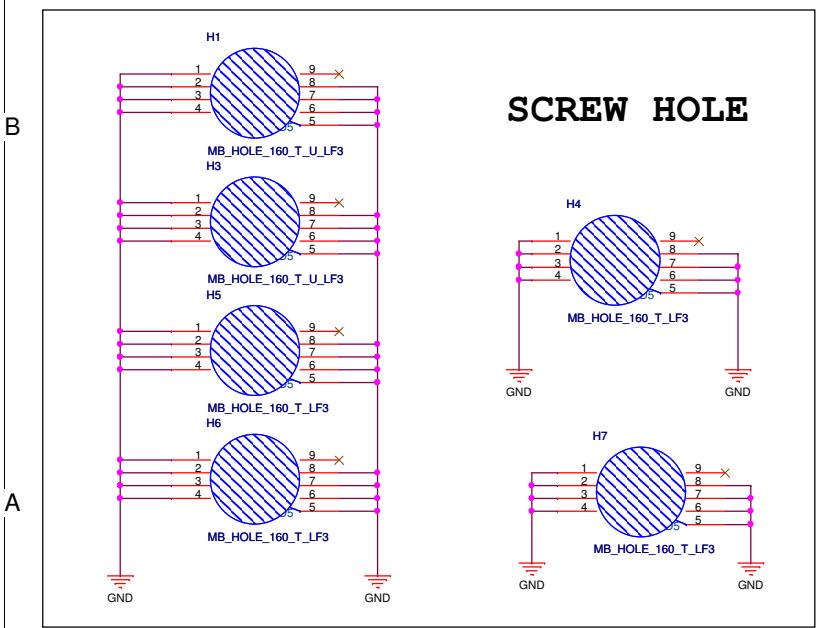
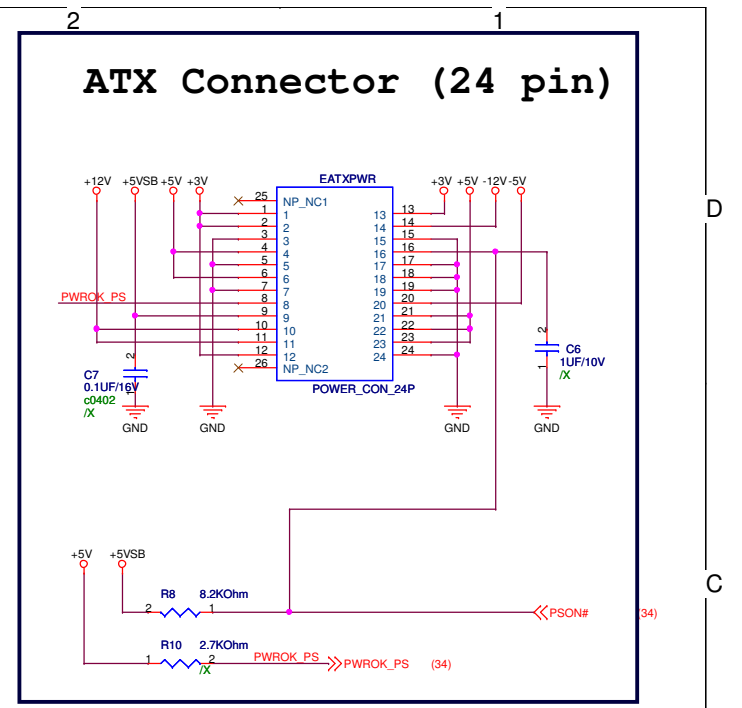
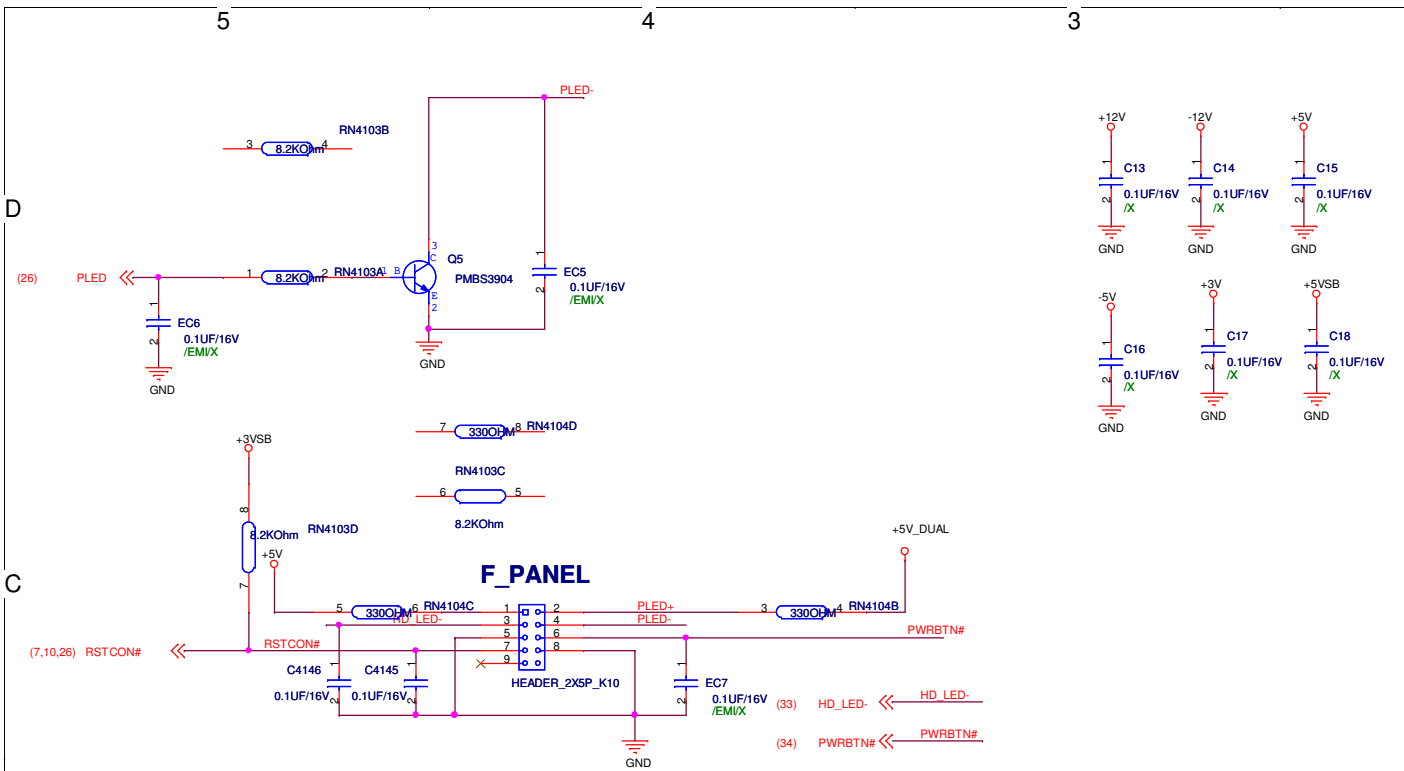
11/29
 1.remove ZR29 ZQ13, remove net CPUIM# connected to SIO_OVT1
Jumperless - CPU Trap by GPO
 (only for Intel MCH)

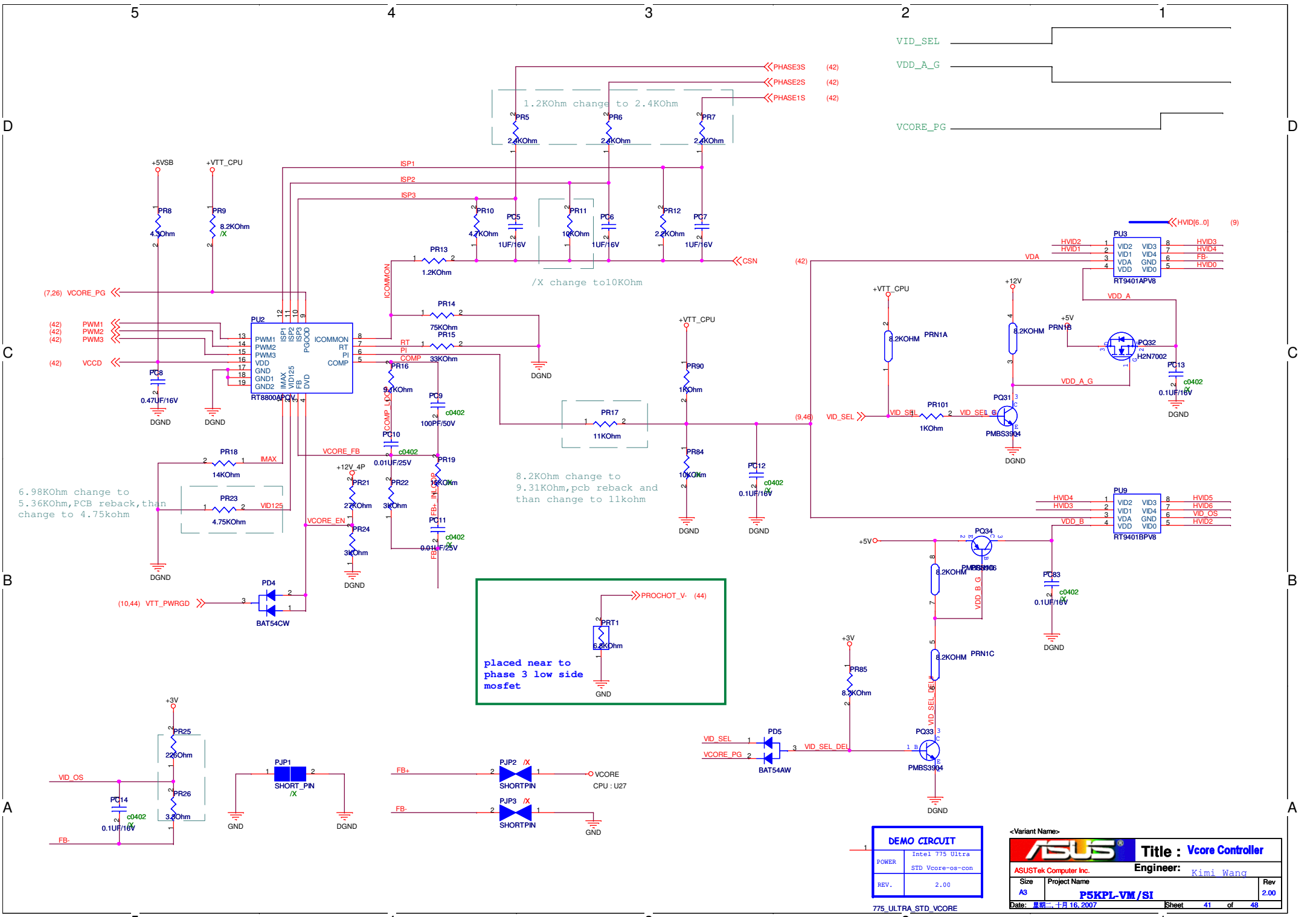


ASUS		Title : FAN CONTROL	
ASUSTEK		Engineer: Kimi_Wang	
Size A3	Project Name PSKPL-VM/SI	Rev 2.01G	
Date: 星期二, 十月 16, 2007	Sheet	37	of 49









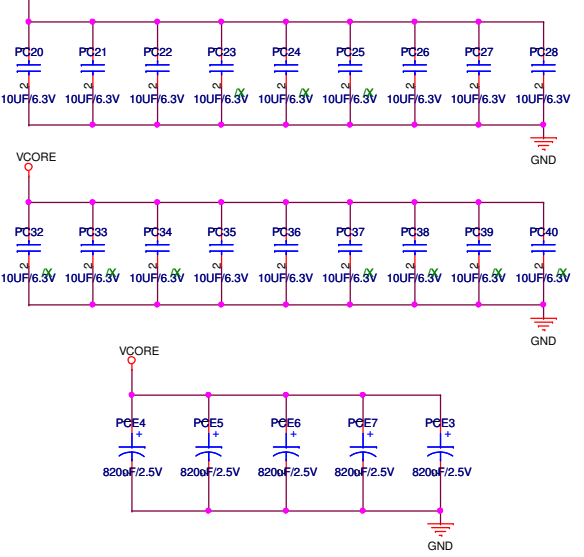
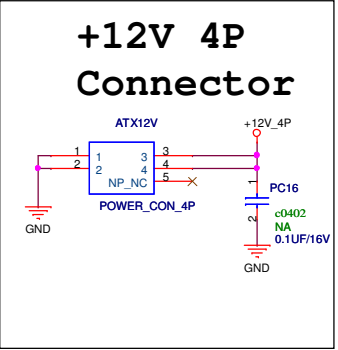
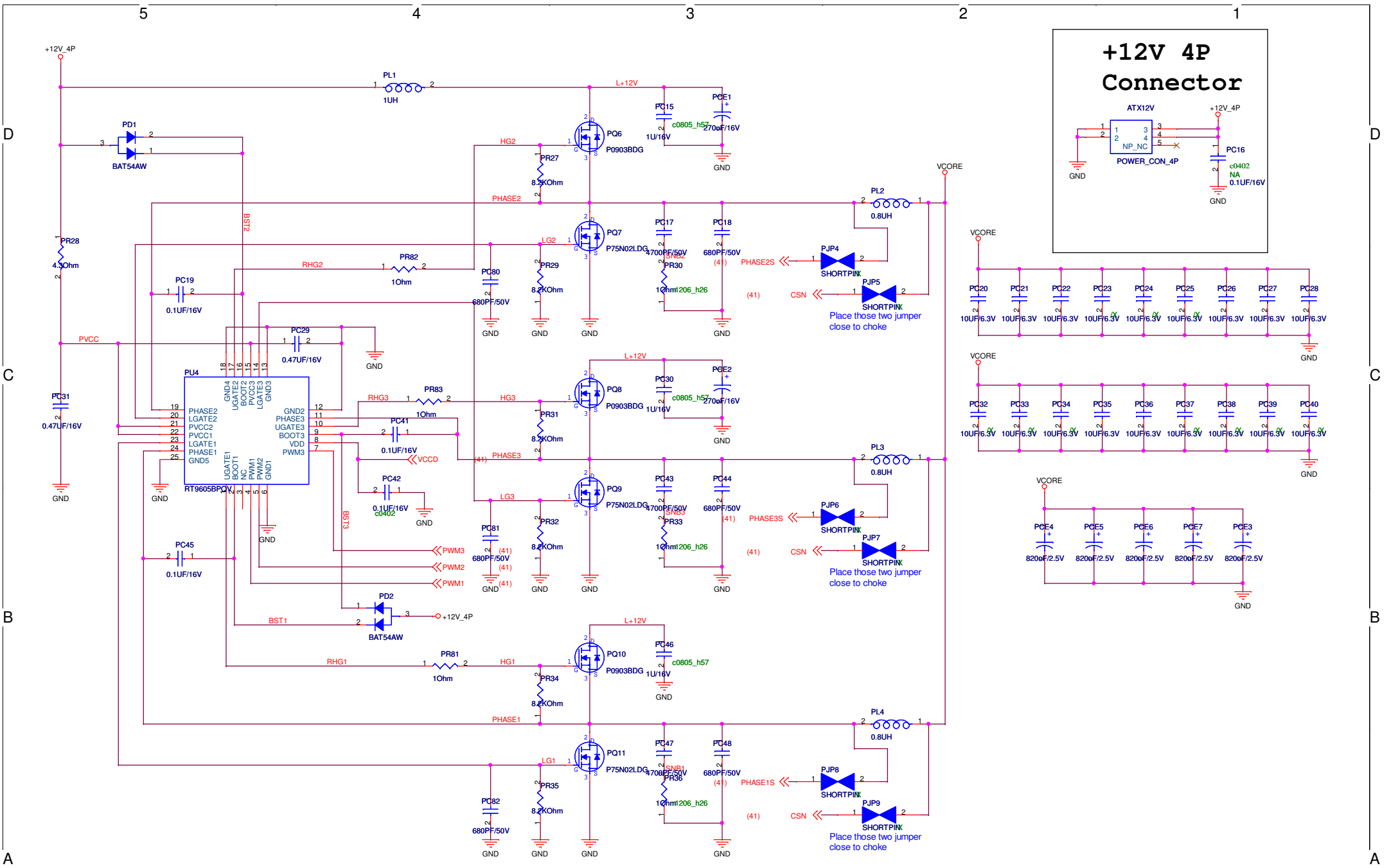
6.98KOhm change to 5.36KOhm, PCB reback, then change to 4.75kohm

8.2KOhm change to 9.31KOhm, pcb reback and than change to 11kohm

placed near to phase 3 low side mosfet

DEMO CIRCUIT	
POWER	Intel 775 Ultra
REV.	STD Vcore-os-con
	2.00

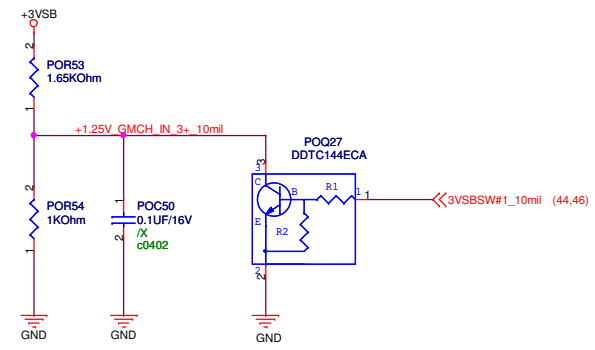
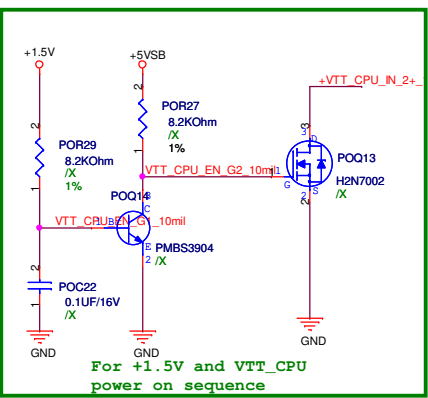
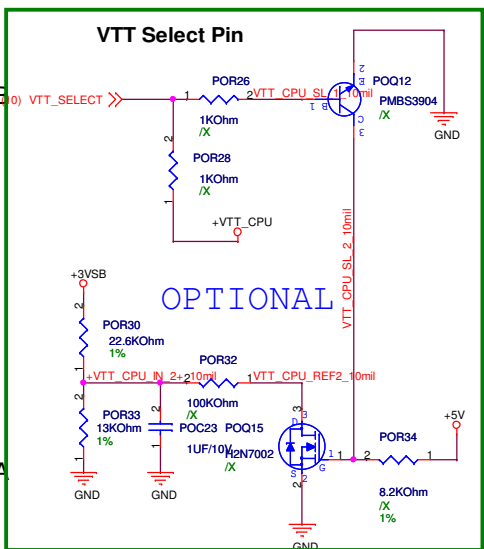
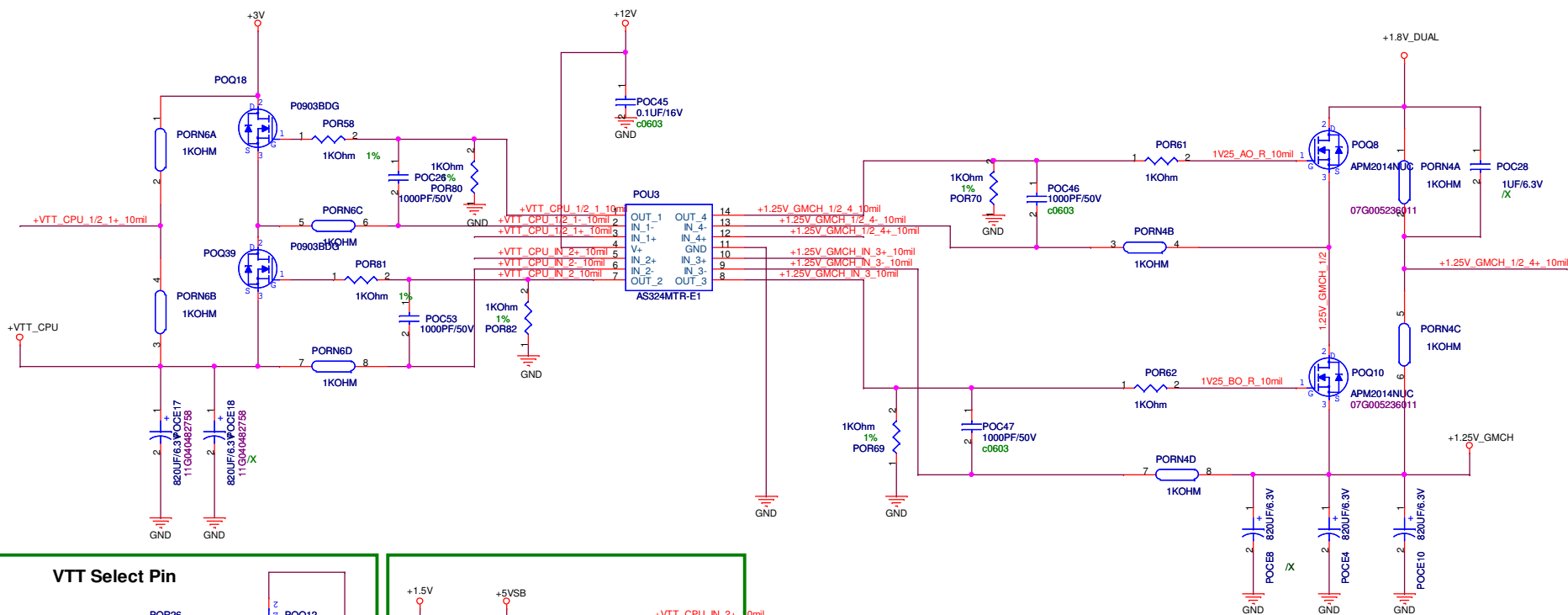
<Variant Name>		ASUS		Title : Vcore Controller	
ASUSTek Computer Inc.		Engineer:		Kimi Wang	
Size	Project Name			Rev	2.00
A3	P5KPL-VM/SI				
Date:	星期二, 十月 16, 2007	Sheet	41	of	48



+3V--->+VTT_CPU

+1.25V_GMCH

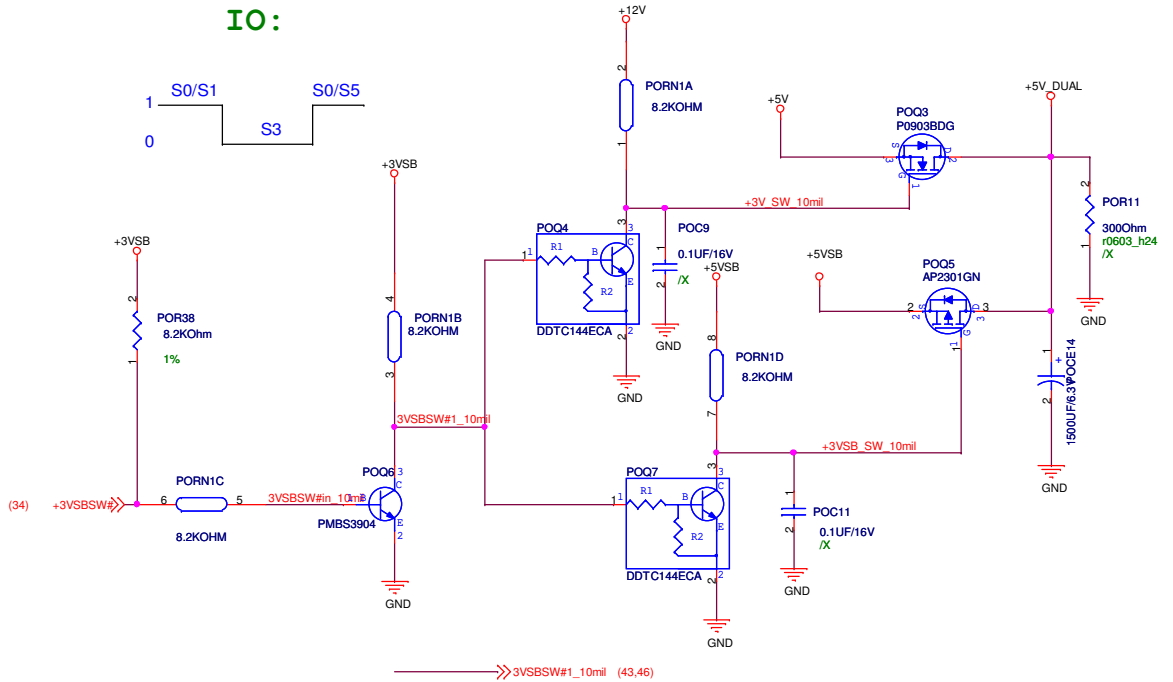
Io:5.79A



ASUS		Title : +1.8V_DUAL,VTT_DDR	
ASUSTEK	Engineer: Kimi_Wang		
Size A3	Project Name P5KPL-VM/SI	Rev 1.00G	
Date: 2007.10.16	Sheet	43	of 48

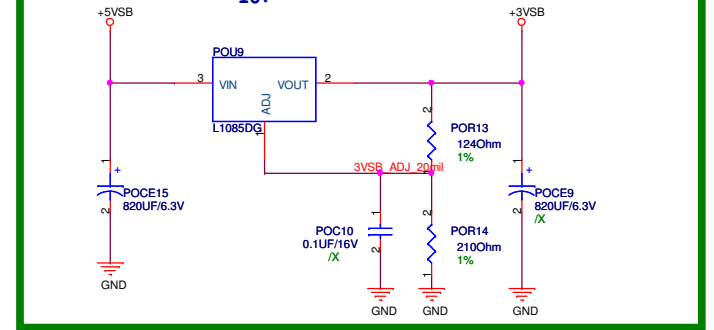
+5V&+5VSB====>+5V_DUAL

IO:

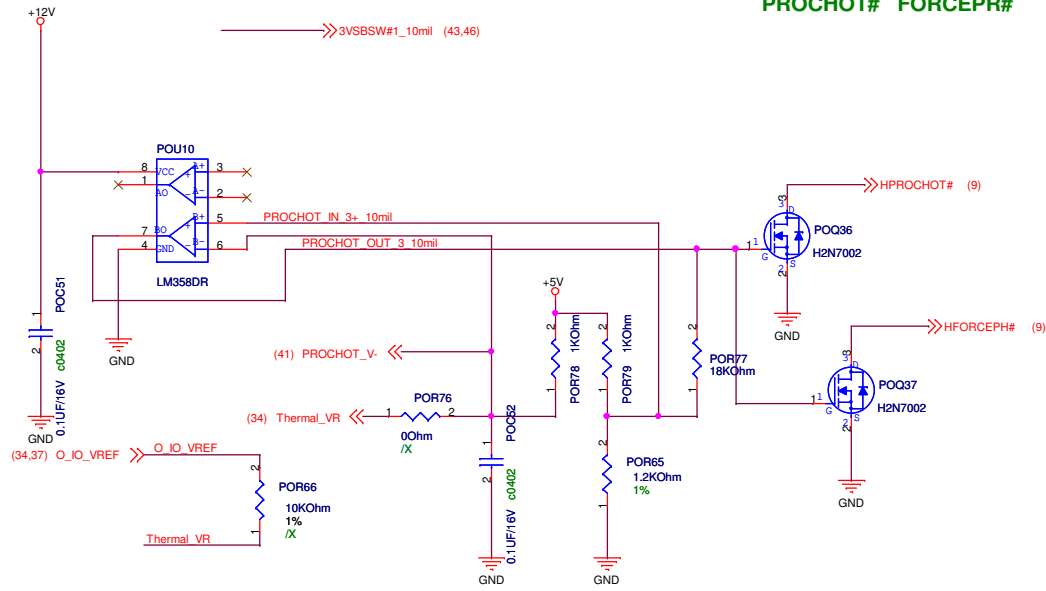


+5VSB====>+3VSB

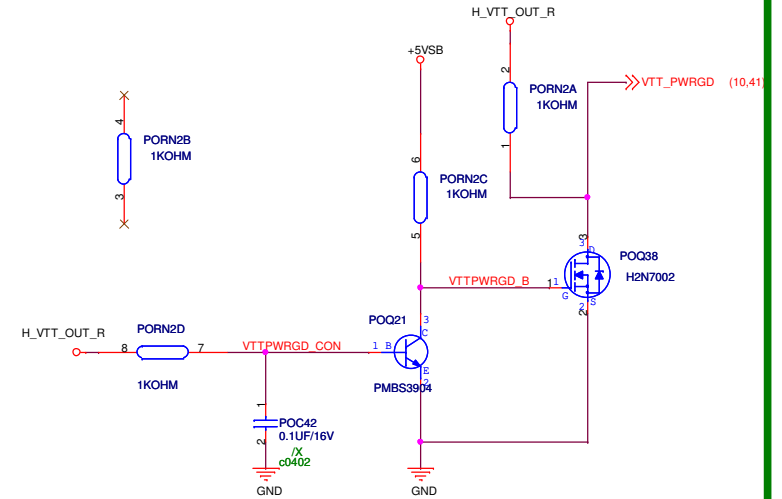
IO:

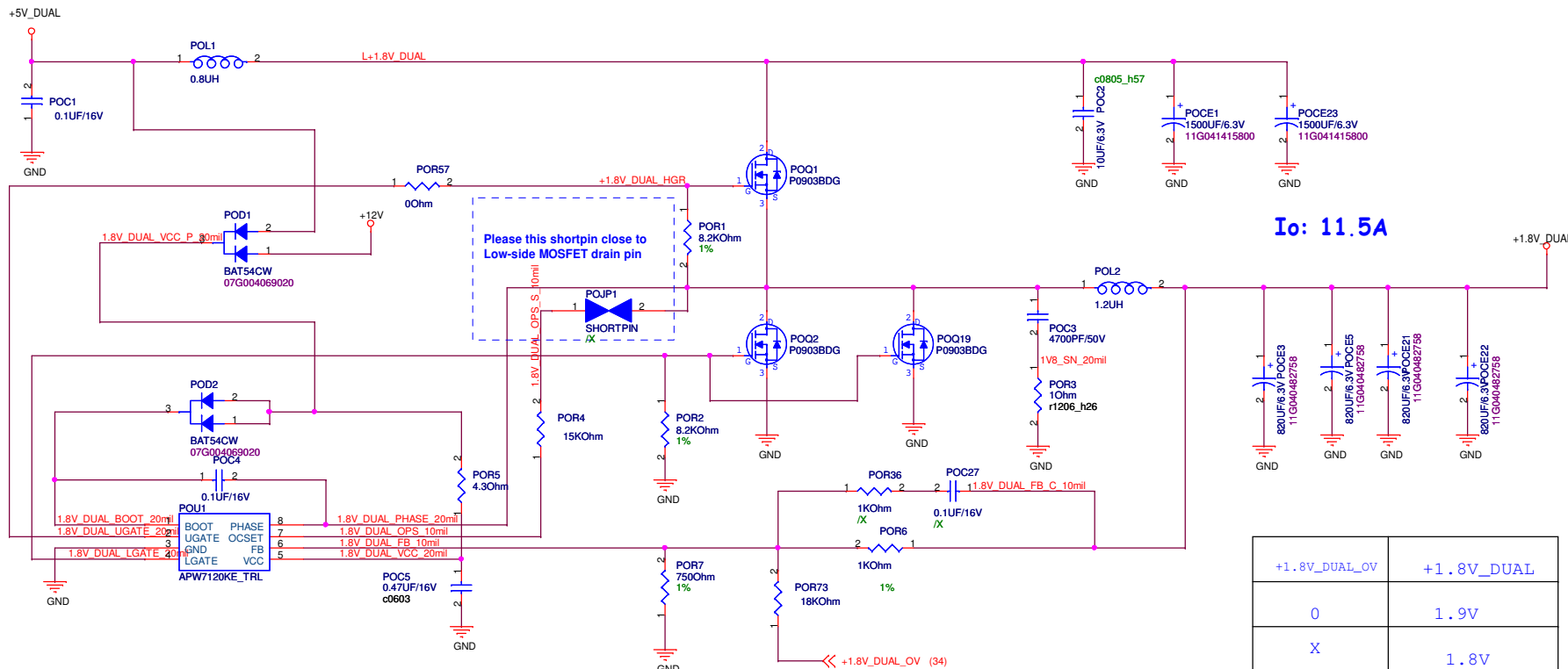


PROCHOT# FORCEPR#



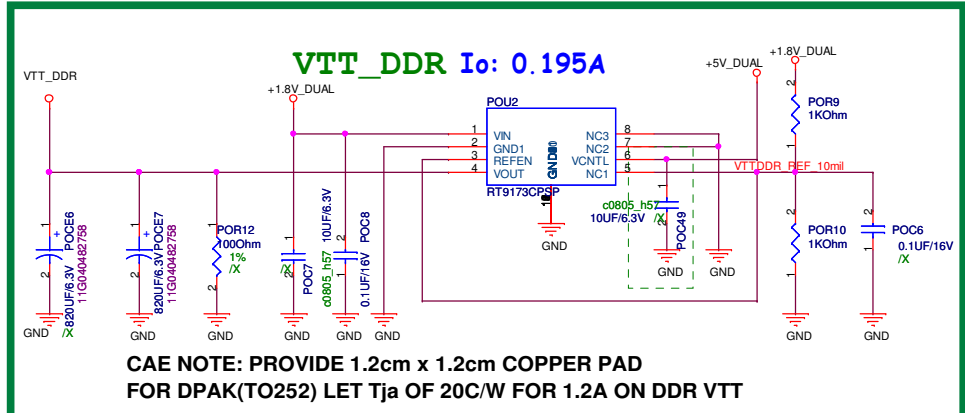
3/3 add this for Intel's CPU power sequence





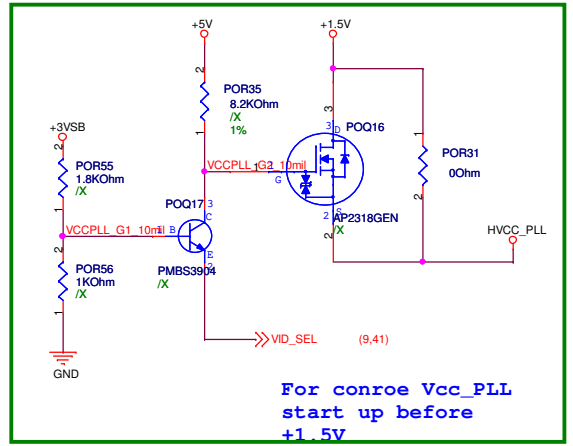
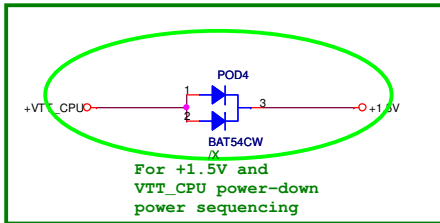
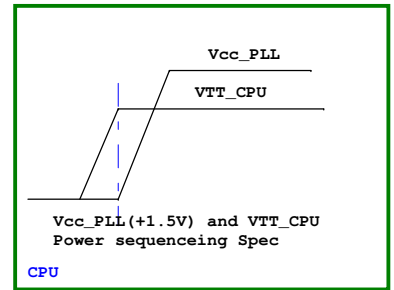
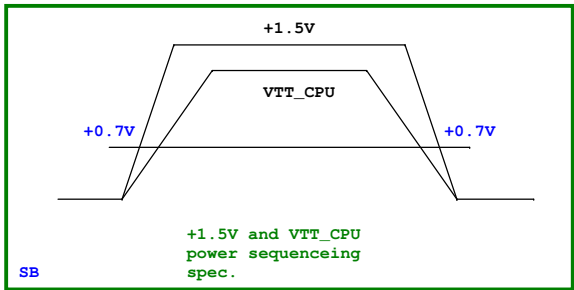
Io: 11.5A

+1.8V_DUAL_OV	+1.8V_DUAL
0	1.9V
X	1.8V



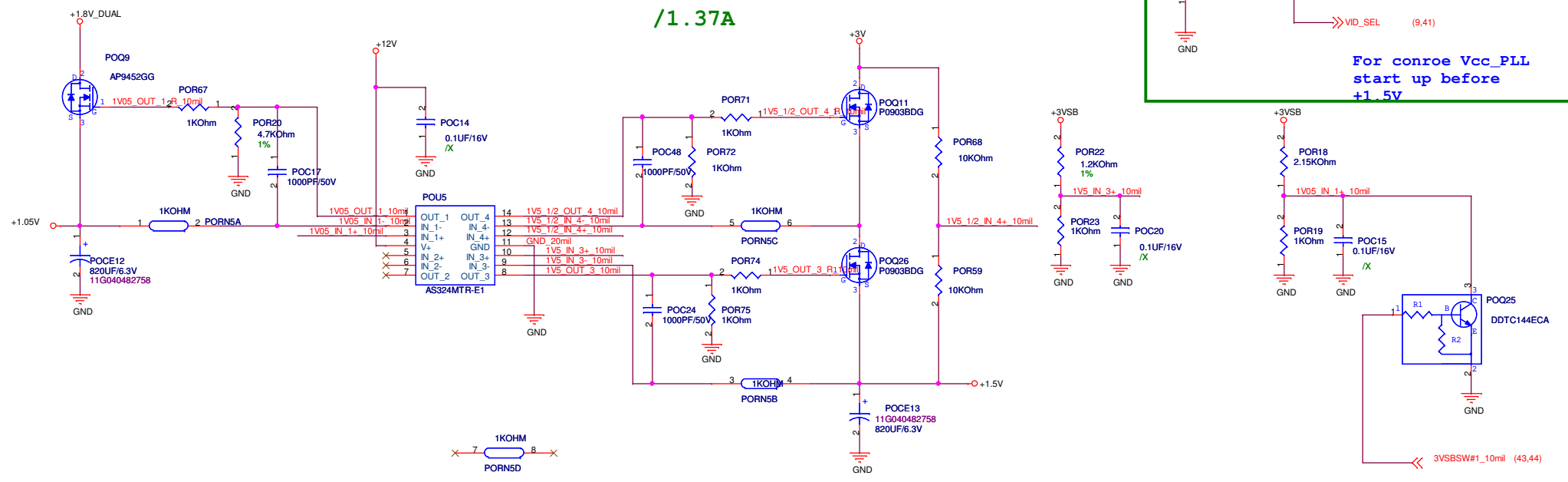
CAE NOTE: PROVIDE 1.2cm x 1.2cm COPPER PAD FOR DPAK(TO252) LET Tja OF 20C/W FOR 1.2A ON DDR VTT

5 4 3 2 1



+1.8V_DUAL ==> +1.05V
Io: 0.51A

+3V ==> +1.5V
/1.37A



ASUS		Title : VTT_CPU	
ASUSTEK		Engineer: <i>Kimi_Wang</i>	
Size A3	Project Name P5KPL-VM/SI	Rev 2.03G	
Date: 星期二, 十月 16, 2007		Sheet 46 of 48	

5

4

3

2

1

D

D

C

C

B

B

A

A

		Title LAN 2.5V&LAN 1.5V	
ASUSTEK		Engineer: <i>Kimi_Wang</i>	
Size A3	Project Name PSKPL-VM/SI		Rev 2.03G
Date: 星期二, 十月 16, 2007	Sheet 47 of 48		

