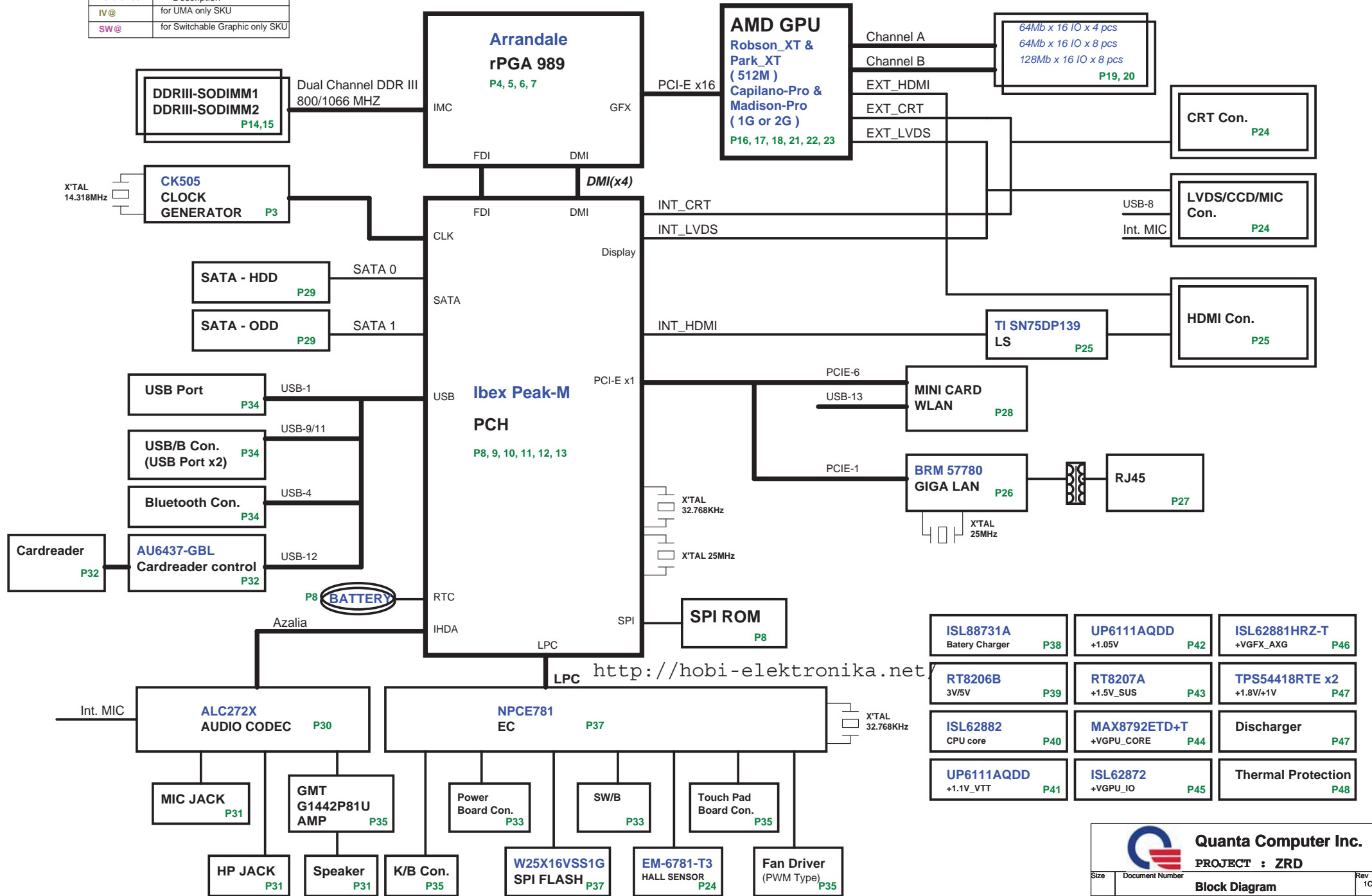


# HM55\_CP (ZRD) SYSTEM BLOCK DIAGRAM

BOM Option Table

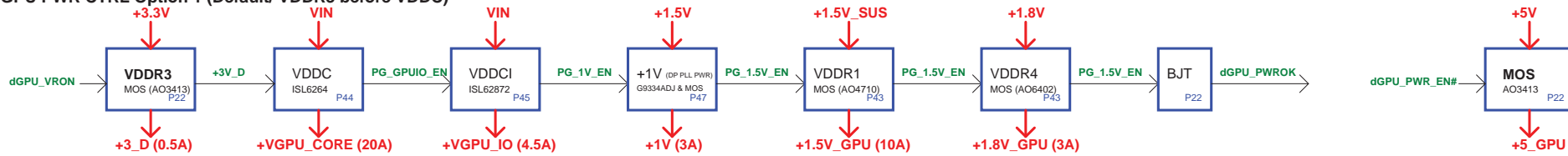
Reference	Description
IV@	for UMA only SKU
SW@	for Switchable Graphic only SKU



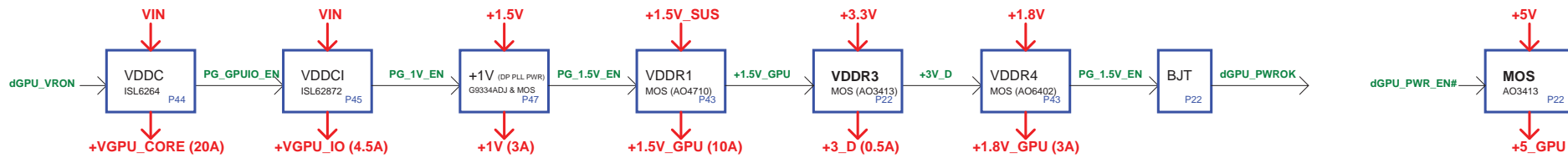
<http://hobi-elektronika.net/>

<b>ISL88731A</b> Battery Charger P38	<b>UP6111AQDD</b> +1.05V P42	<b>ISL62881HRZ-T</b> +VGF_X_AG P46
<b>RT8206B</b> 3V/5V P39	<b>RT8207A</b> +1.5V_SUS P43	<b>TPS54418RTE x2</b> +1.8V/+1V P47
<b>ISL62882</b> CPU core P40	<b>MAX8792ETD+T</b> +VGPU_CORE P44	Discharger P47
<b>UP6111AQDD</b> +1.1V_VTT P41	<b>ISL62872</b> +VGPU_IO P45	Thermal Protection P48

### GPU PWR CTRL Option 1 (Default/ VDDR3 before VDDC)



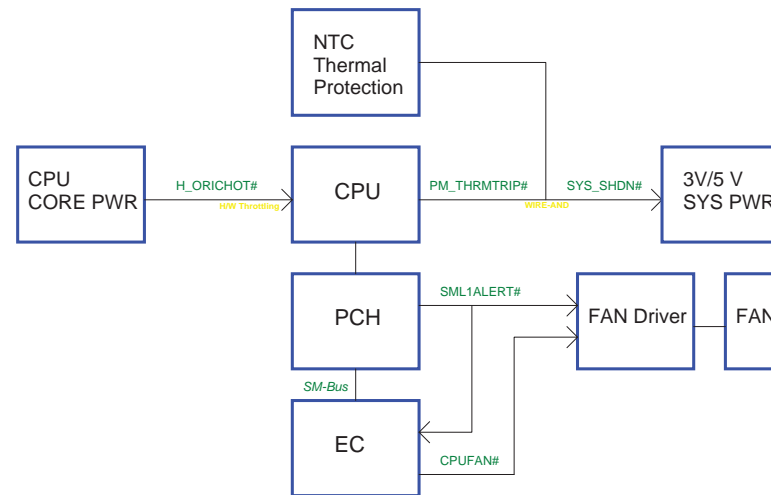
### GPU PWR CTRL Option 2 (VDDR3 after VDDC)



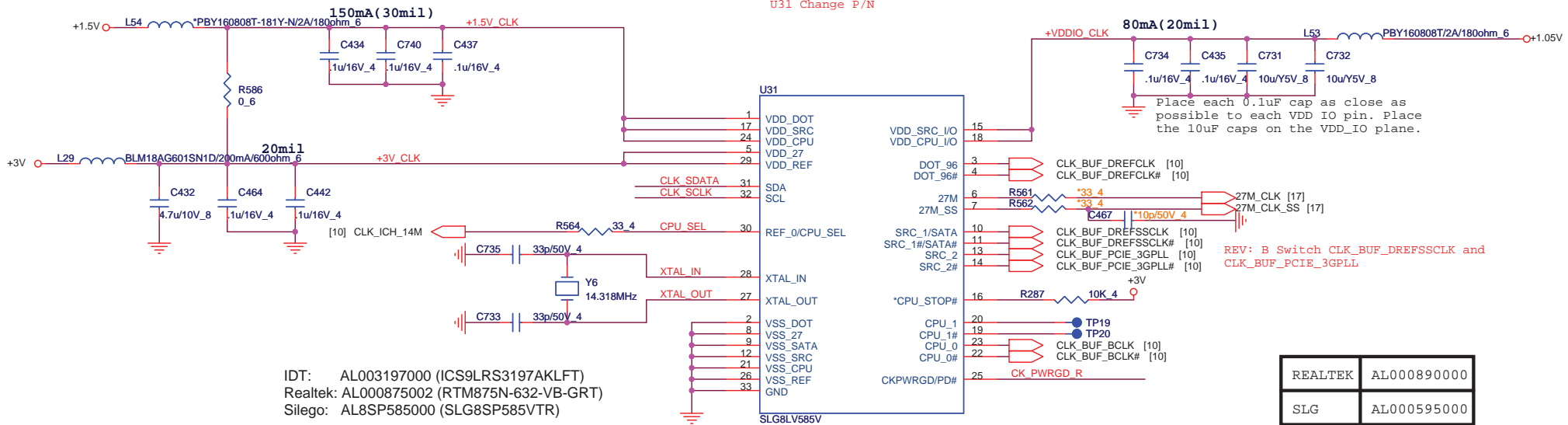
### Power States

POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	+10V~+19V	MAIN POWER	ALWAYS	ALWAYS
+VCCRTC	+3V~+3.3V	RTC POWER	ALWAYS	ALWAYS
+3VPCU	+3.3V	EC POWER	ALWAYS	ALWAYS
+5VPCU	+5V	CHARGE POWER	ALWAYS	ALWAYS
+15V	+15V	CHARGE PUMP POWER	ALWAYS	ALWAYS
+3V_S5	+3.3V	LAN/BT/CIR POWER	S5_ON	S0-S5
+5V_S5	+5V	USB POWER	S5_ON	S0-S5
+5V	+5V	HDD/ODD/Codec/TP/CRT/HDMI POWER	MAINON	S0
+3V	+3.3V	PCH/GPU/Peripheral component POWER	MAINON	S0
+1.5VSUS	+1.5V	CPU/SODIMM CORE POWER	SUSON	S0-S3
+0.75V_DDR_VTT	+0.75V	SODIMM Termination POWER	MAINON	S0
+VGFX_AXG	variation	Internal GPU POWER	GFX_ON	S0
+1.8V	+1.8V	CPU/PCH/Braidwood POWER	MAINON	S0
+1.5V	+1.5V	MINI CARD/NEW CARD POWER	MAINON	S0
+1.1V_VTT	+1.05V or +1.1V	CPU VTT POWER	MAINON	S0
+1.05V	+1.05V	PCH CORE POWER	MAINON	S0
+VCC_CORE	variation	CPU CORE POWER	VRON	S0
LCDVCC	+3.3V	LCD POWER	LVDS_VDDEN	S0
+5V_GPU	+5V	SWITCHABLE PWM IC POWER	dGPU_PWR_EN#	Discrete enable
+GPU_CORE	+0.9V~+1.1V	GPU CORE POWER	+3V_D	Discrete enable
+GPU_IO	+0.9V~+1.1V	GPU I/O POWER	PG_GPUIO_EN	Discrete enable
+1.5V_GPU	+1.5V	VRAM CORE POWER	PG_1.5V_EN	Discrete enable
+1.8V_GPU	+1.8V	GPU_CRE/LVDS/PLL POWER	+1.5V_GPU	Discrete enable
+1V	+1V	DP/PEG POWER	PG_1V_EN	Discrete enable

### Thermal Follow Chart



6/21 add R586 for 3V CLK gen  
Un-stuff L54  
U31 Change P/N

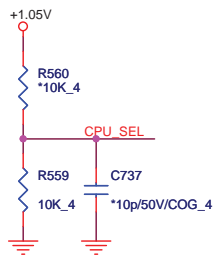


IDT: AL003197000 (ICS9LRS3197AKLFT)  
Realtek: AL000875002 (RTM875N-632-VB-GRT)  
Silego: AL8SP585000 (SLG8SP585VTR)

REALTEK	AL000890000
SLG	AL000595000

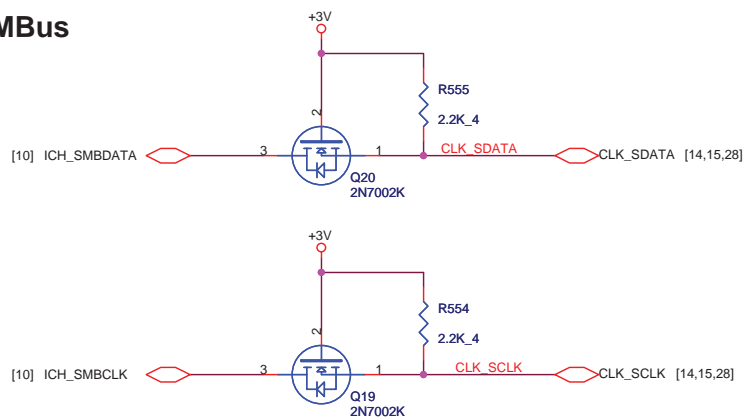
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### CPU\_CLK select

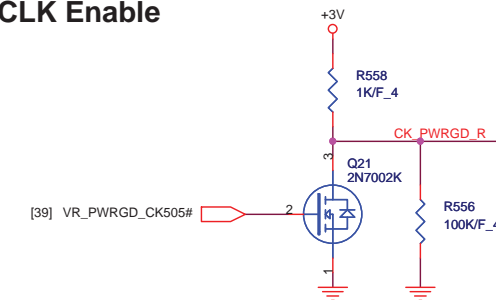


	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz

### SMBus

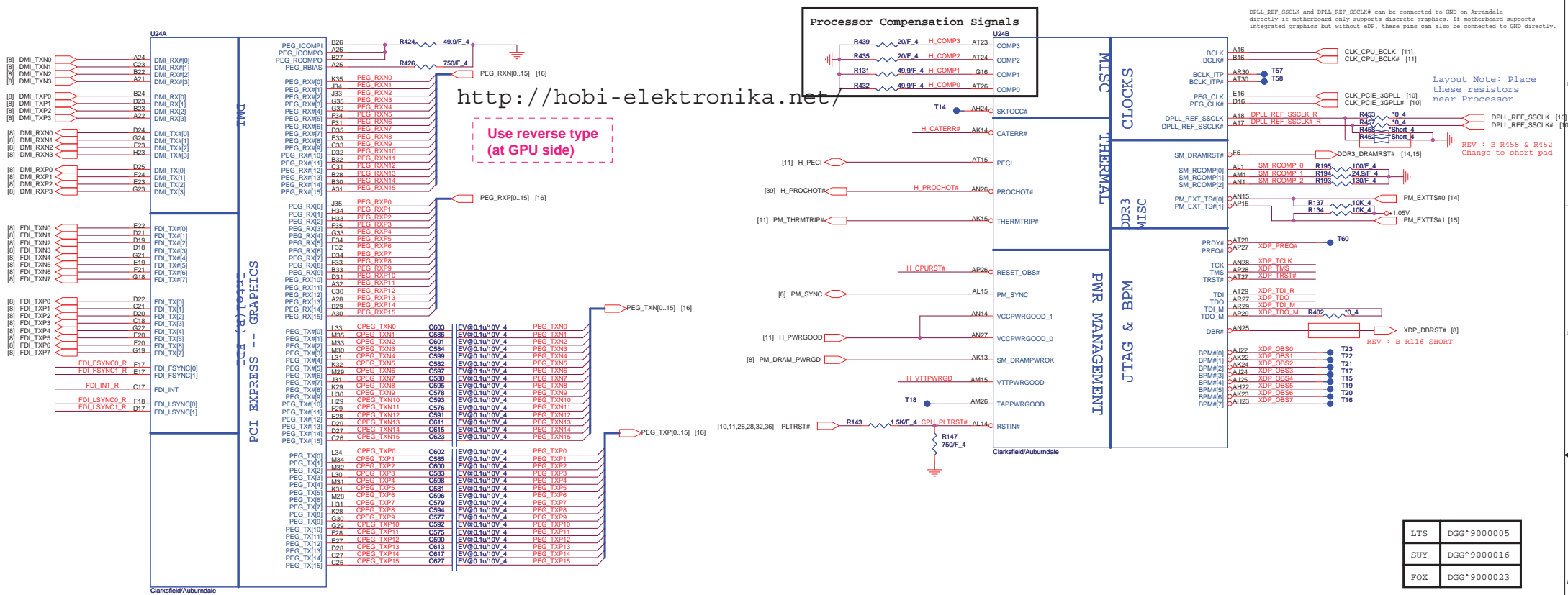


### CLK Enable



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	<b>Clock Generator</b>	1C
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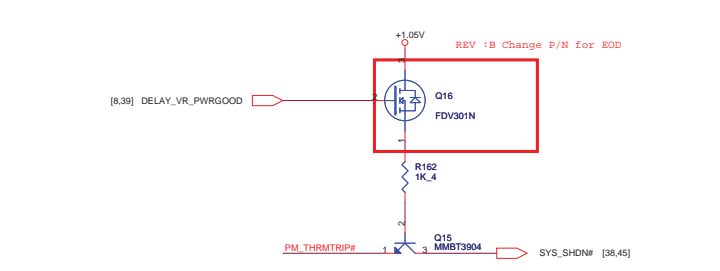


<http://hobi-elektronika.net/>

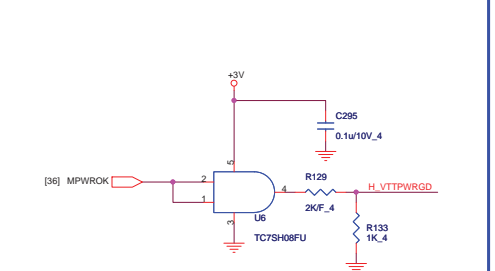
Use reverse type (at GPU side)

ITS	DG9*9000005
SUY	DG9*9000016
POX	DG9*9000023

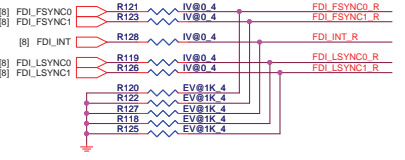
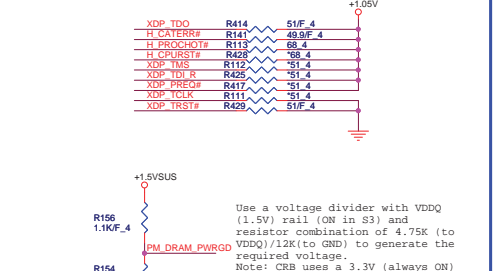
**Thermaltrip protect**



**VTT PWR\_Good**



**Processor pull-up**

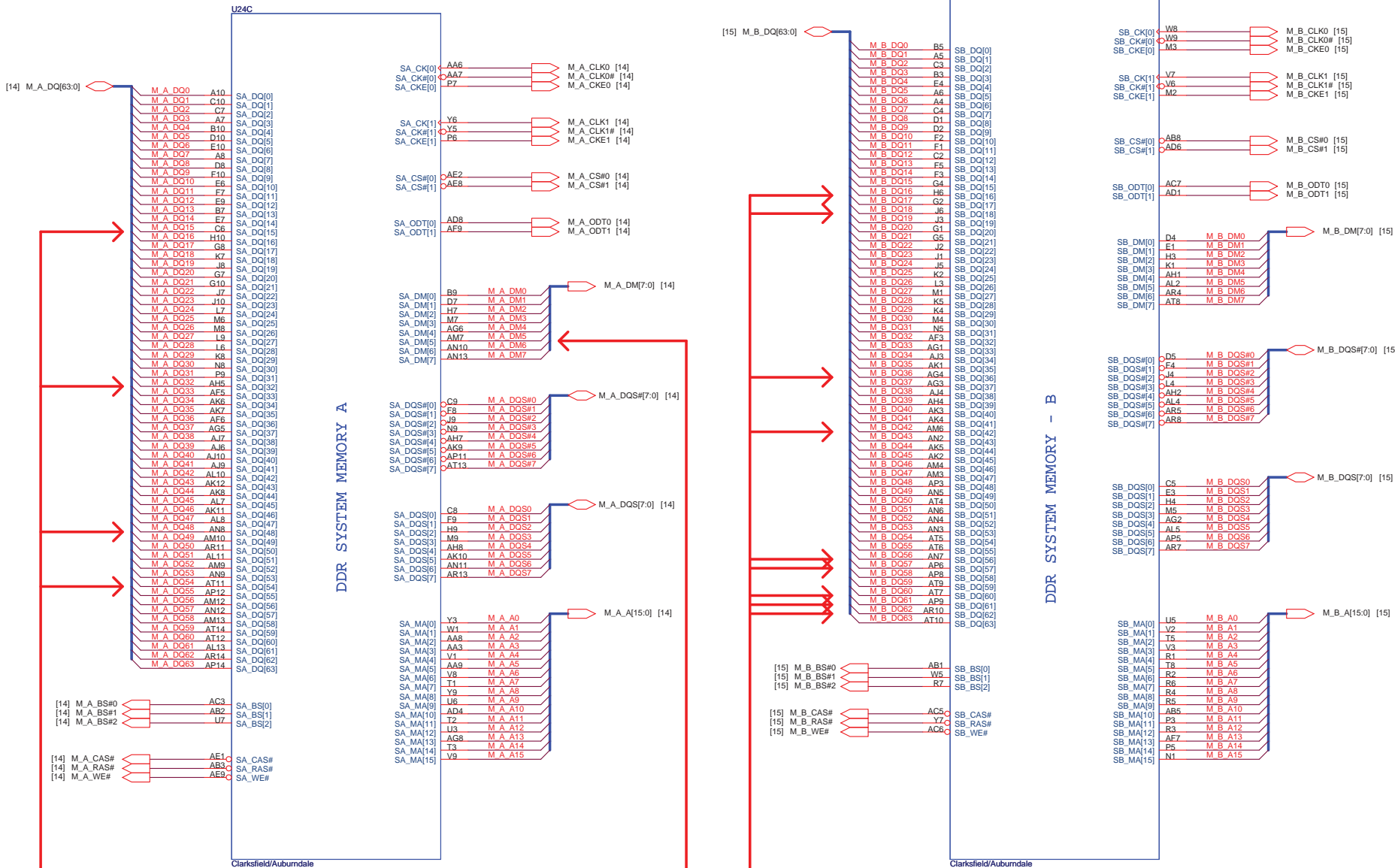


<The GFX\_IMON, FDI\_FSYN0[0], FDI\_FSYN0[1], FDI\_LSYNC0[0], FDI\_LSYNC1[1], and FDI\_INT>Note that if these signals are left as no connect, there are no functional impacts, but a small amount of power (~15 mW) maybe wasted.

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# AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



Channel A DQ[15,32,48,54], DM[5]  
Requires minimum 12mils spacing  
with all other signals, including data signals.

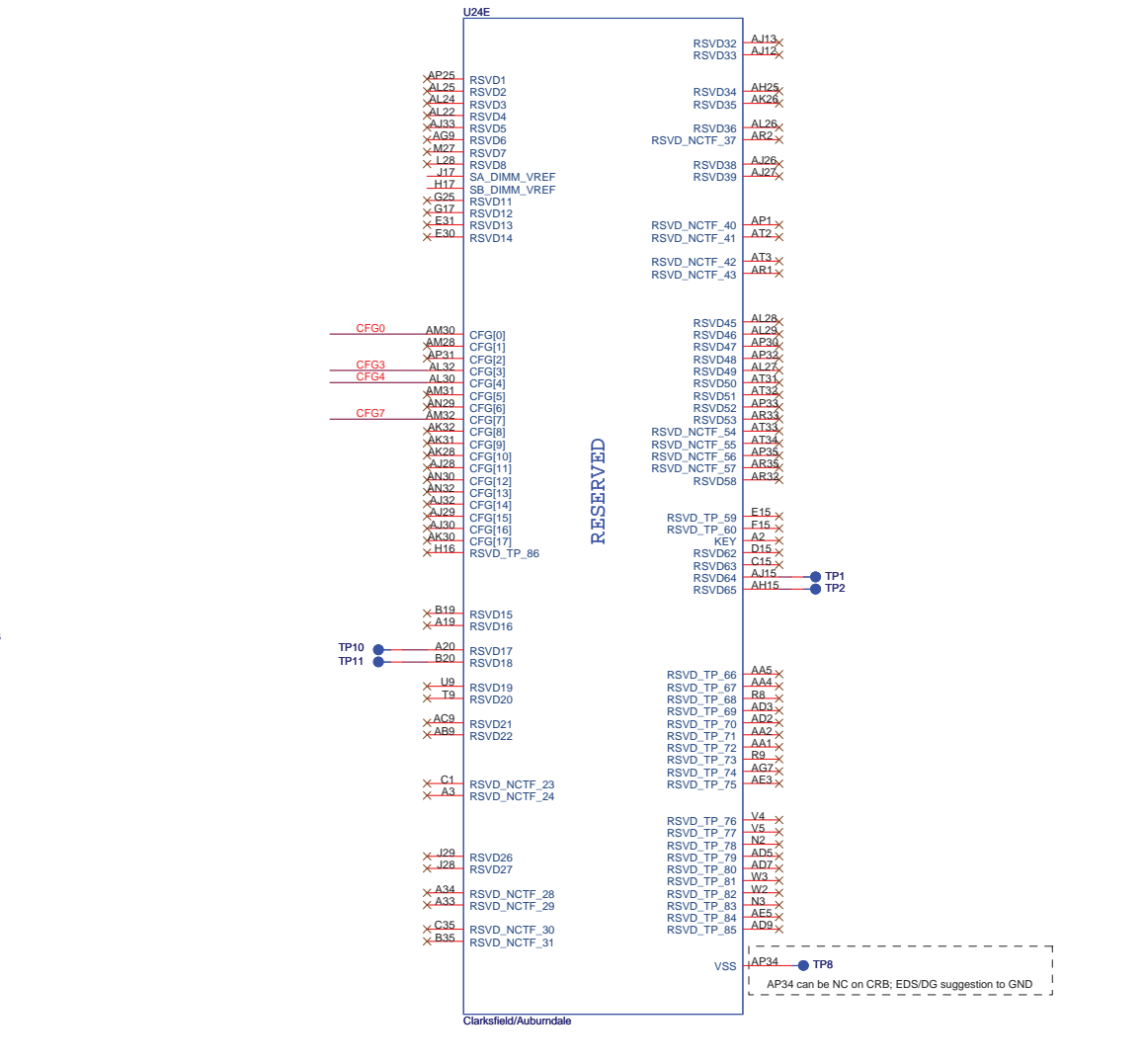
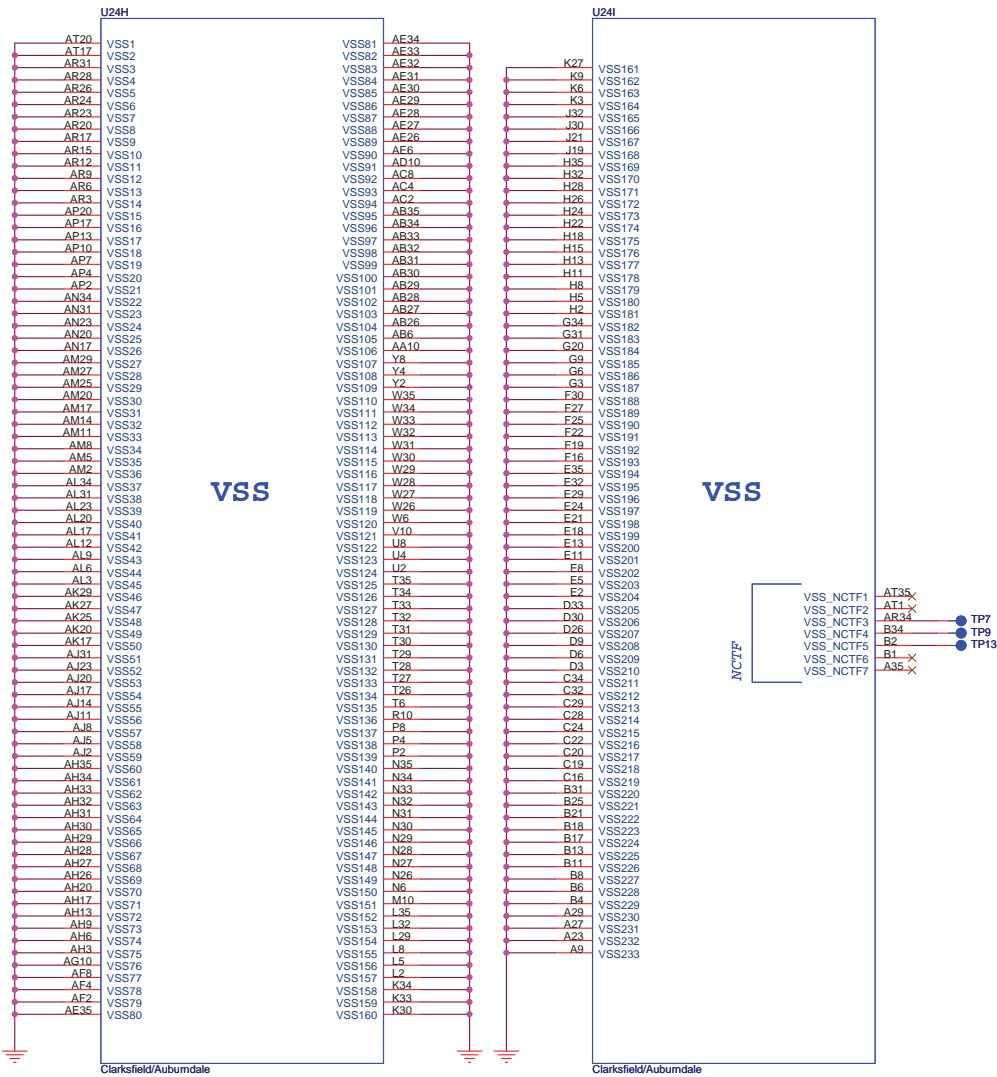
Channel B DQ[16,18,36,42,56,57,60,61,62]  
Requires minimum 12mils spacing  
with all other signals, including data signals.





# AUBURNDALE/CLARKSFIELD PROCESSOR (GND)

# AUBURNDALE/CLARKSFIELD PROCESSOR ( RESERVED, CFG)



## Processor Strapping

	1	0	DEFAULT	
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled	1	
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed	1	
CFG4 (Embedded Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port	1	
The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.				

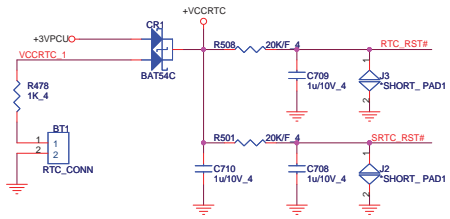
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**PROJECT : ZRD**

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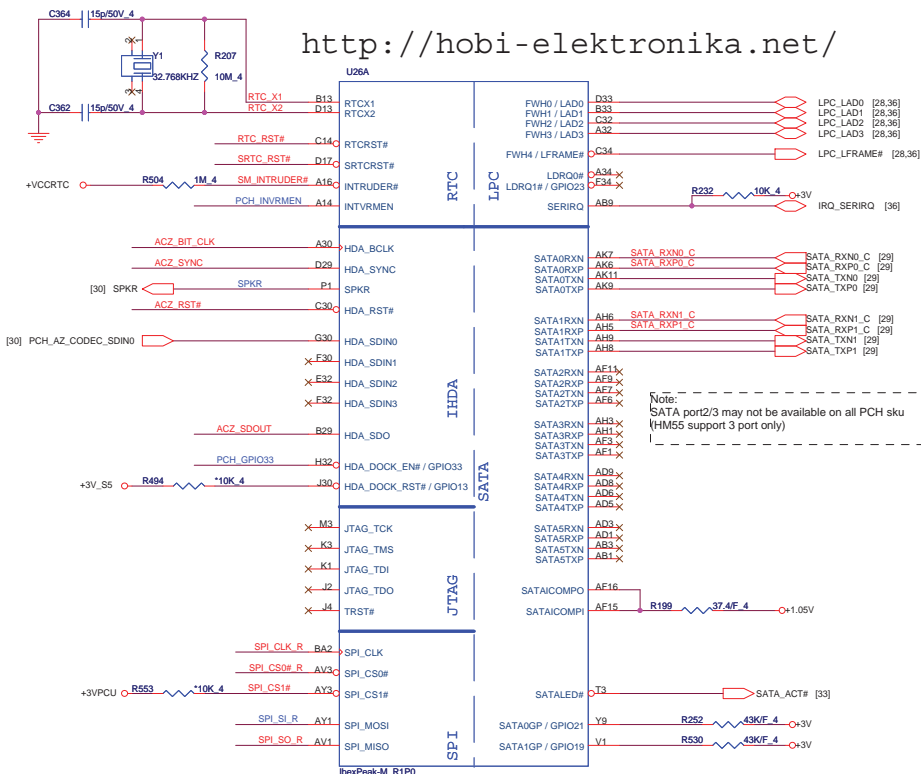


### RTC Circuitry



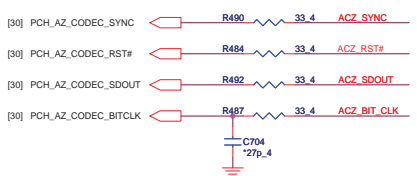
**HDA\_SYNC (PCH strap pin)**  
 Internal weak pull-down  
 VCCVRM=>1.8V (default)  
 external pull-up  
 VCCVRM=>1.5V

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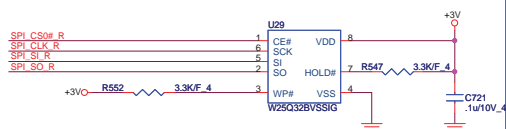


Note:  
 SATA port2/3 may not be available on all PCH sku  
 (HM55 support 3 port only)

### HDA Bus

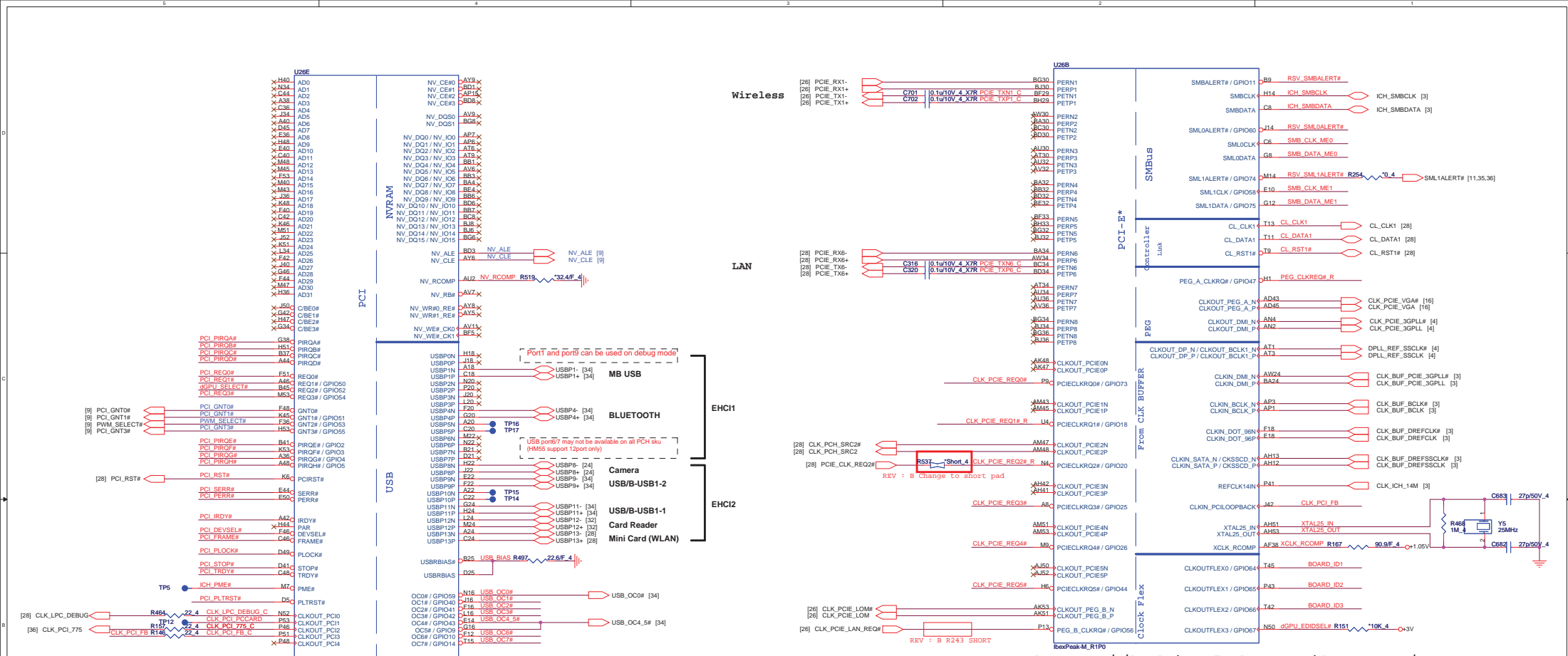


### PCH SPI

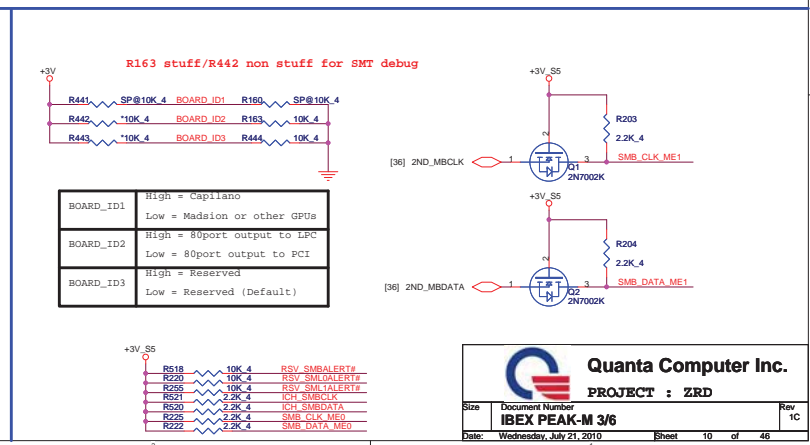
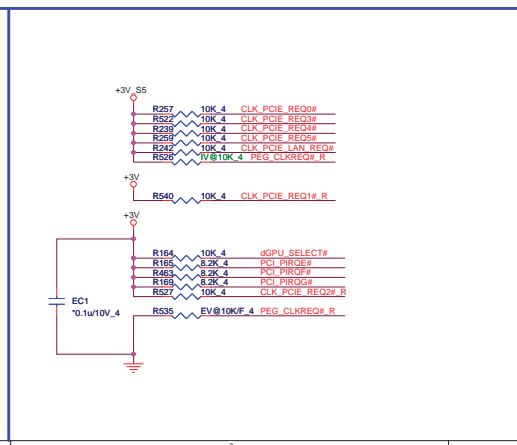
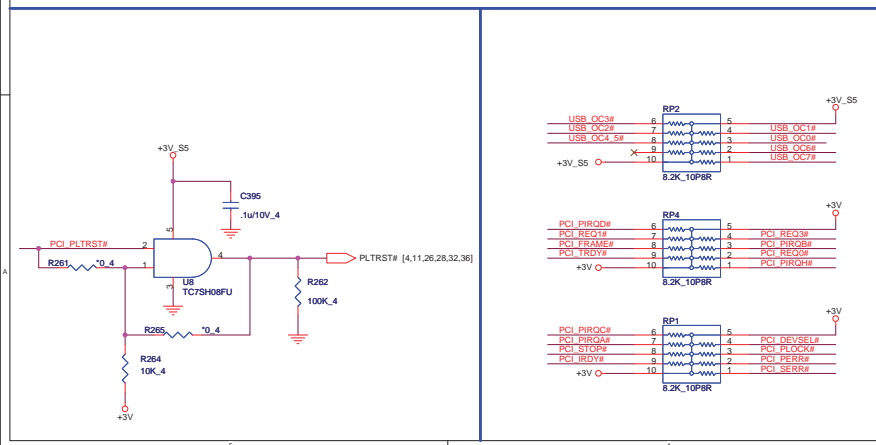


**PCH Strap Pin Configuration Table-1**

<b>INTVRMEN</b>	Integrated 1.05V VRM Enable / Disable	1 = Integrated VRM is enabled 0 = Integrated VRM is disabled	+VCCRTC ○ R511 330K 6 PCH_INVRMEN
<b>SPI_MOSI</b>	TPM Functionality Disable	1 = Enabled 0 = Disable	+3V ○ R551 1K 4 SPI_SI_R
<b>SPKR</b>	Reboot option at power-up	0 = Default Mode (Internal weak Pull-down) 1 = No Reboot Mode with TCO Disabled	+3V ○ R538 1K 4 SPKR
<b>HDA_DOCK_EN#/GPIO33</b>	Flash Descriptor Security Override	0 = Flash Descriptor Security will be overridden 1 = Security measure defined in the Flash Descriptor will be enabled.	PCH_GPIO33 J1 1 2 'SHORT_PAD1
<b>GNT0#, GNT1#</b>	Boot BIOS Strap	(0,0) = LPC (0,1) = Reserved NAND (1,0) = PCI (1,1) = SPI	[10] PCH_GNT0# [10] PCH_GNT1# R158 1K 4 R159 1K 4 R159 1K 4
<b>GNT2#/GPIO53</b>	ESI Strap (Server Only)	ESI compatible mode is for server platforms only	[10] PWM_SELECT# R182 1K 4
<b>GNT3#/GPIO55</b>	Top-Block Swap Override	0 = Top Block Swap Mode 1 = Default Mode (Internal pull-up)	[10] PCH_GNT3# R462 10K 4
<b>NV_ALE</b>	Intel® Anti-Theft Technology HDD Data Protection (Intel AT-d) Enable	1 = Enabled 0 = Disabled (Default)	[10] NV_ALE R213 1K 4 +1.8V
<b>NV_CLE</b>	DMI Termination Voltage	DMI termination voltage. Weak internal pull-up. Do not pull low.	[10] NV_CLE R216 1K 4 +1.8V
<b>GPIO8</b>	Reserved	This signal has a weak internal pull up. NOTE: This signal should not be pulled low	[11] RSV_GPIO8 R215 10K 4 +3V_S5 R214 1K 4
<b>GPIO15</b>	Reserved	0 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality 1 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality	[11] CR_WAKE# R256 1K 4 +3V_S5
<b>GPIO27</b>	On-Die PLL Voltage Regulator <internal weak pull-up>	0 = Disables the VccVRM. 1 = Enables the internal VccVRM to have a clean supply for analog rails.	[11] PCH_GPIO27 R231 10K 4



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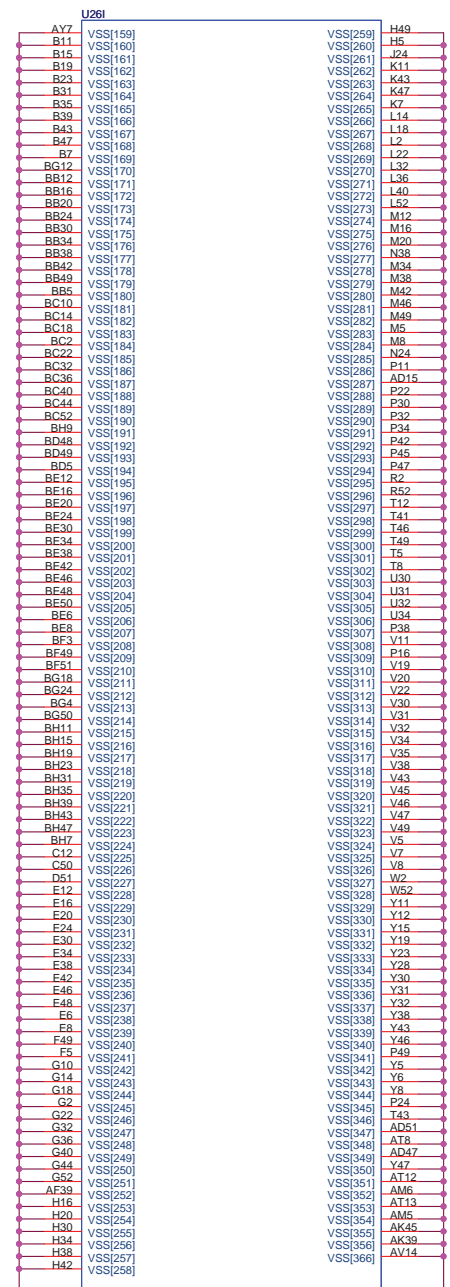
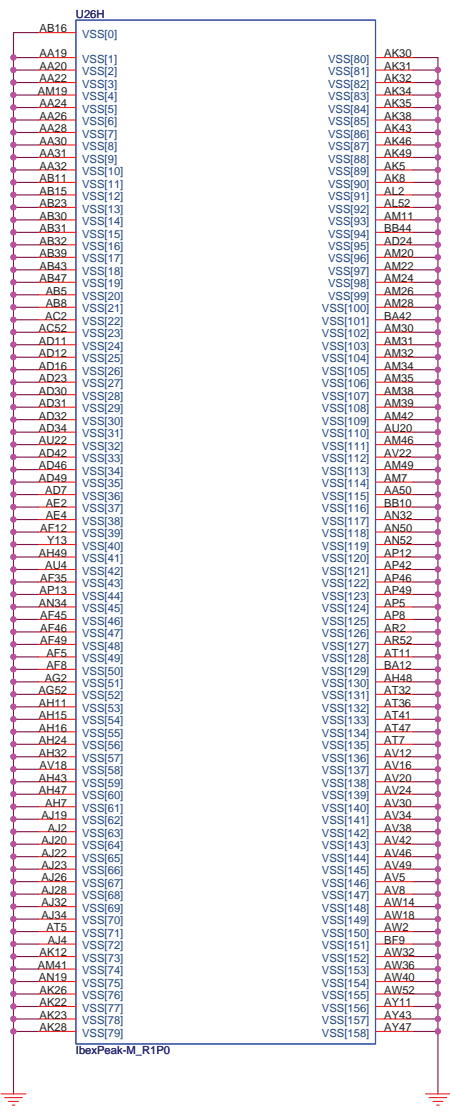
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**IBEX PEAK-M 3/6**  
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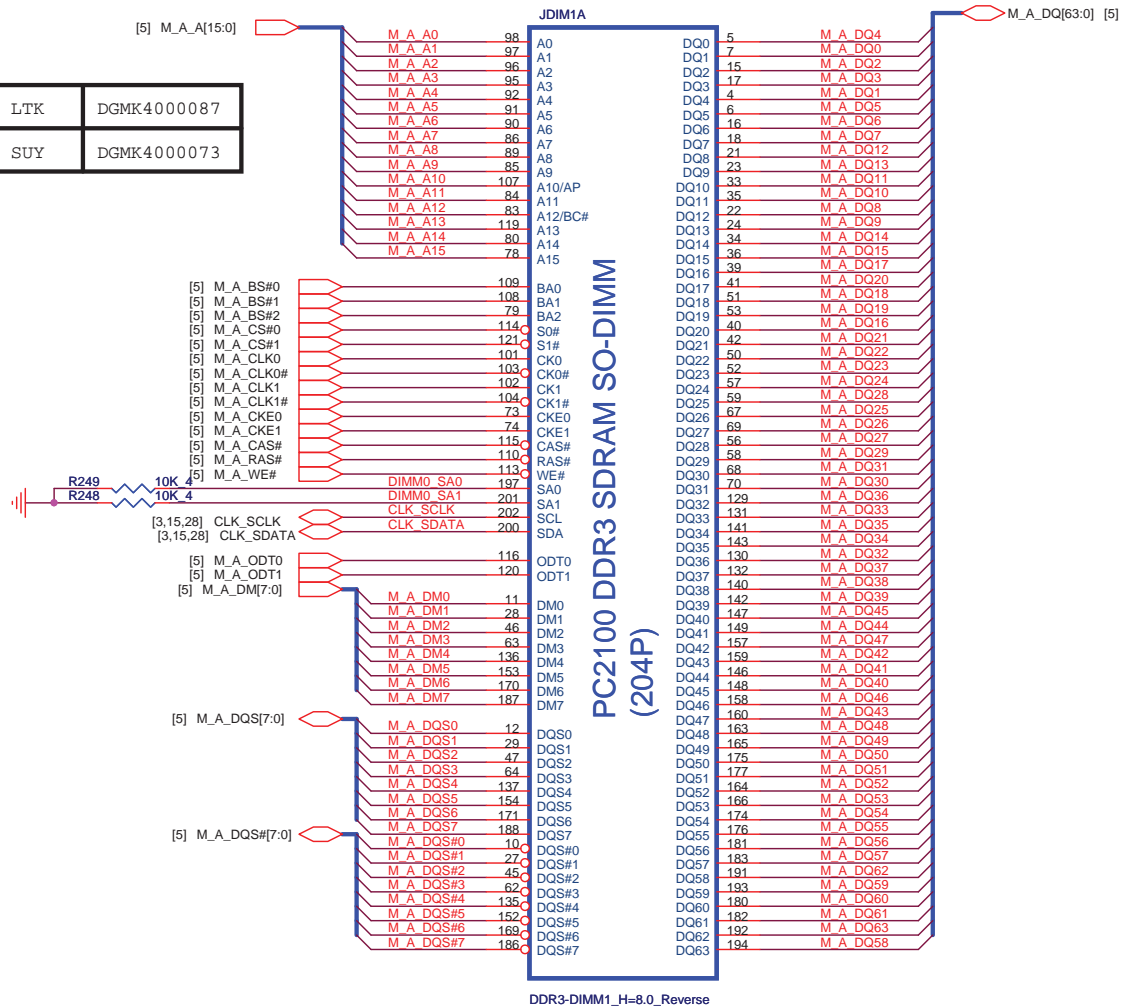
# IBEX PEAK-M (GND)



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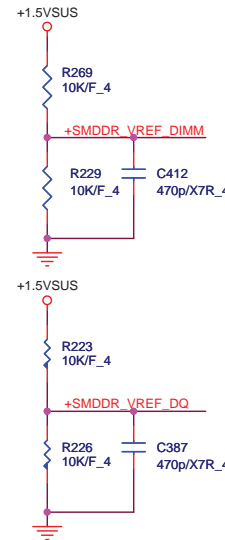
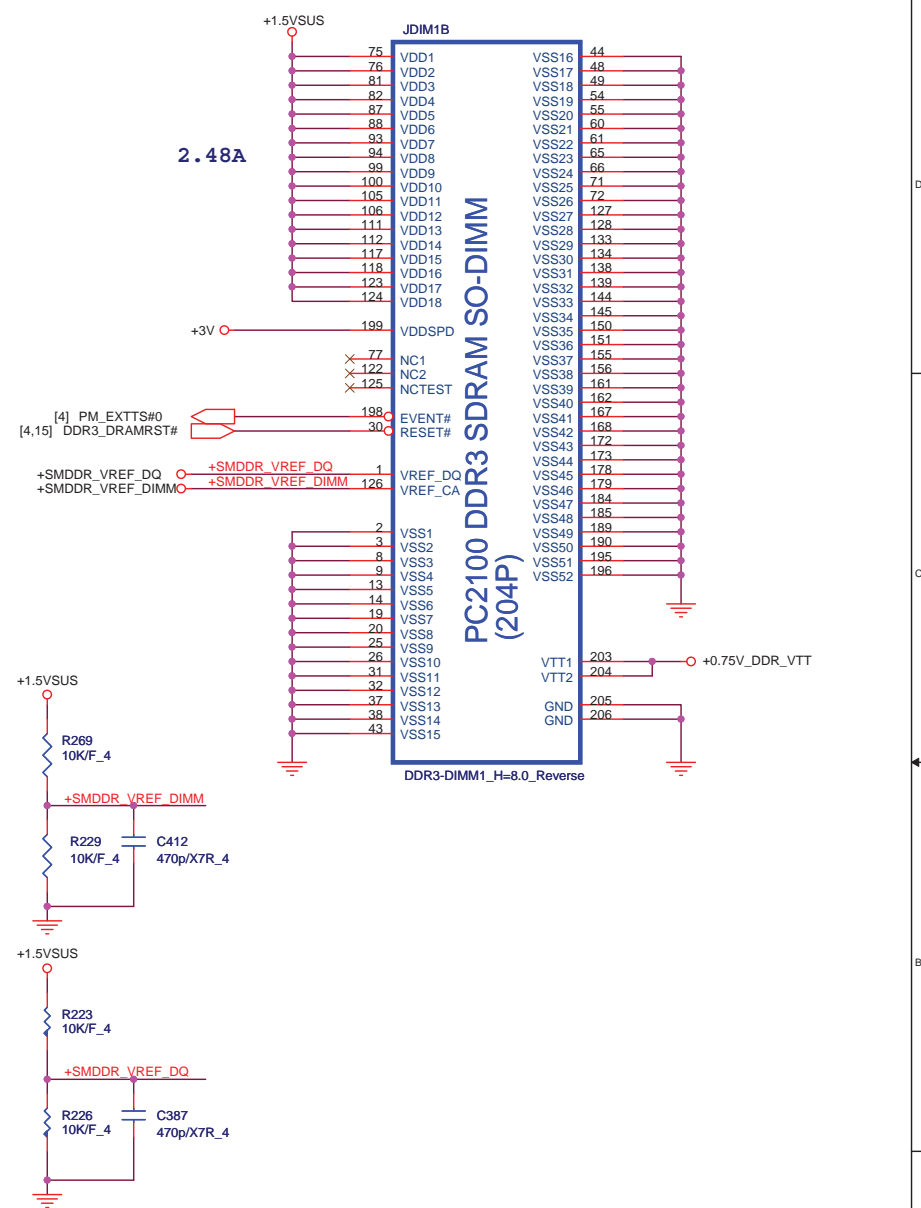
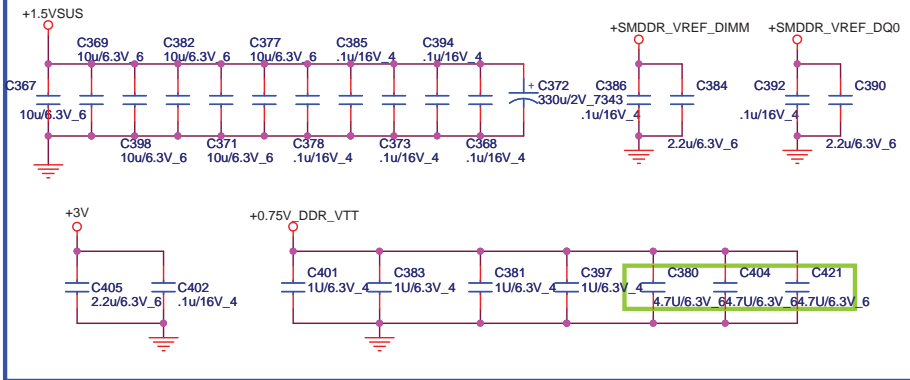
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	<b>IBEX PEAK-M 6/6</b>	1C
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LTK	DGMK4000087
SUY	DGMK4000073



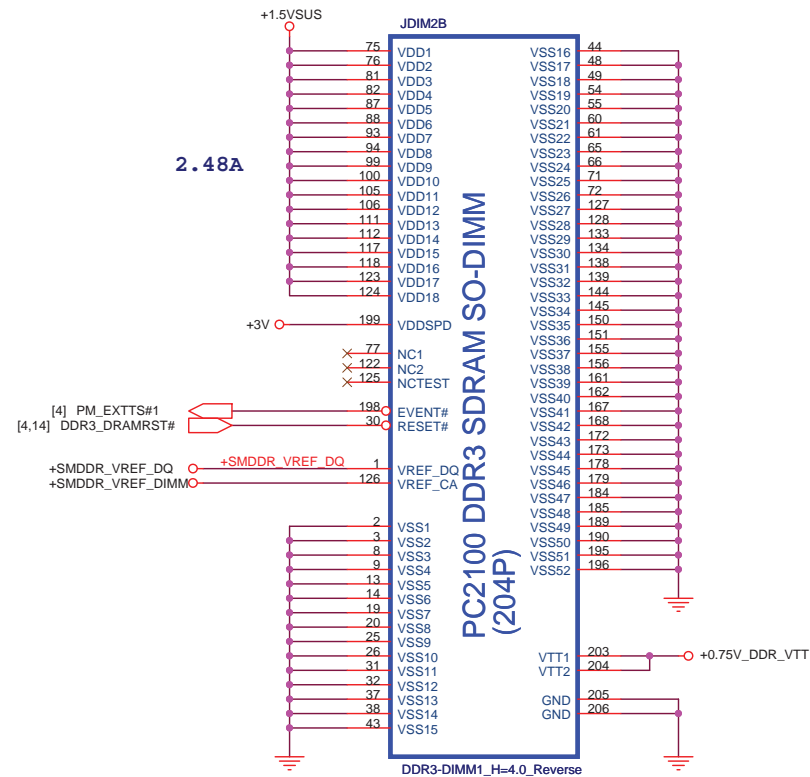
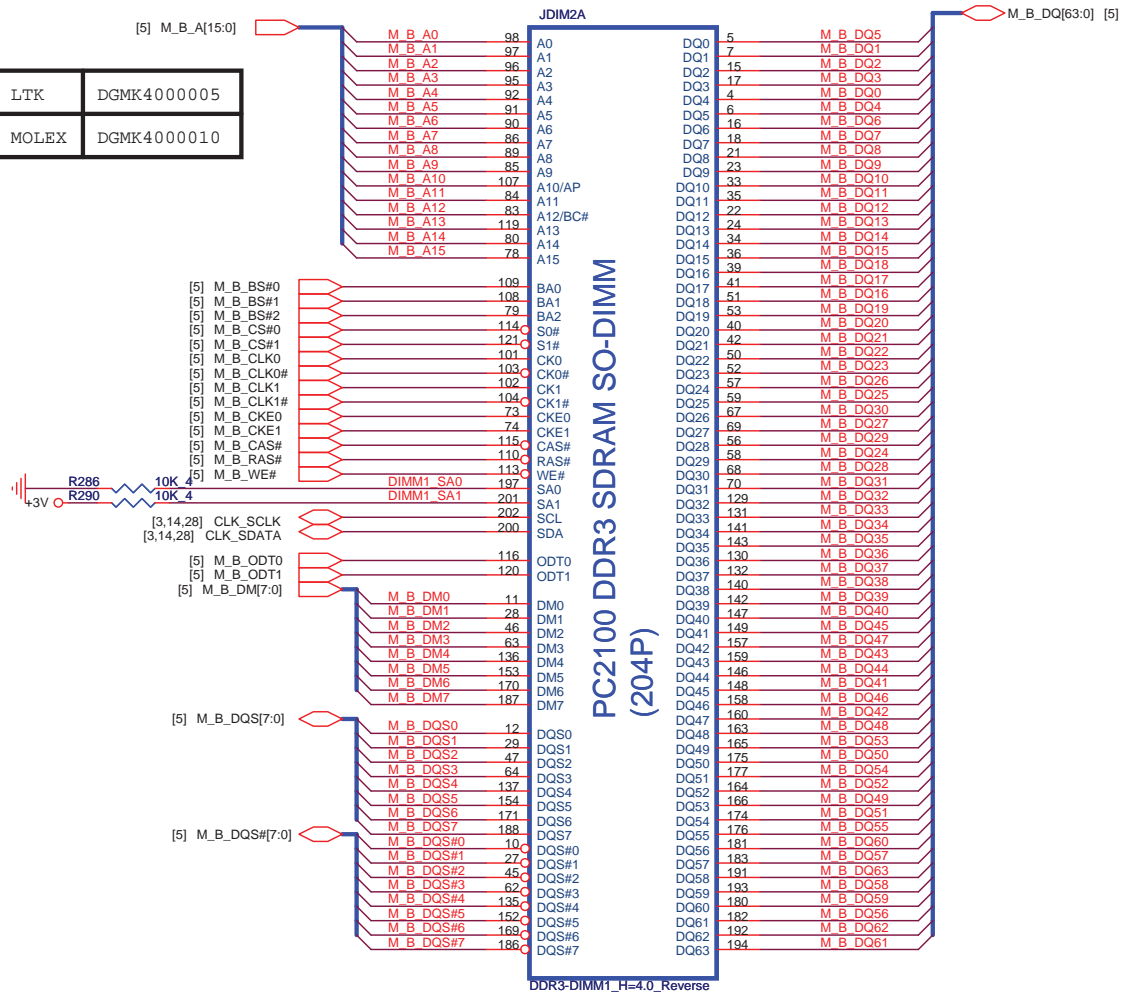
DDR3-DIMM1\_H=8.0\_Reverse

**Place these Caps near So-Dimm0.**

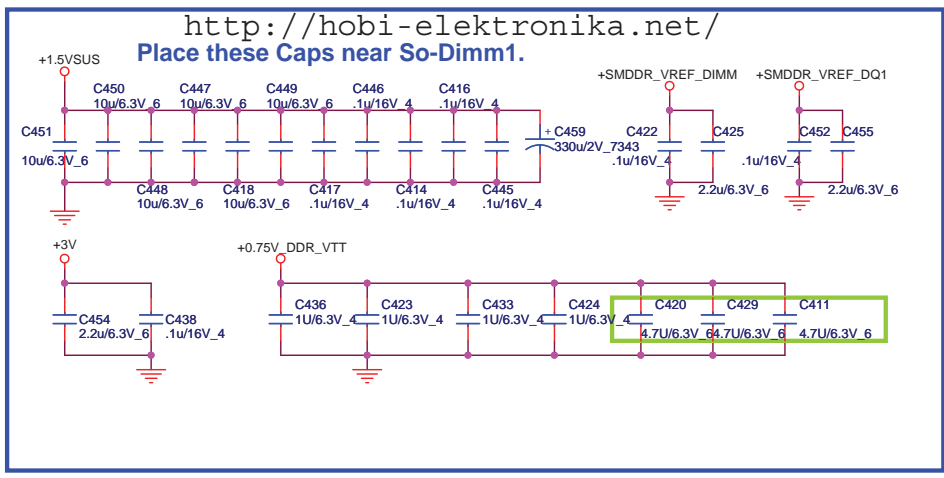




LTK	DGMK4000005
MOLEX	DGMK4000010



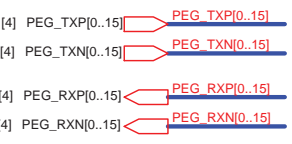
2.48A



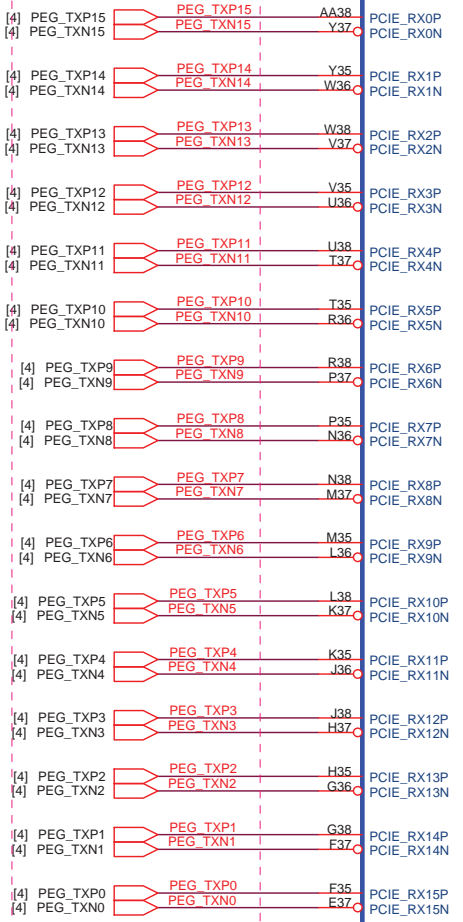
**Quanta Computer Inc.**  
PROJECT : ZRD

Size	Document Number	Rev
	DDRIII SO-DIMM-1	1C
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# GPU\_1(VGA)



0518 SWAP PCIE for VGA side



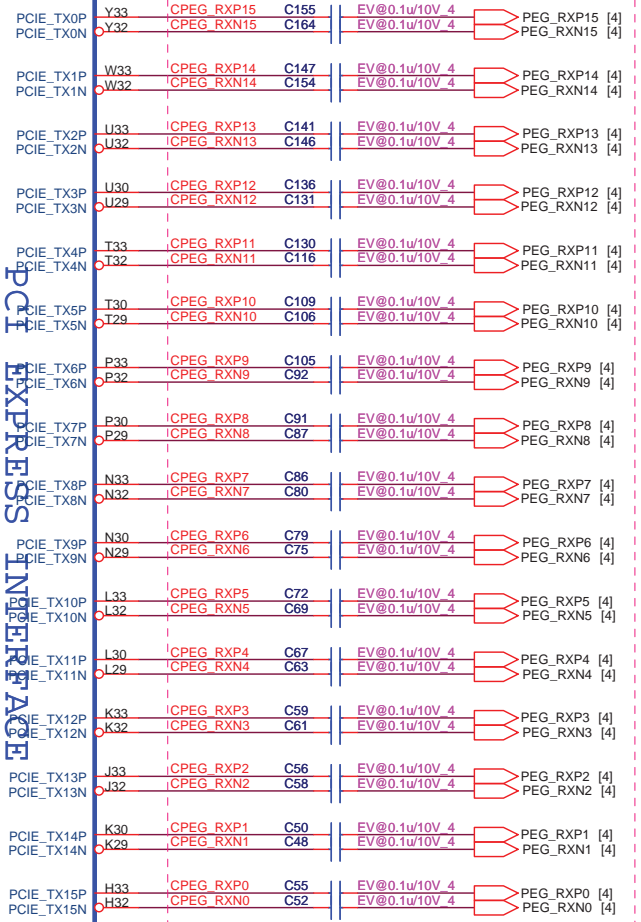
For Broadway, Madison and Park the PWRGOOD ball must be connected to ground



SP@Capilano/Robson

0518 SWAP PCIE for VGA side

PCI EXPRESS INTERFAC



For M97, Broadway, Madison and Park PCIE\_VDDC is 1.0V

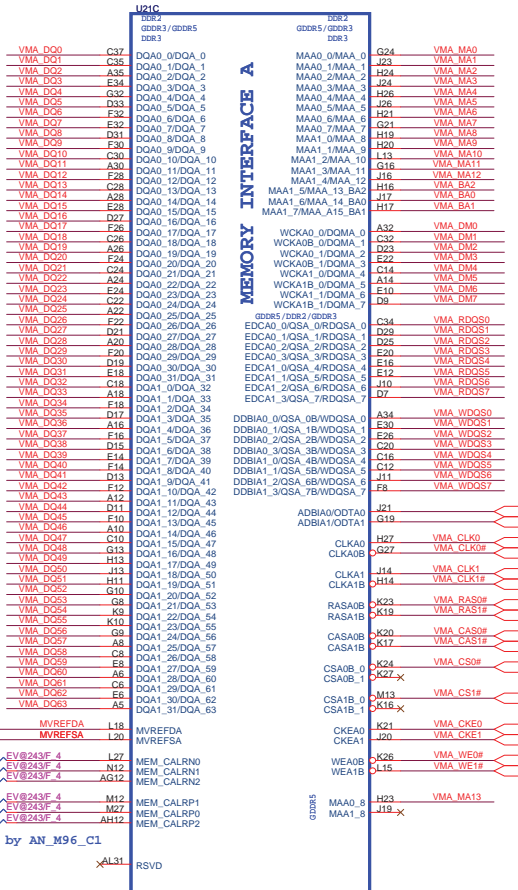
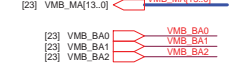
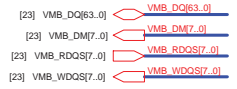
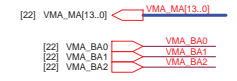
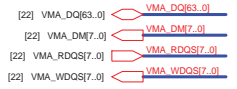
+1.0V

Madison	AJ007720T02
Park	AJ077400T08

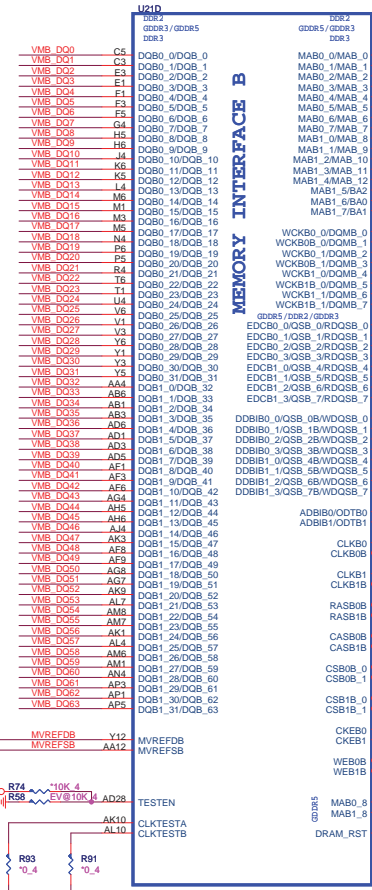
**Quanta Computer Inc.**  
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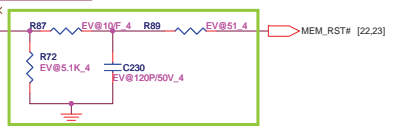
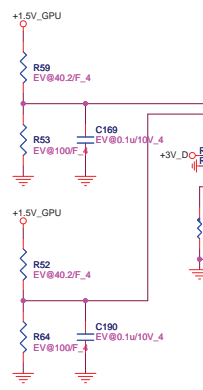
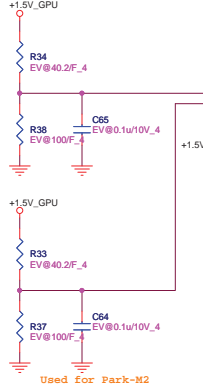




QSA[7..0]  
 QSA#[7..0]



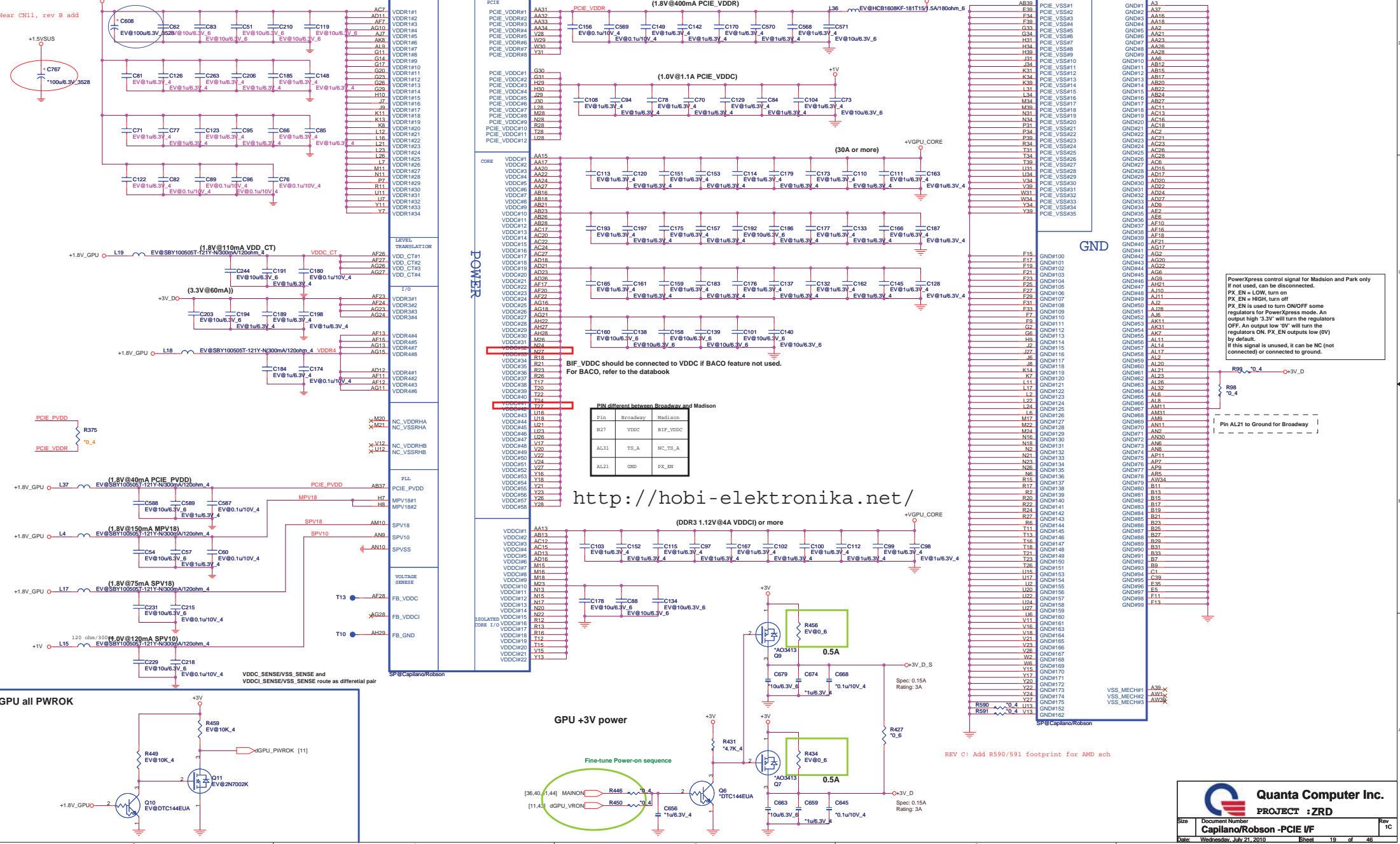
QSB[7..0]  
 QSB#[7..0]



Place all these components very close to GPU

GPU\_4(VGA)

For DDR3, MVDDQ = 1.5V (7.5A)



Pin different between Broadway and Madison

Pin	Broadway	Madison
N27	VDDC	BIF_VDDC
AL31	TS_A	NC_TS_A
AL21	GND	PX_EN

BIF\_VDDC should be connected to VDDC if BACO feature not used. For BACO, refer to the databook

<http://hobi-elektronika.net/>

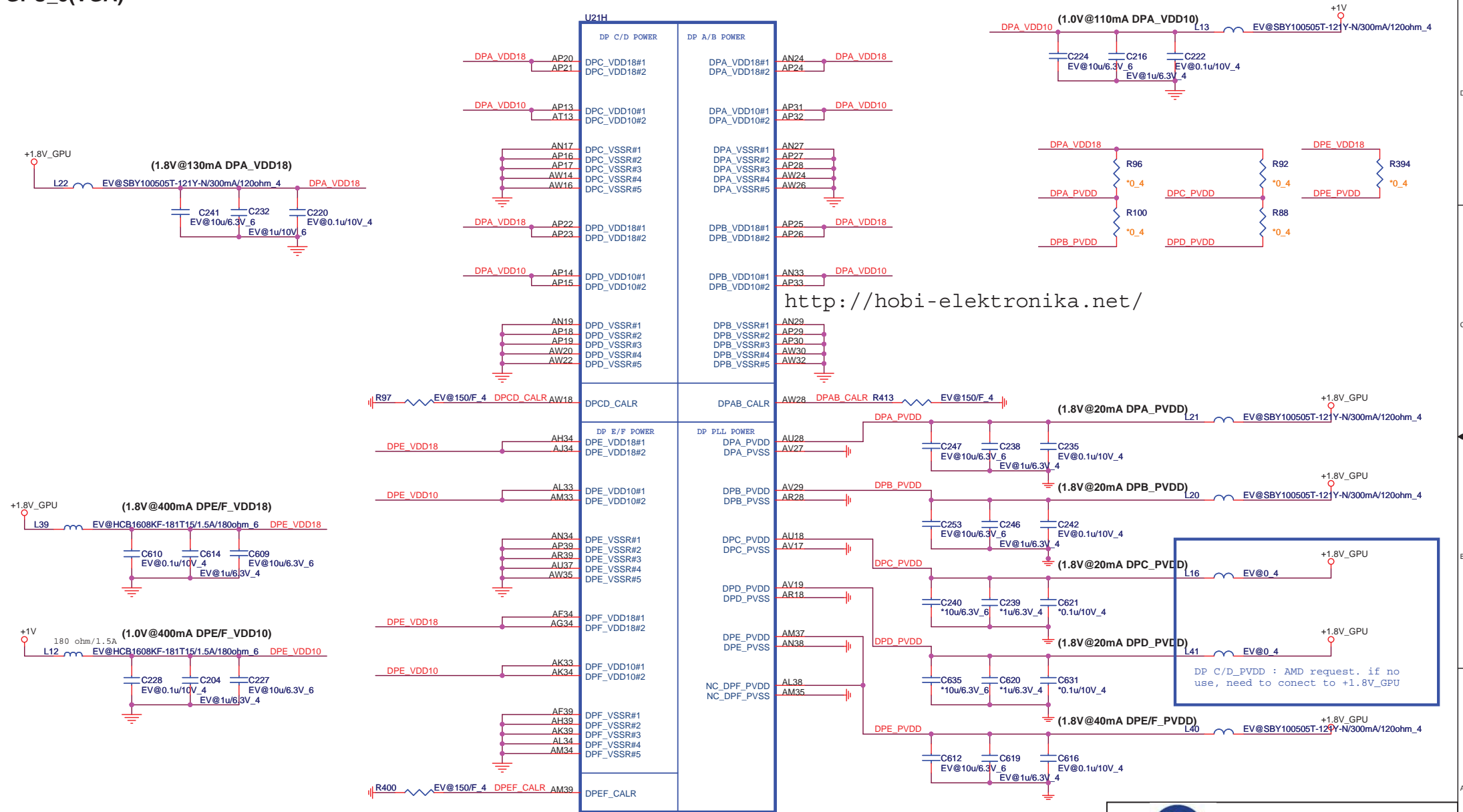
PowerXpress control signal for Madison and Park only  
 If not used, can be disconnected.  
 PX\_EN = LOW, turn on  
 PX\_EN = HIGH, turn off  
 PX\_EN is used to turn ON/OFF some regulators for PowerXpress mode. An output high 3.3V will turn the regulators OFF. An output low 0V will turn the regulators ON. PX\_EN outputs low (0V) by default.  
 If this signal is unused, it can be NC (not connected) or connected to ground.

Pin AL21 to Ground for Broadway

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# GPU\_5(VGA)



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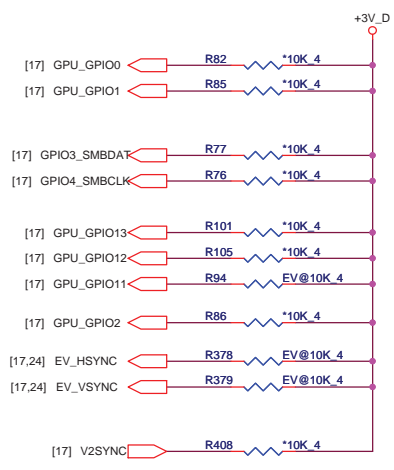
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DP C/D\_PVDD : AMD request. if no use, need to connect to +1.8V\_GPU

SP@Capilano/Robson



**PIN STRAPS(VGA)**



Size of the primary memory apertures	GPIO[13:11]
128 MB	000
256MB	001
64 MB	010
32 MB	011
More than 512 MB	Not Supported

CONFIGURATION STRAPS				
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET				
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	DEFAULT	REMARK
TX_PWRS_ENB	GPIO0	0 = 50% TX OUTPUT SWING 1 = FULL TX OUTPUT SWING	0	
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0 = TX DE-EMPHASIS DISABLED 1 = TX DE-EMPHASIS ENABLED	0	
BIOS_ROM_EN	GPIO_22_ROMCSB	Enable external BIOS ROM device 0 - Disable external BIOS ROM device 1 - Enable external BIOS ROM device	0	
ROMIDCFG[2:0]	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	001	See ROM table
BIF_GEN2_EN_A	GPIO2	0 = PCIE DEVICE AS 2.5GT/S CAPABLE 1 = PCIE DEVICE AS 5GT/S CAPABLE	0	
GPIO_8_ROMSO H2SYNC GPIO_21_BB_EN	GPIO8 H2SYNC GPIO21	Reserved Only	0	
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1:0] 00: NO AUDIO FUNCTION. 01: AUDIO FOR DISPLAYPORT AND HDMI IF ADAPTER IS DETECTED. 10: AUDIO FOR DISPLAYPORT ONLY. 11: AUDIO FOR BOTH DISPLAYPORT AND HDMI.	11	See Audio table
GPIO_9_ROMSI	GPIO9	0 = VGA controller capacity enable	0	
VIP_DEVICE_STRAP_ENA	V2SYNC	0 = DRIVER would ignore the value sample on VHAD_0 during RESET.	0	

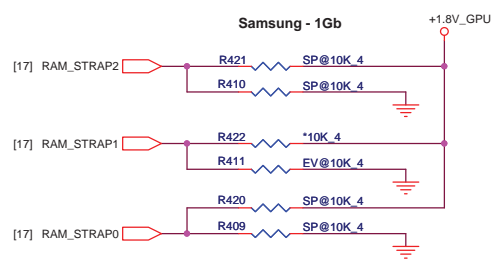
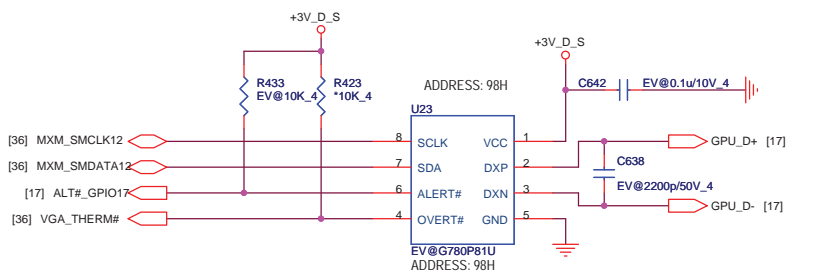
**DDR3 Memory Aperture size(GPU)**

DDR3 Memory size					
Vendor	Vendor P/N	STN B/S P/N	RAM_STRAP2 DVPDATA_2	RAM_STRAP1 DVPDATA_1	RAM_STRAP0 DVPDATA_0
Hynix			1	1	0
	H5TQ1G63BFR-12C	AKD5LZGTW04 (64M*16)	1	0	0
	H5TQ2G63BFR-12C	AKD5MGGTW03 (128M*16)	1	0	1
Samsung					
	K4W1G1646E-HC12	AKD5LGGT506 (64M*16)	0	0	0
	K4W2G1646B-HC12	AKD5MGGT500 (128m*16)	0	0	1
AMD					
	23EY2387MA12-SZ	AKD5LGGT700	0	1	0

**Thermal Sensor(VGA)**

Vendor	P/N
WINDBOND	AL83L771K01
GMT	AL000780000

USD0.16



RAM\_STRAP2 SET DDR3 Vendor  
RAM\_STRAP[1:0] SET SIZE.

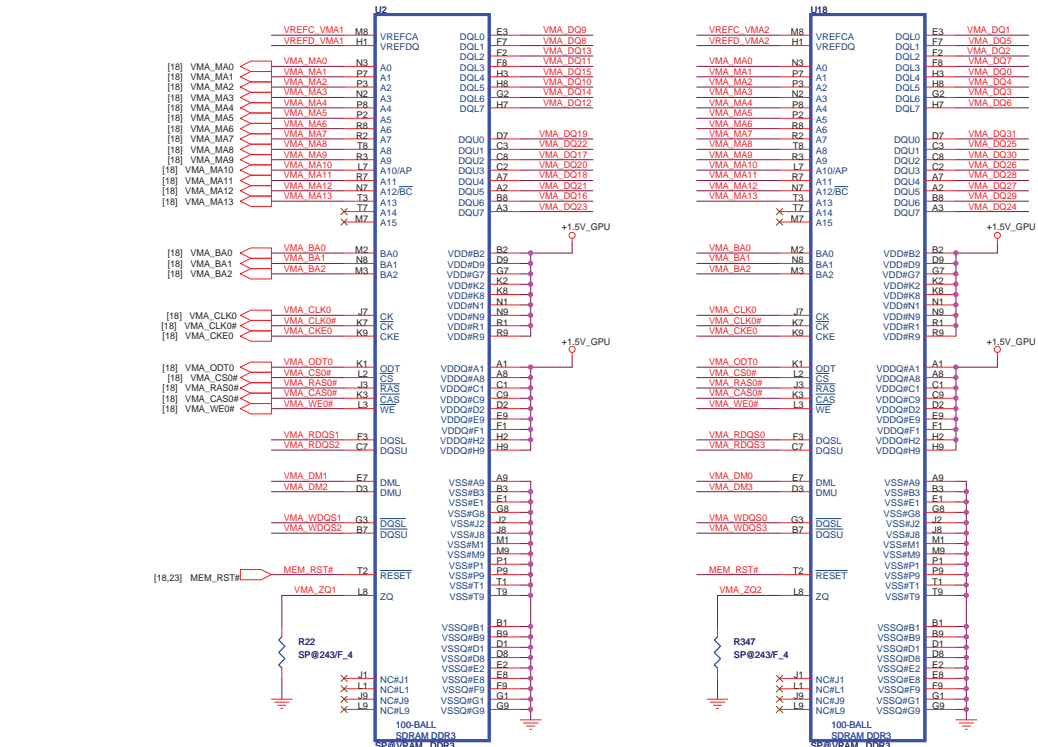
**Quanta Computer Inc.**  
PROJECT :ZRD

Size Document Number Strip/Thermal Rev 1C  
Date: Wednesday, July 21, 2010 Sheet 21 of 46

# CHANNEL A: 512MB DDR3 (64M\*16\*4pcs)

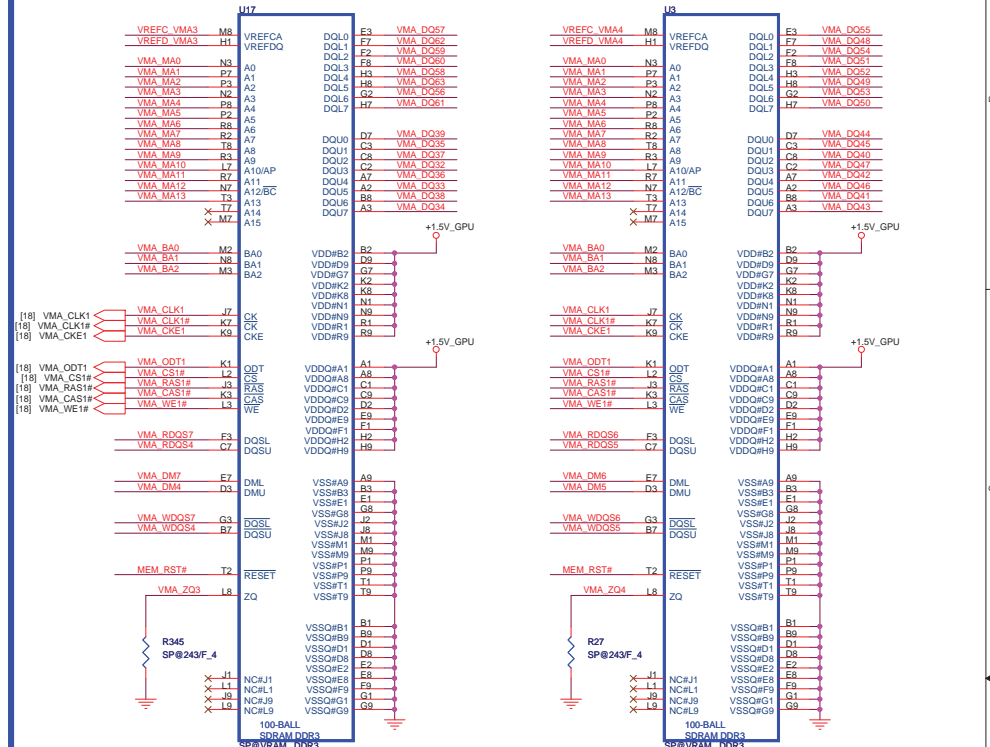
- [18] VMA\_DQ[63..0] VMA\_DQ[63..0]
- [18] VMA\_DM[7..0] VMA\_DM[7..0]
- [18] VMA\_RDQS[7..0] VMA\_RDQS[7..0]
- [18] VMA\_WDQS[7..0] VMA\_WDQS[7..0]

QSA[7..0]  
QSA#[7..0]



TOP Left

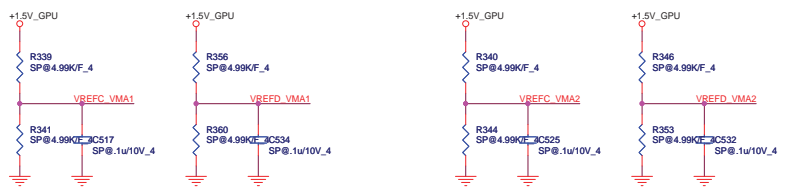
BOT Left



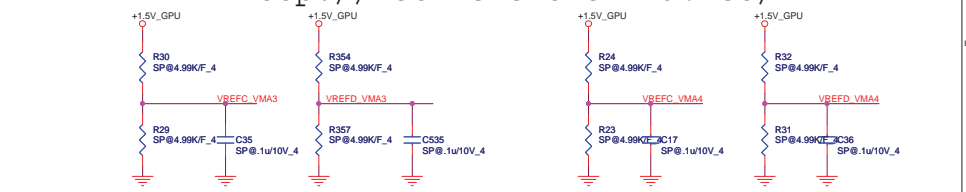
BOT Right

TOP Right

## Group-A0 VREF

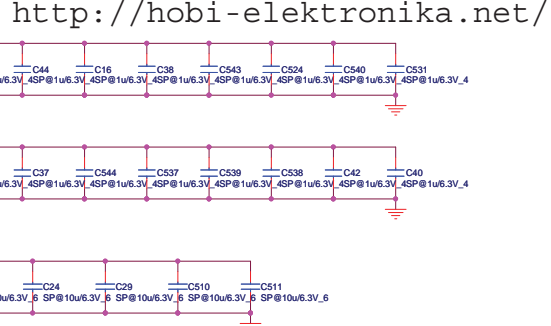


## Group-A1 VREF

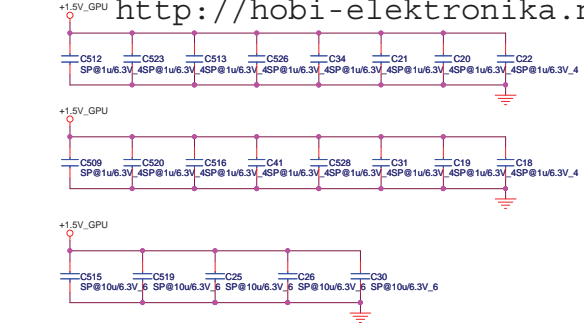


## MEM\_A0 CLK

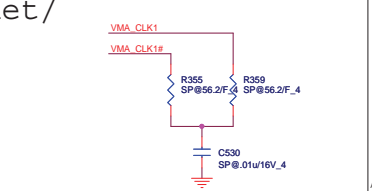
## Group-A0 decoupling CAP



## Group-A1 decoupling CAP



## MEM\_A1 CLK



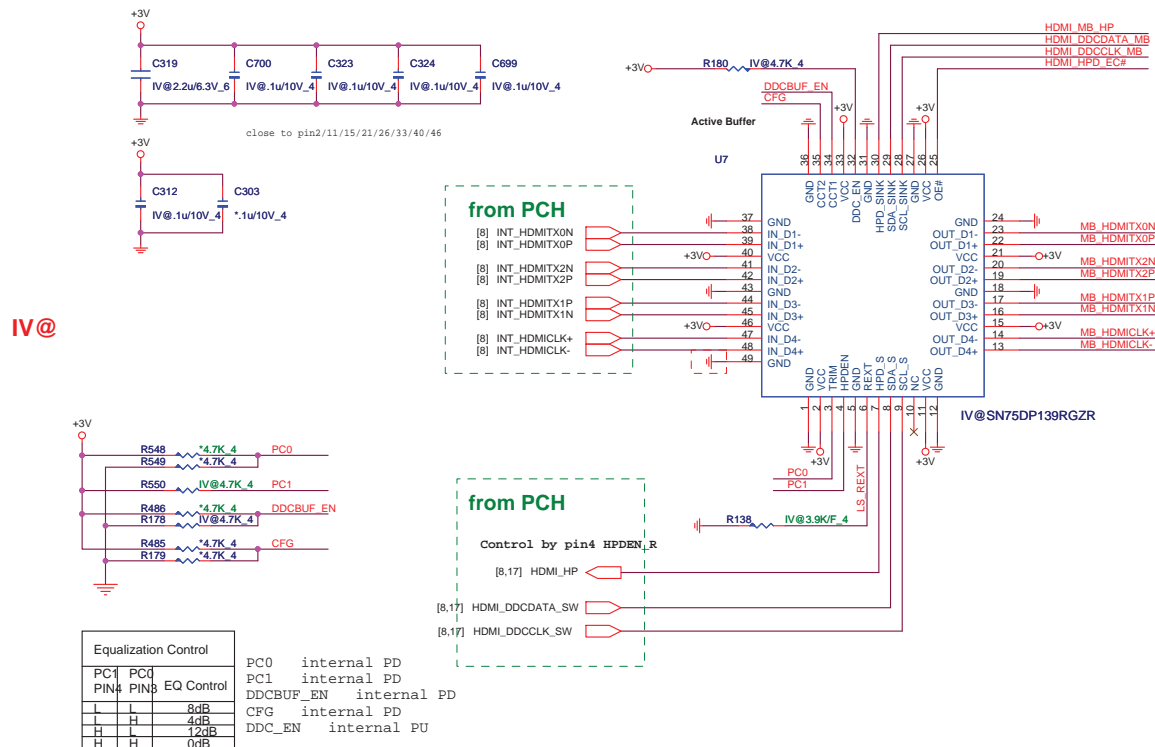
**Quanta Computer Inc.**  
PROJECT : ZRD

Size	Document Number	<b>MEMORY 1 channel A</b>	Rev
Date	Wednesday, July 21, 2010	Sheet 22 of 46	



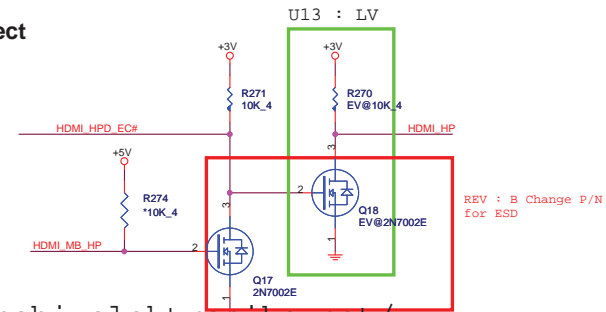


# HDMI LEVEL SHIFTER



# HDMI-detect

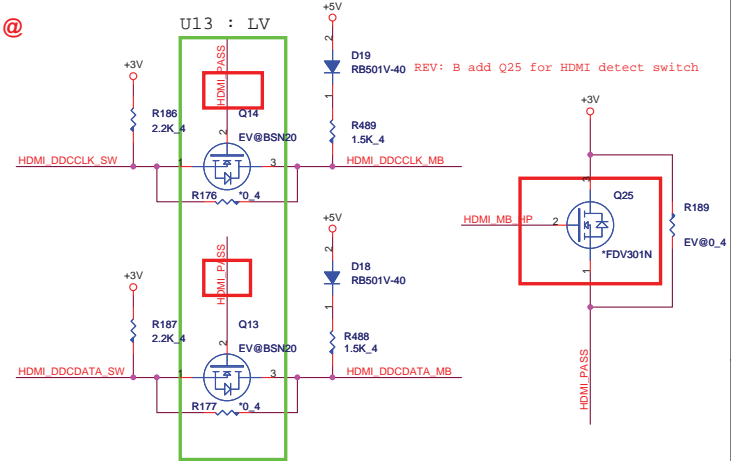
EV@



<http://hobi-elektronika.net/>

# I2C

EV@

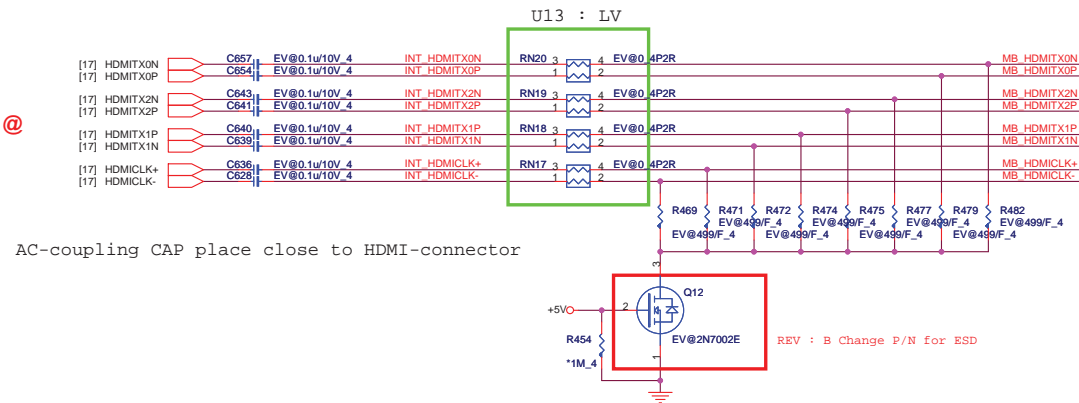


<http://hobi-elektronika.net/>

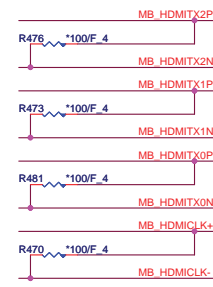
# Switchable Graphic HDMI source

<http://hobi-elektronika.net/>

EV@

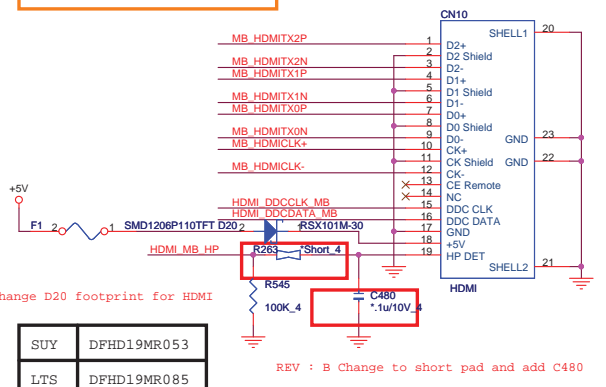


# EMI

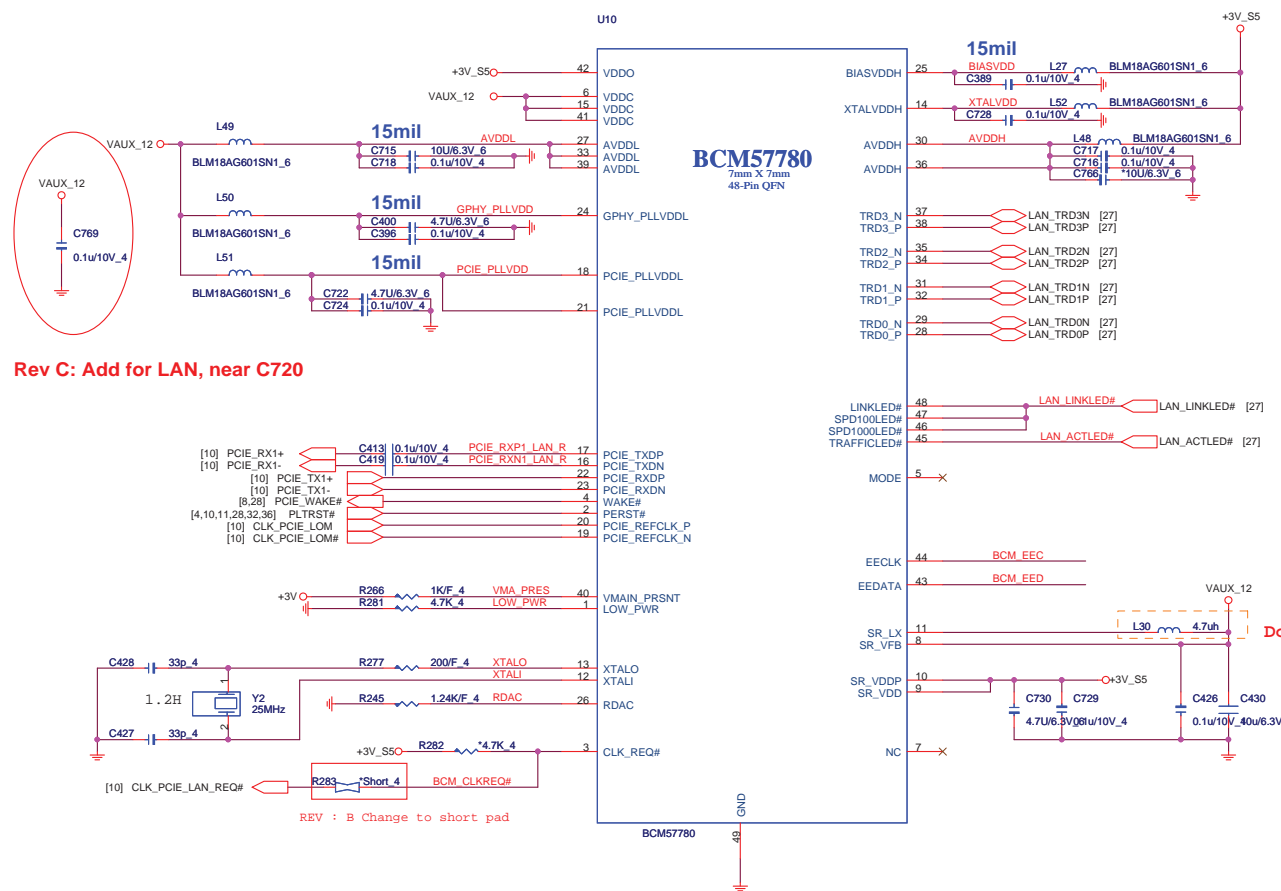


# HDMI connector

REV : C Location :D20 Change Footprint & P/N



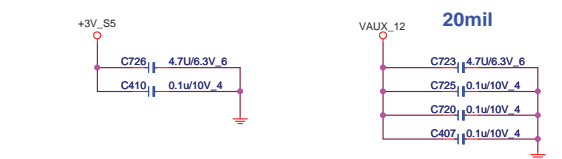
# Giga-LAN BCM57780



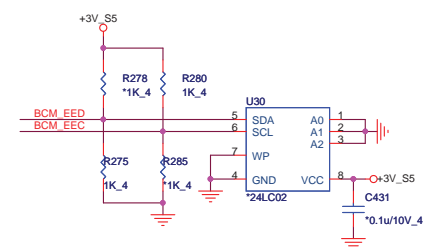
Rev C: Add for LAN, near C720

Don't route under Choke.

## LAN POWER



## EEPROM



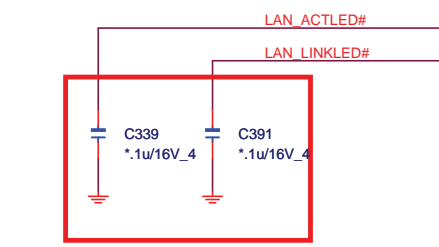
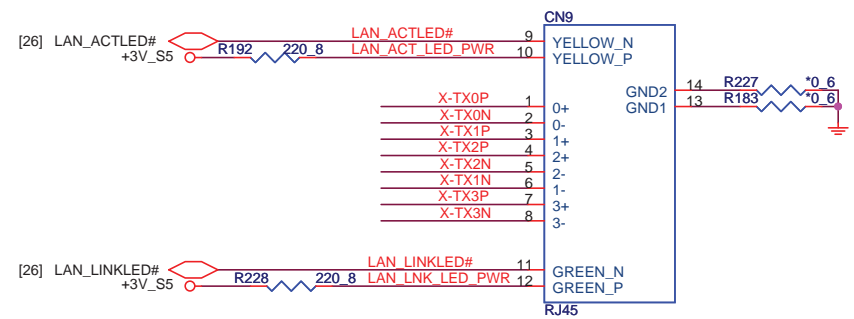
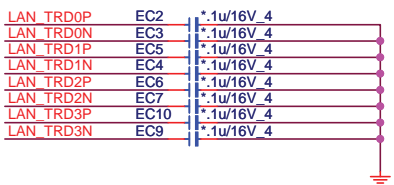
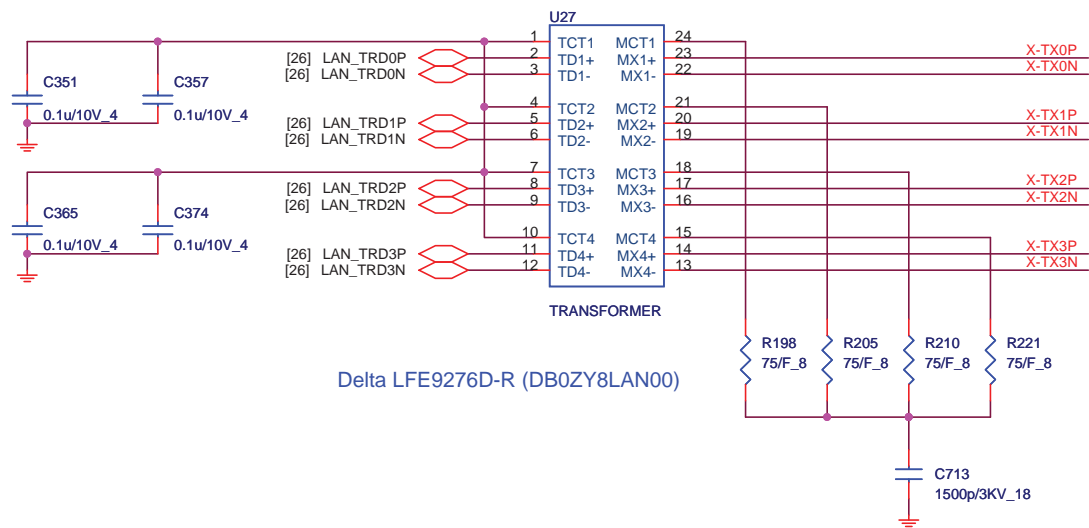
### EEPROM Strapping

EEPROM Type	EECLK	EEDATA
24LC02	1	1
Internal	1	0




# TRANSFORMER

SUY	DFTJ12FR109
AEC	DFTJ12FR135



REV : B Change to 0402 for ESD



**Quanta Computer Inc.**  
PROJECT : ZRD

Size	Document Number	Rev
	<b>LAN Transformer and RJ45</b>	1C
Date:	Wednesday, July 21, 2010	Sheet 27 of 46

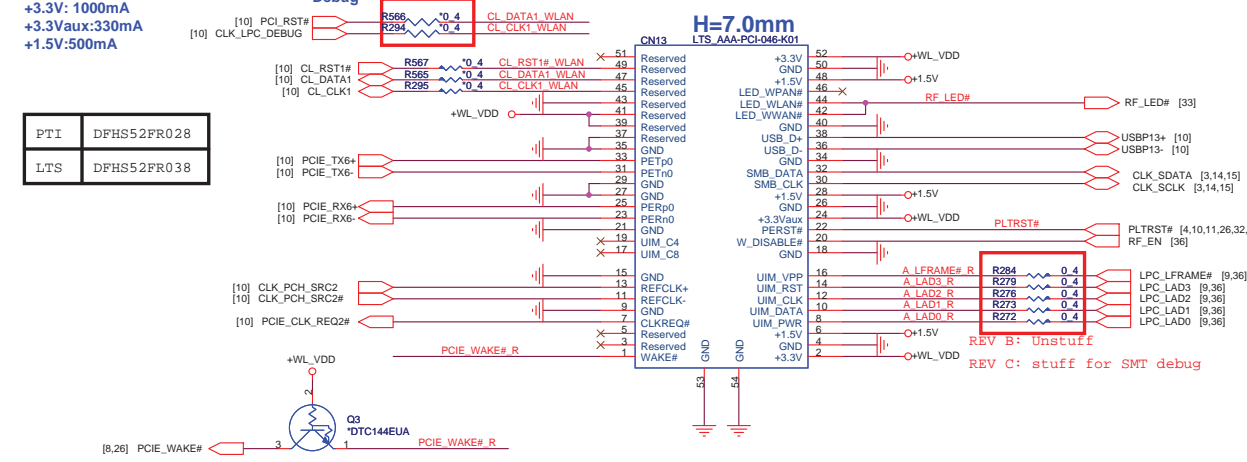
# MINI-CARD WLAN(MPC)

+3.3V: 1000mA  
 +3.3Vaux: 330mA  
 +1.5V: 500mA

REV : B Unstuff

Debug

PTI	DFHS52FR028
LTS	DFHS52FR038

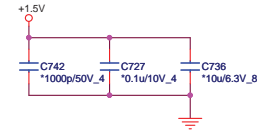
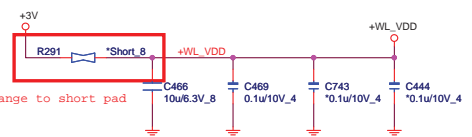


H=7.0mm  
 LTS AAA-PCI-046-K01

Debug

REV B: Unstuff

REV C: stuff for SMT debug



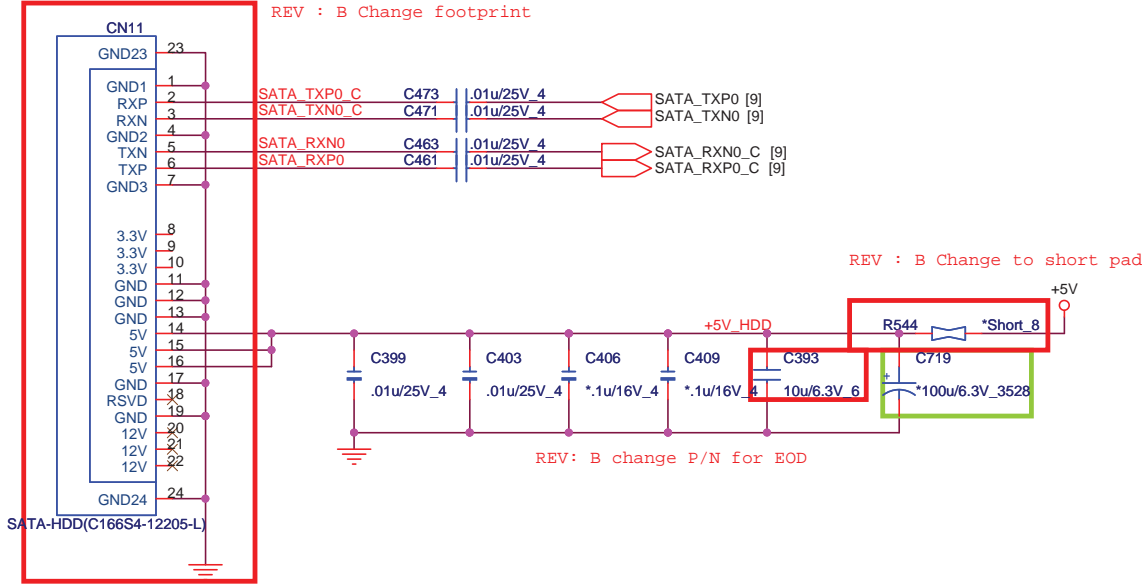
**Quanta Computer Inc.**  
 PROJECT : ZRD

Size	Document Number	Rev
		1C

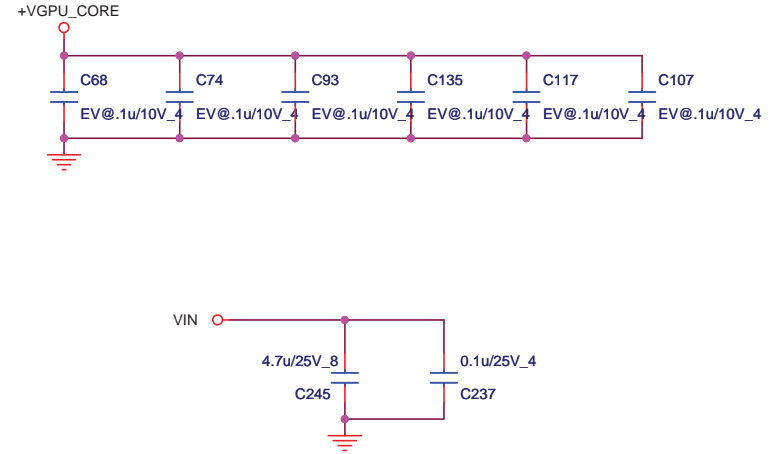
Date: Wednesday, July 21, 2010 Sheet 28 of 46

# MAIN SATA HDD

REV : B Change footprint

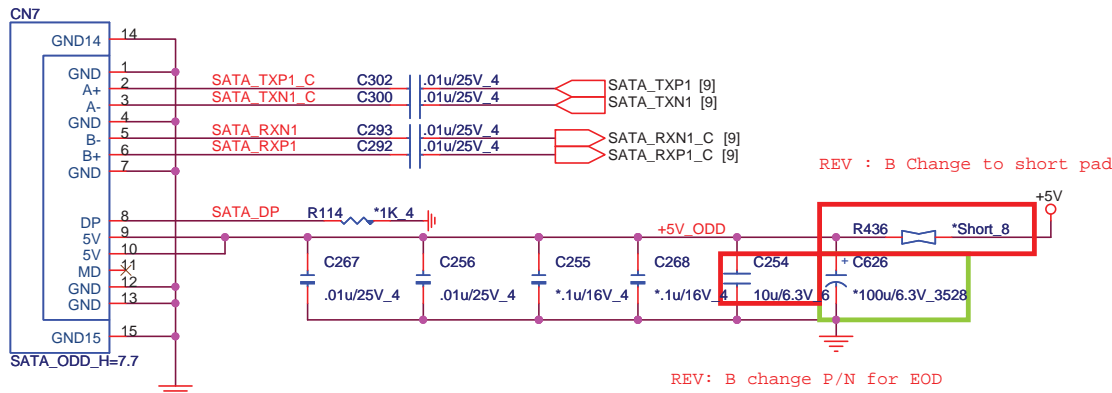


# EE RETURN-PATH CAPACITORS



# ODD (SATA)

<http://hobi-elektronika.net/>



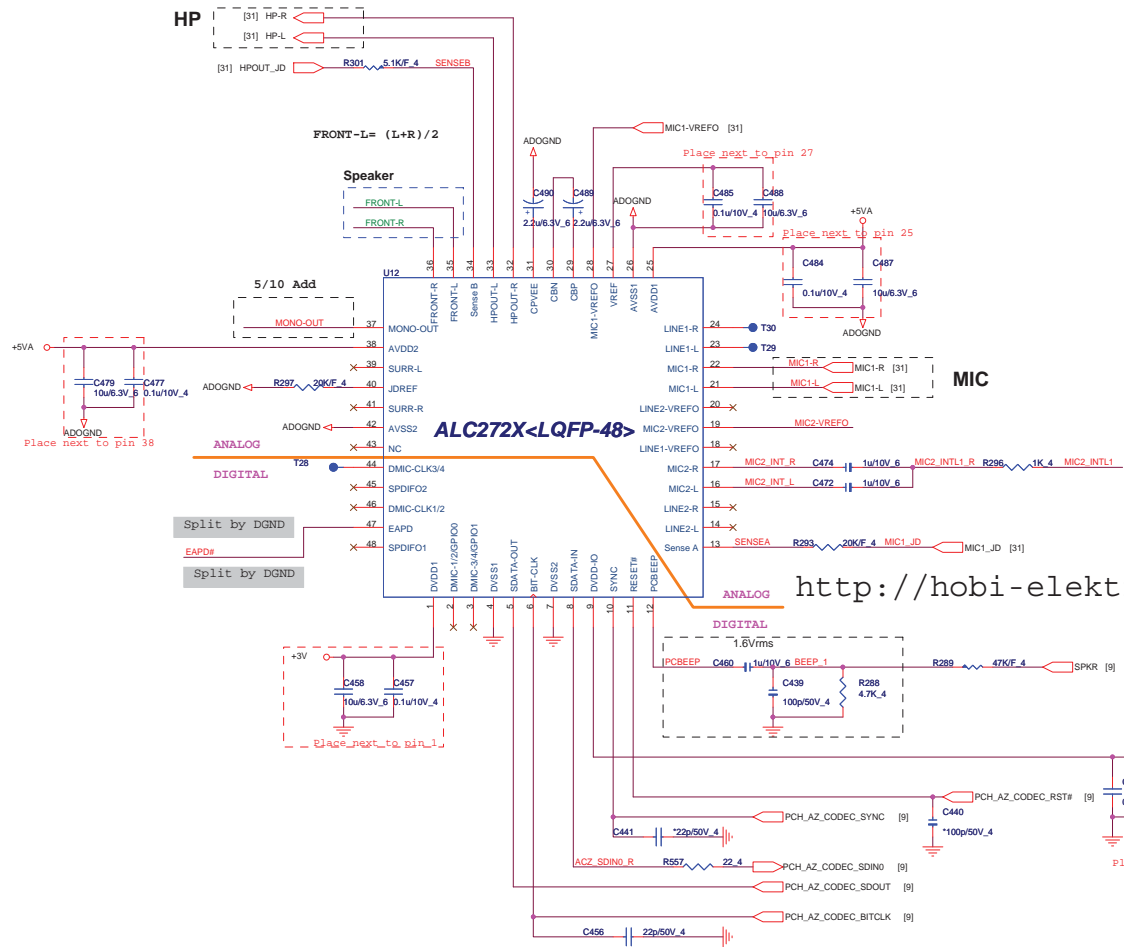
SUY	DFHS22FR214
AOP	DFHS22FR232
AEC	DFHS22FR216

AOP	DFHS13FR011
OTK	DFHS13FR010

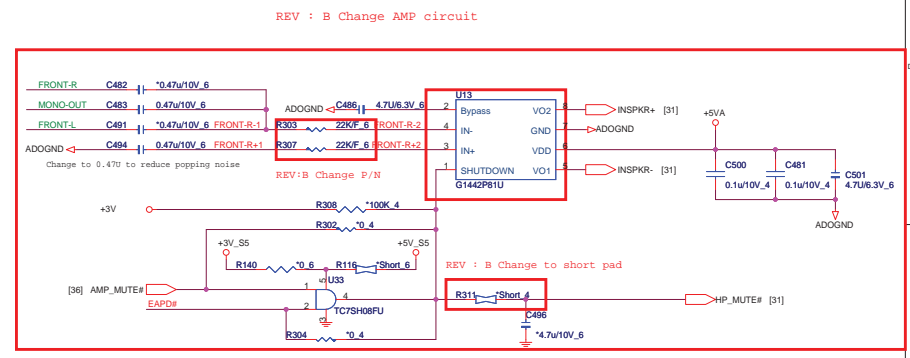
**Quanta Computer Inc.**  
**PROJECT : ZRD**

Size	Document Number	Rev
	<b>SATA-HDD/ODD/RETURN-PATH</b>	1C
Date:	Wednesday, July 21, 2010	Sheet 29 of 46

**Codec(ADO)**



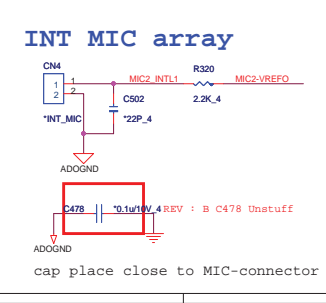
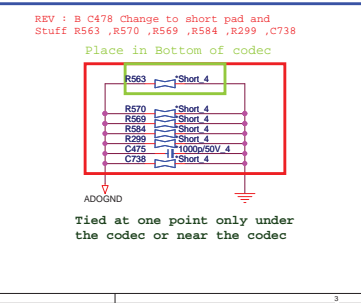
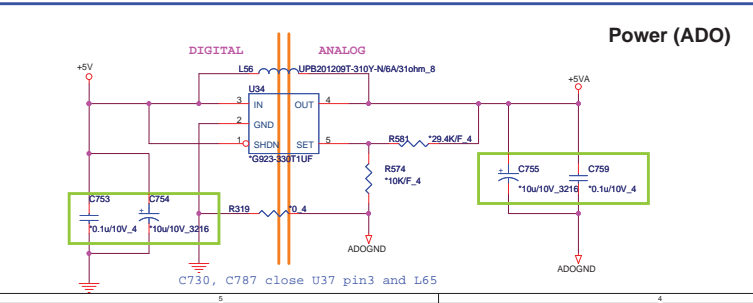
**MUTE(AMP)**



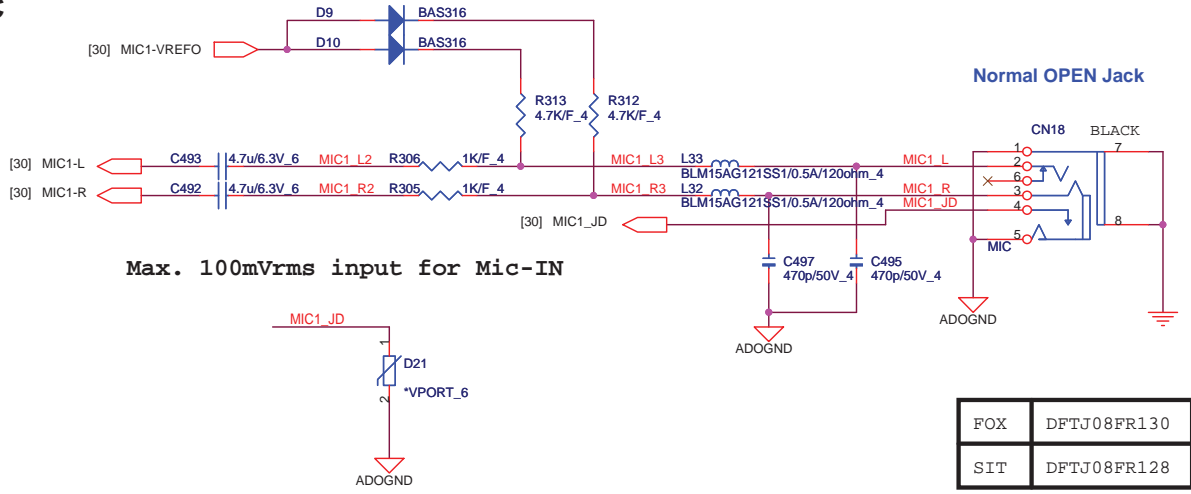
<http://hobi-elektronika.net/>

<http://hobi-elektronika.net/>

<http://hobi-elektronika.net/>  
<http://hobi-elektronika.net/>  
<http://hobi-elektronika.net/>  
<http://hobi-elektronika.net/>  
<http://hobi-elektronika.net/>  
<http://hobi-elektronika.net/>

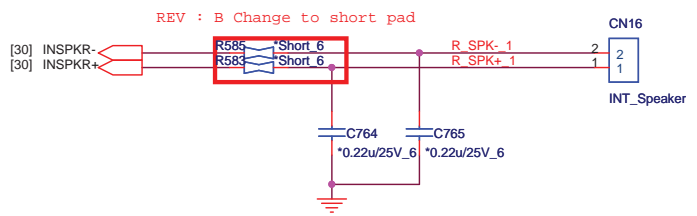


**MIC**



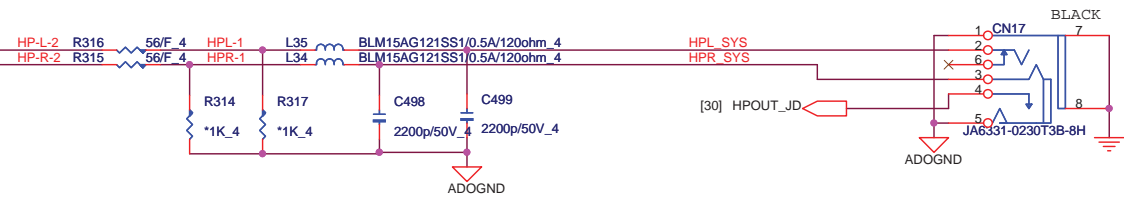
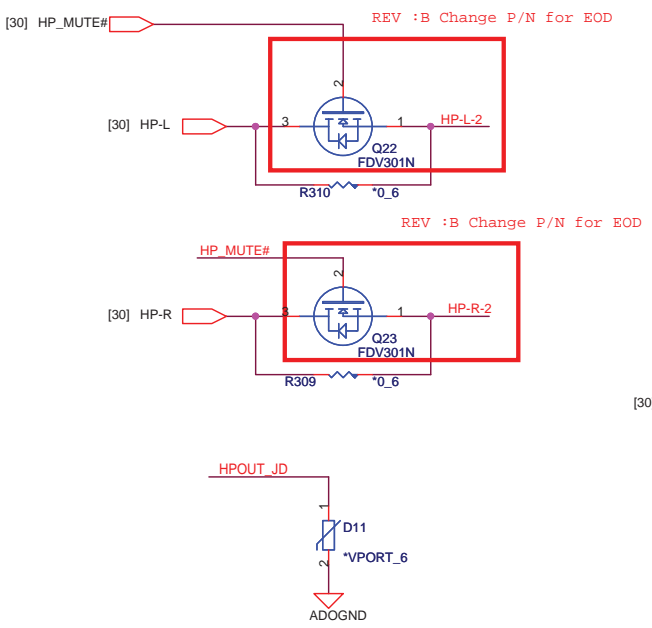
FOX	DFTJ08FR130
SIT	DFTJ08FR128

**Internal Speaker**



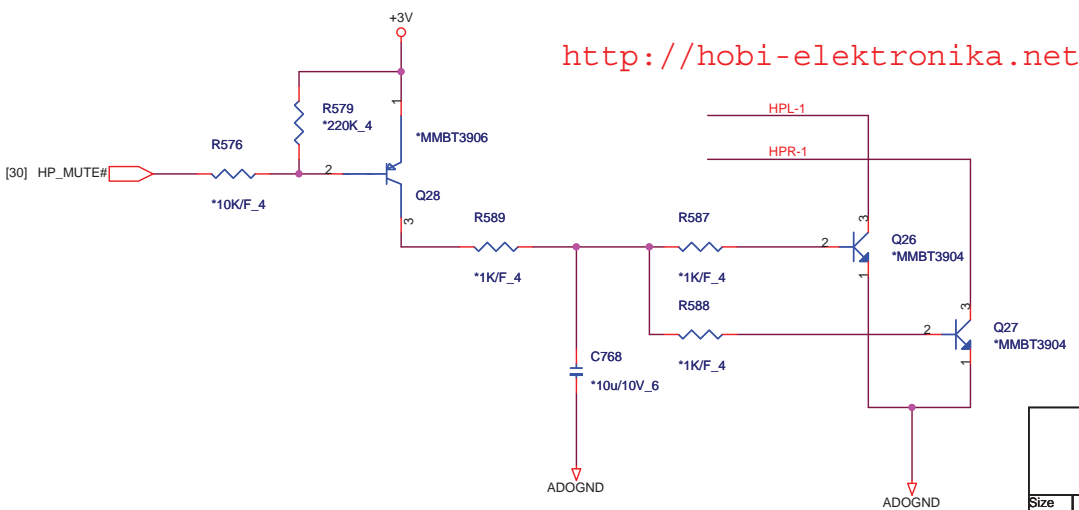
ACS	DFHD02MR311
PTI	DFHD02MR508

**HP/SPDIF**



REV : B Add

<http://hobi-elektronika.net/>

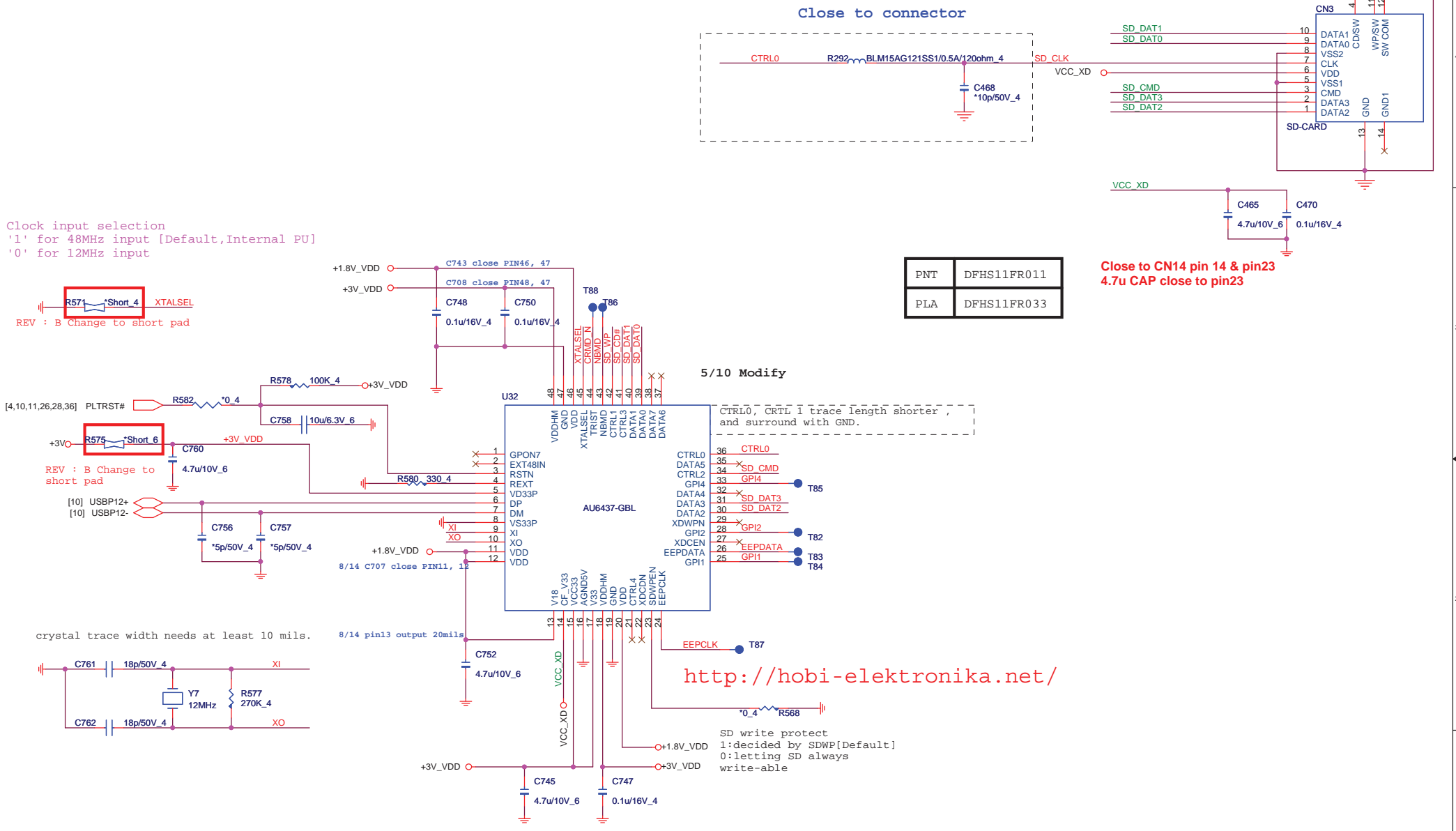


**Quanta Computer Inc.**  
PROJECT : ZRD

Size	Document Number	Rev
	<b>AMP /AUDIO JACK CONN</b>	1C
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# CARD READER Controller

# 2 IN 1 CARD READER (SD/MMC)



Clock input selection  
 '1' for 48MHz input [Default, Internal PU]  
 '0' for 12MHz input

REV : B Change to short pad

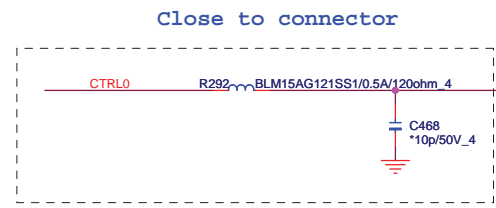
REV : B Change to short pad

5/10 Modify

CTRL0, CTRL1 trace length shorter, and surround with GND.

<http://hobi-elektronika.net/>

SD write protect  
 1:decided by SDWP[Default]  
 0:letting SD always write-able



Close to CN14 pin 14 & pin23  
 4.7u CAP close to pin23

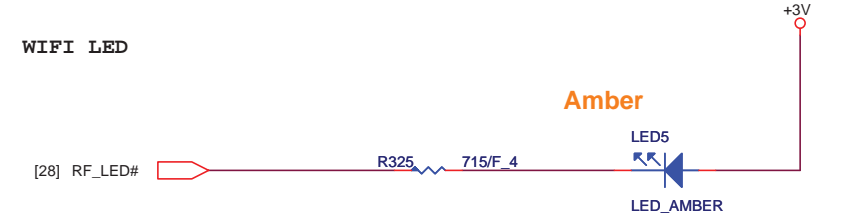
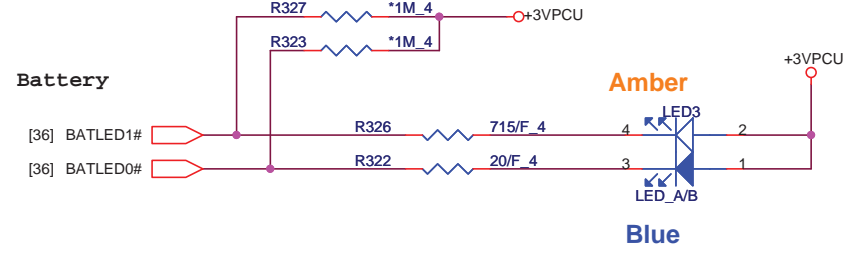
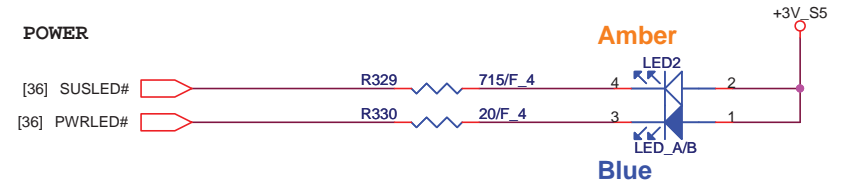
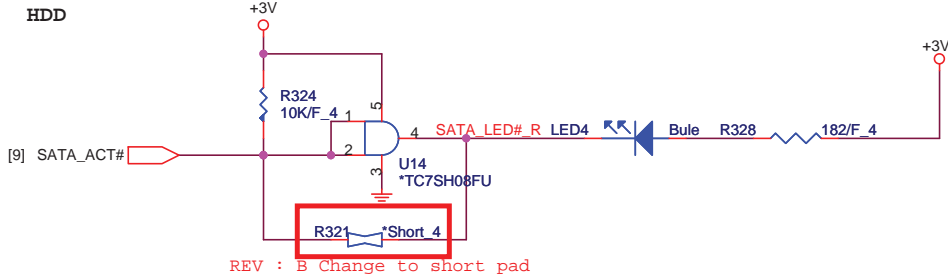
PNT	DFHS11FR011
PLA	DFHS11FR033


**PROJECT : ZQ5**  
**Quanta Computer Inc.**

Size	Document Number <b>AU6433 CardReader</b>	Rev <b>1C</b>
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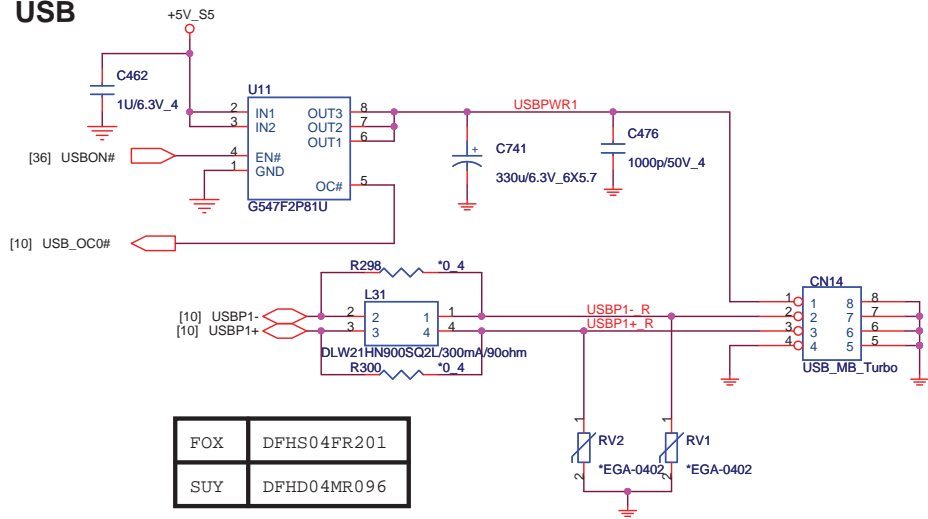


# LED

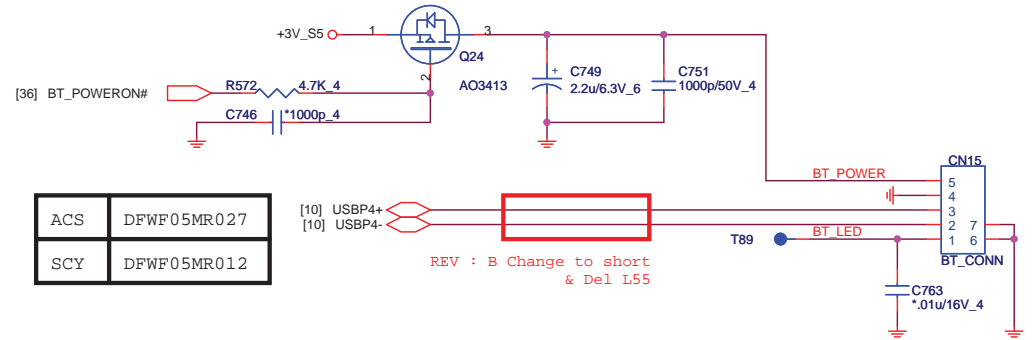


 <b>Quanta Computer Inc.</b> <b>PROJECT : ZRD</b>		Size	Document Number	Rev
				1C
Date: Wednesday, July 21, 2010		Sheet	33	of 46

# USB

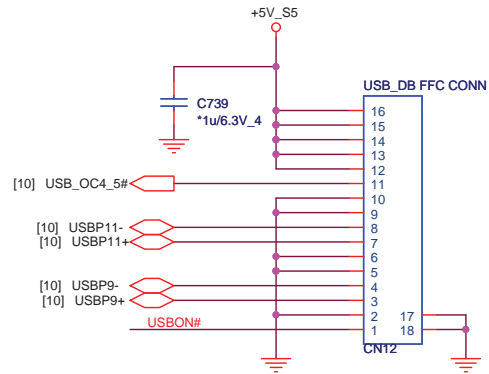



# BLUETOOTH CONNECTOR

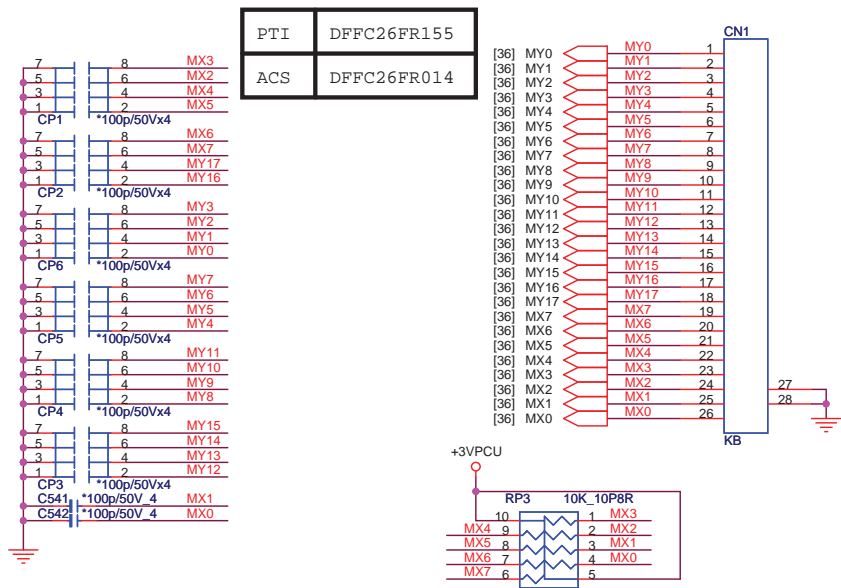


<http://hobi-elektronika.net/>

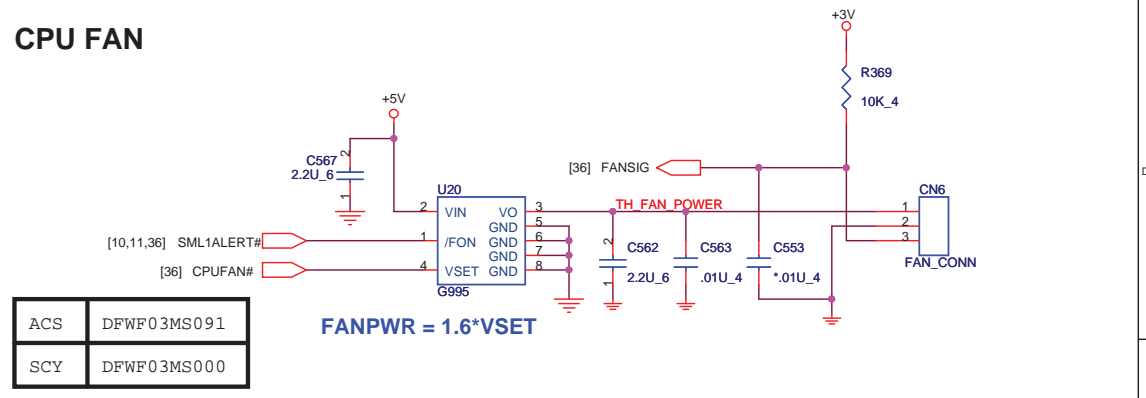
# USB/B



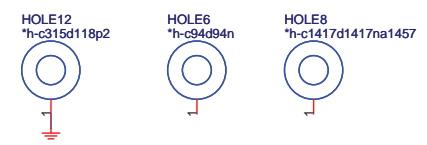
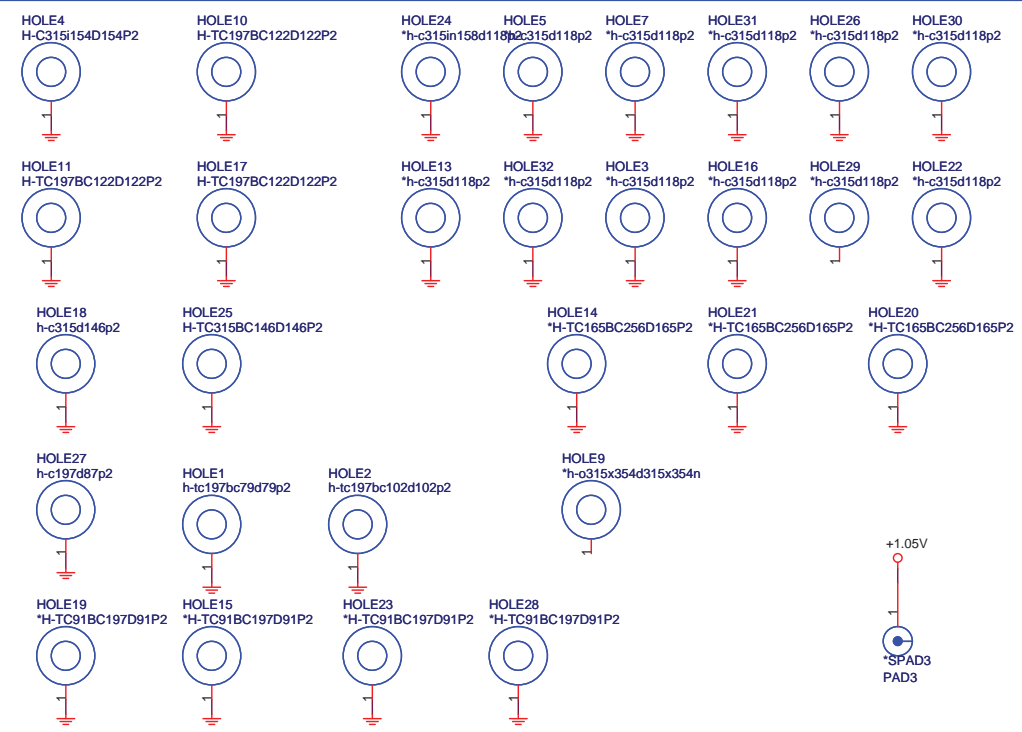
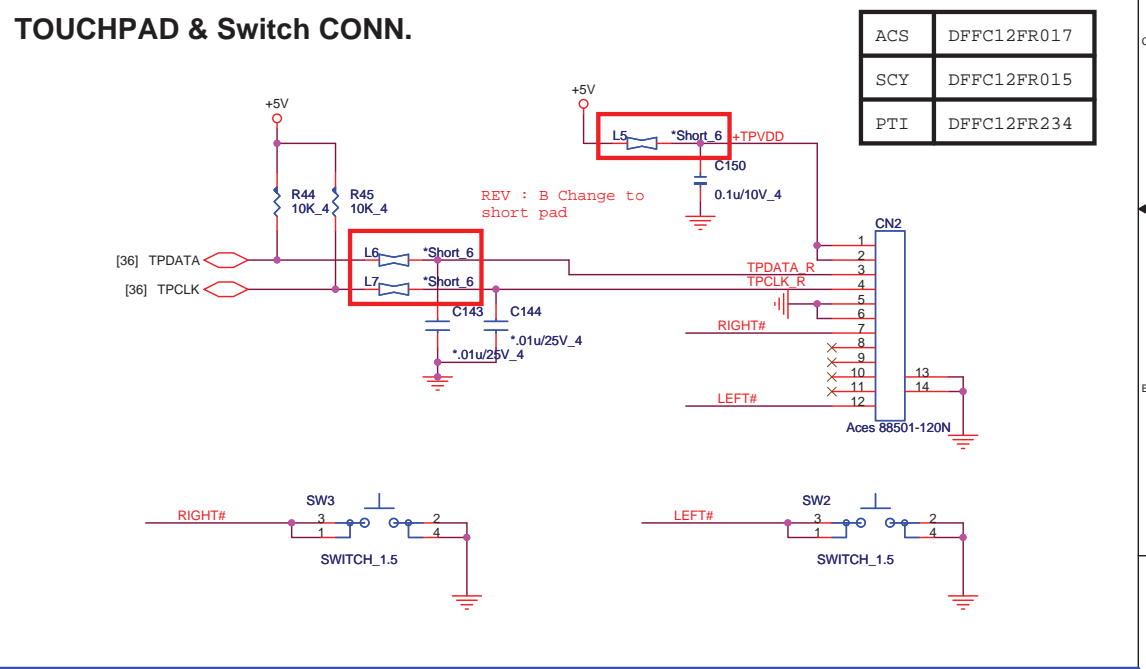
 <b>Quanta Computer Inc.</b> PROJECT : ZRD		Rev
		1C
Size	Document Number	USB/ BT
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CPU FAN



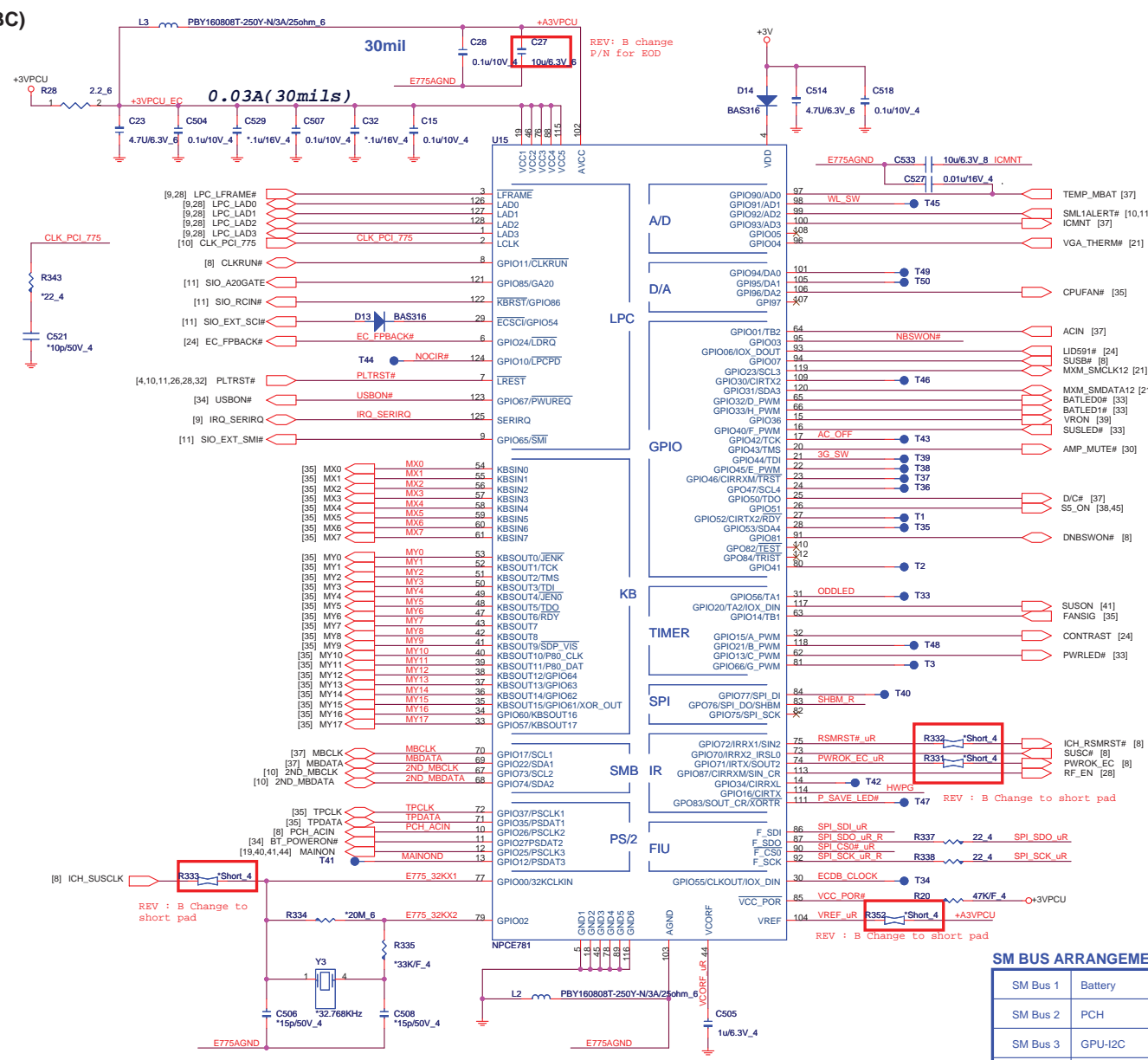
TOUCHPAD & Switch CONN.



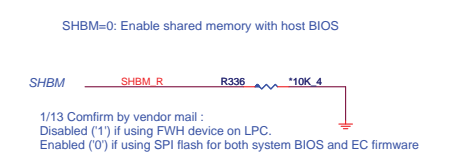
**Quanta Computer Inc.**  
PROJECT : ZRD

Size	Document Number	Rev
	KB/FAN/TP+FP	1C
Date	Wednesday, July 21, 2010	Sheet 35 of 46

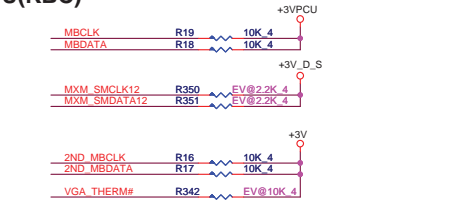
**EC(KBC)**



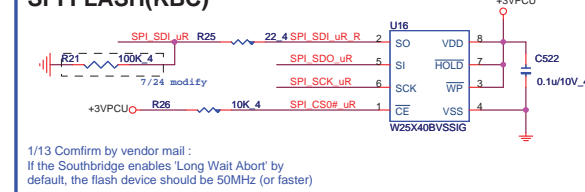
**I/O ADDRESS SETTING(KBC)**



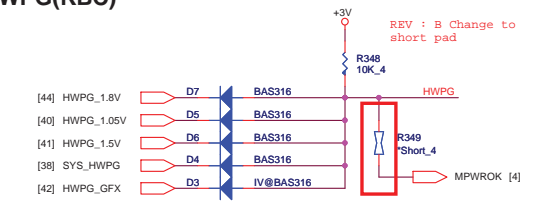
**SM BUS PU(KBC)**



**SPI FLASH(KBC)**



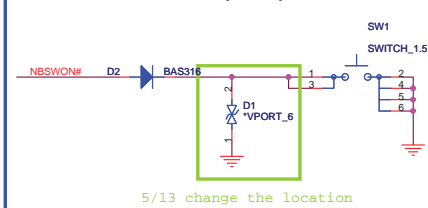
**HWPG(KBC)**



**SM BUS ARRANGEMENT TABLE**

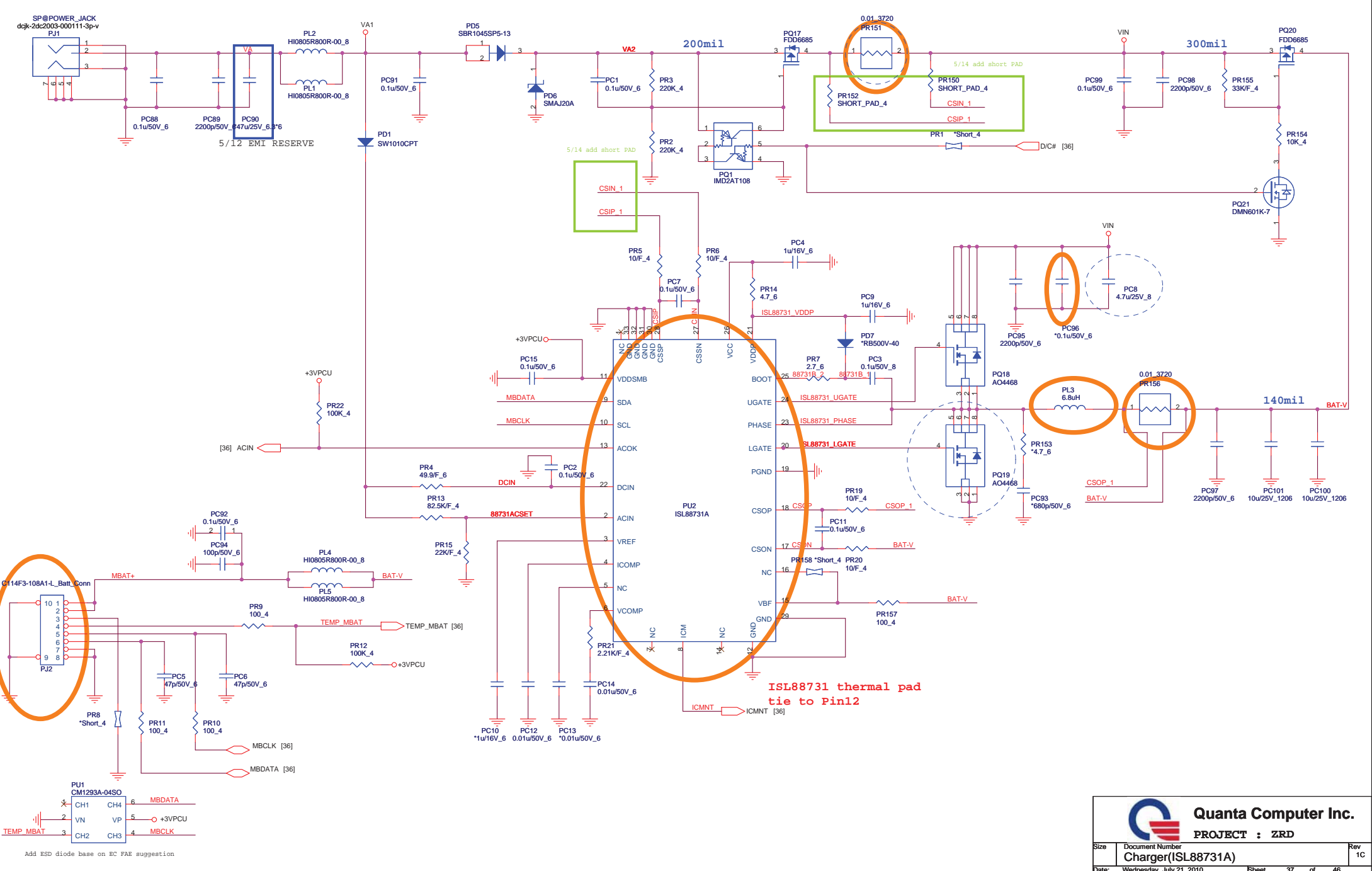
SM Bus 1	Battery
SM Bus 2	PCH
SM Bus 3	GPU-I2C
SM Bus 4	N/A

**POWER-ON Switch(KBC)**




**INTERNAL KEYBOARD STRIP SET(KBC)**

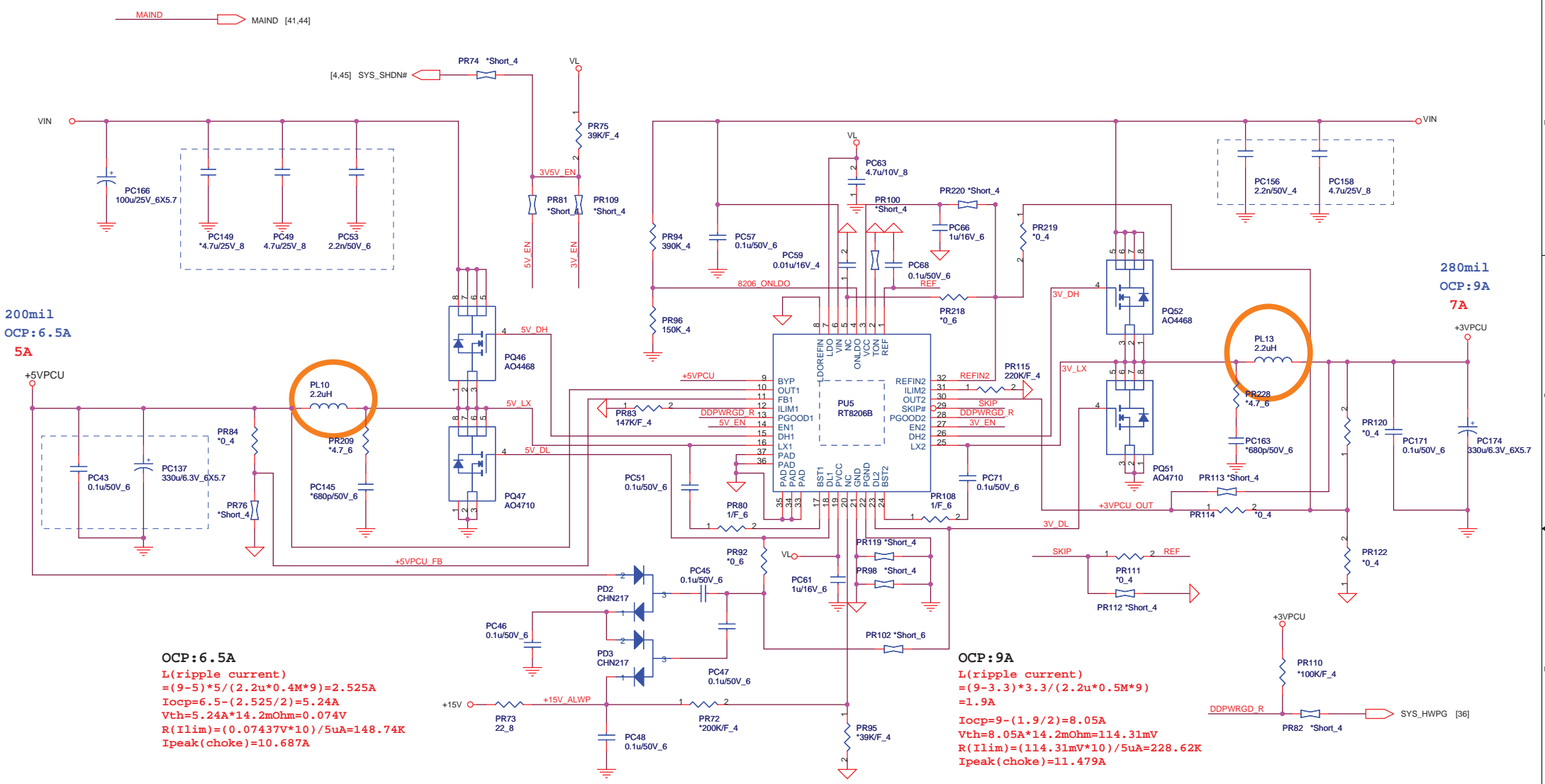




ISL88731 thermal pad tie to Pin12

 <b>Quanta Computer Inc.</b> PROJECT : ZRD		Rev 1C
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Add ESD diode base on EC FAE suggestion

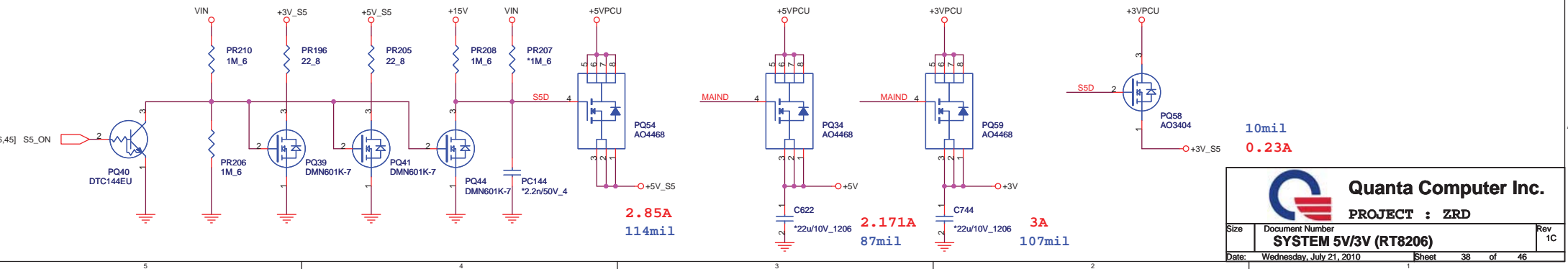


200mil  
OCP: 6.5A  
5A

280mil  
OCP: 9A  
7A

**OCP: 6.5A**  
 $L(\text{ripple current}) = (9-5) * 5 / (2.2u * 0.4M * 9) = 2.525A$   
 $I_{ocp} = 6.5 - (2.525 / 2) = 5.24A$   
 $V_{th} = 5.24A * 14.2m\Omega = 0.074V$   
 $R(I_{lim}) = (0.07437V * 10) / 5uA = 148.74K$   
 $I_{peak}(\text{choke}) = 10.687A$

**OCP: 9A**  
 $L(\text{ripple current}) = (9-3.3) * 3.3 / (2.2u * 0.5M * 9) = 1.9A$   
 $I_{ocp} = 9 - (1.9 / 2) = 8.05A$   
 $V_{th} = 8.05A * 14.2m\Omega = 114.31mV$   
 $R(I_{lim}) = (114.31mV * 10) / 5uA = 228.62K$   
 $I_{peak}(\text{choke}) = 11.479A$



2.85A  
114mil

2.171A  
87mil

3A  
107mil

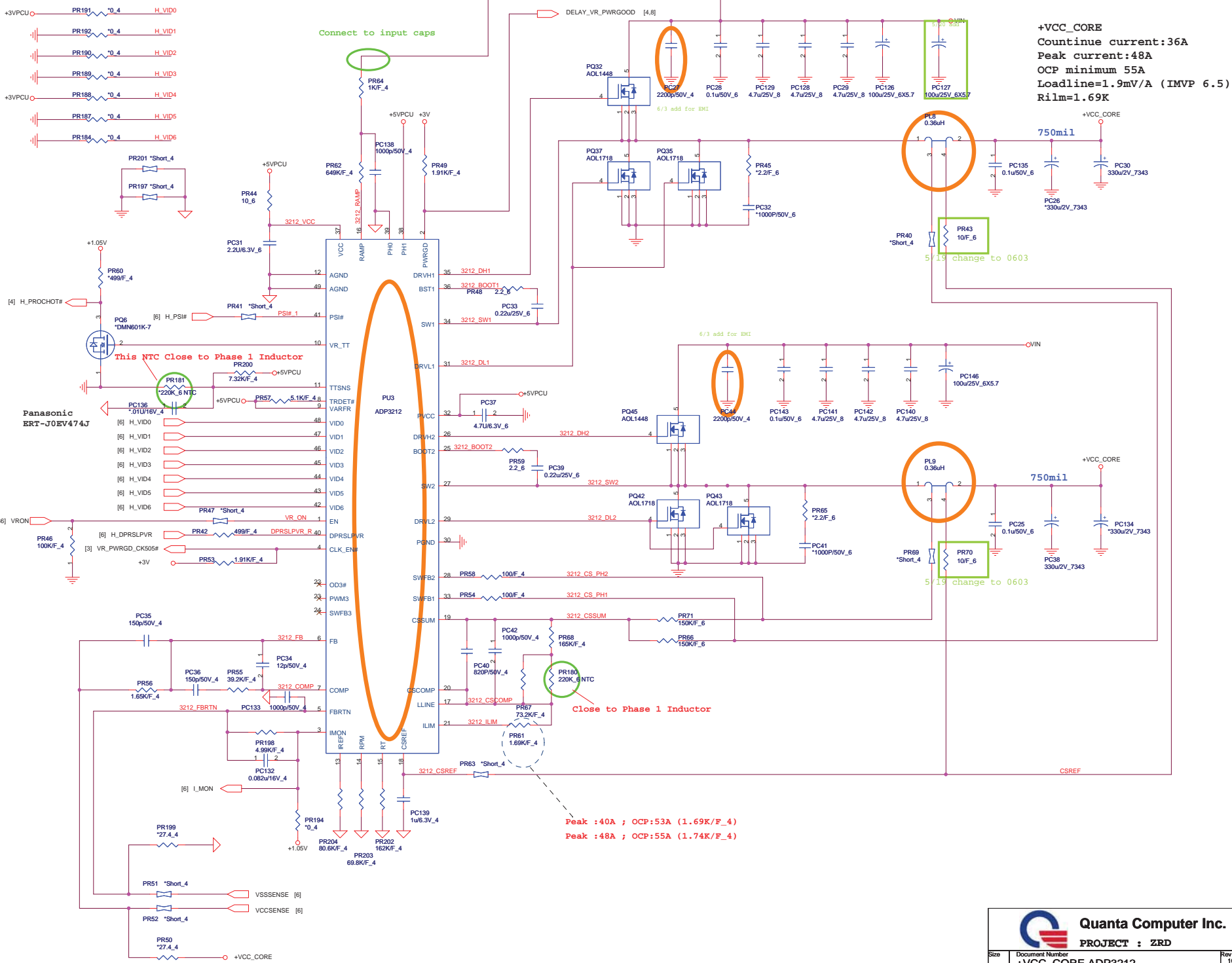
10mil  
0.23A

**Quanta Computer Inc.**  
PROJECT : ZRD

Size	Document Number	Rev
	<b>SYSTEM 5V/3V (RT8206)</b>	1C
Date: Wednesday, July 21, 2010		Sheet 38 of 46



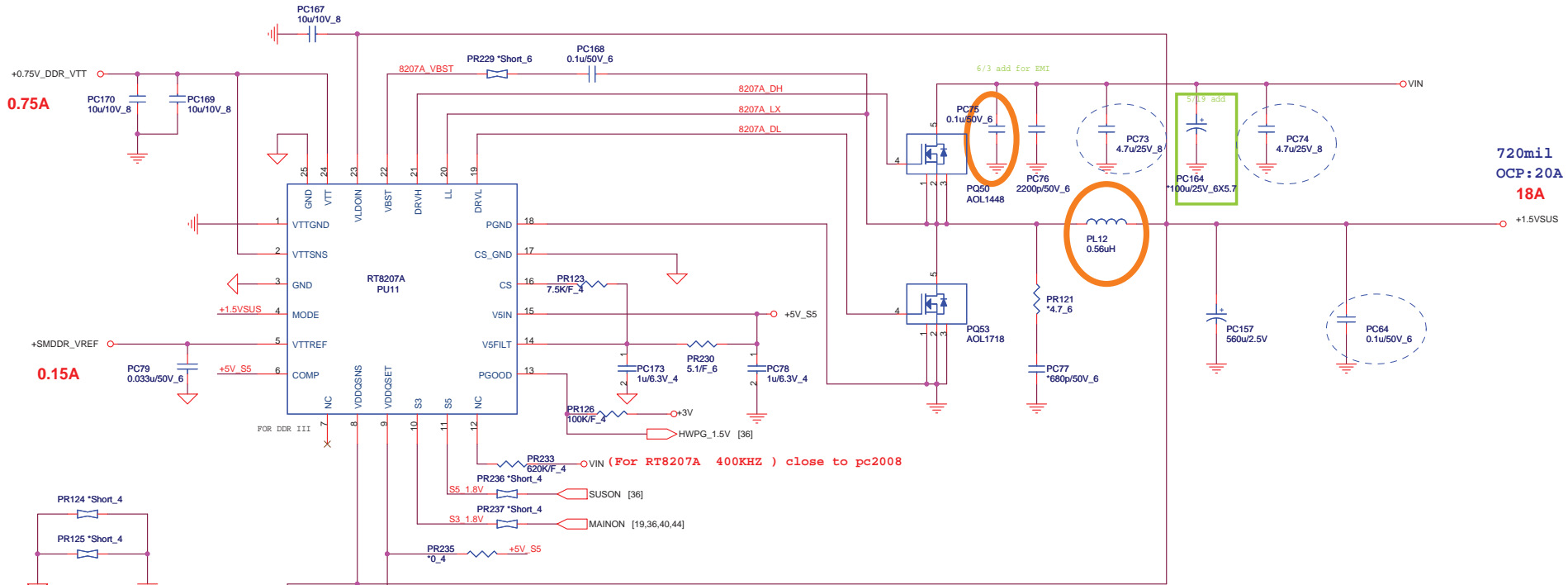
VID 1.2875V



**Quanta Computer Inc.**  
PROJECT : ZRD

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	+VCC_CORE ADP3212	1C
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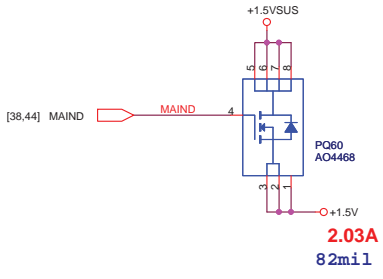




720mil  
 OCP: 20A  
 18A

$$V_{out} = (PR150/PR149) \times 0.75 + 0.75$$

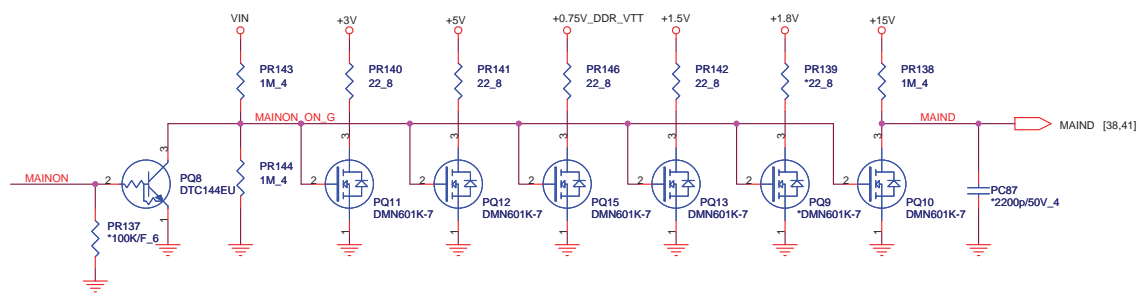
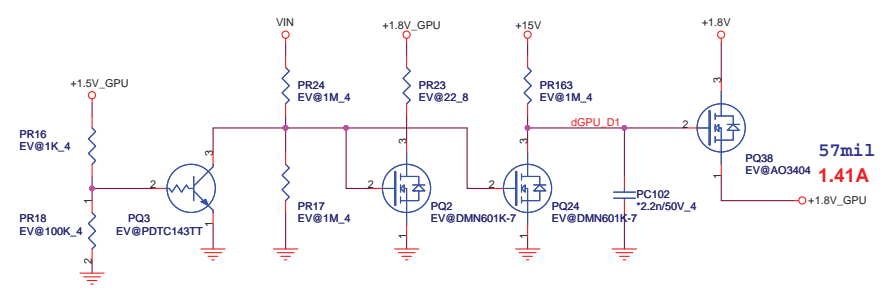
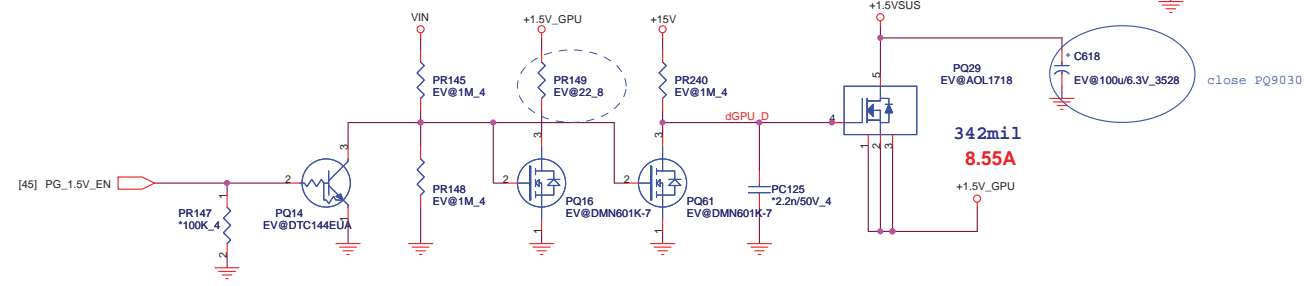
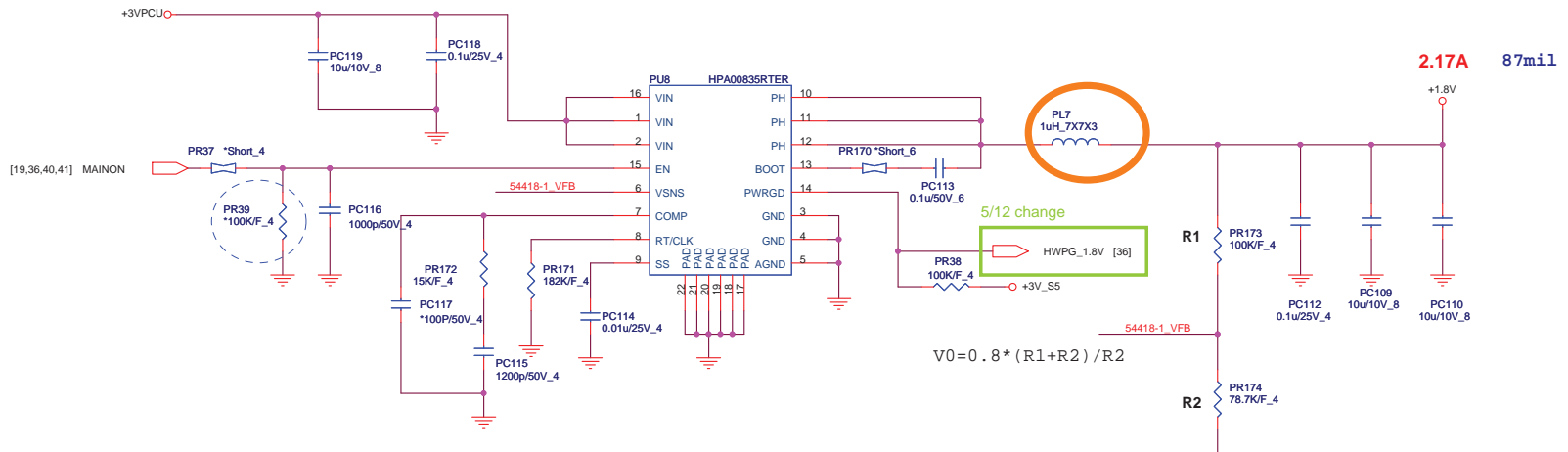
AO1718  $R_{dson} = 3.8 \sim 4.3m\Omega$   
 L(ripple current)  
 $= (19 - 1.5) \times 1.5 / (0.56\mu \times 400k \times 19)$   
 $\sim 6.168A$   
 $V_{trip} = (20 - 6.168 / 2) \times 4.3m\Omega = 0.072739V$   
 $RILIM = V_{trip} / 10\mu = 7.273K$



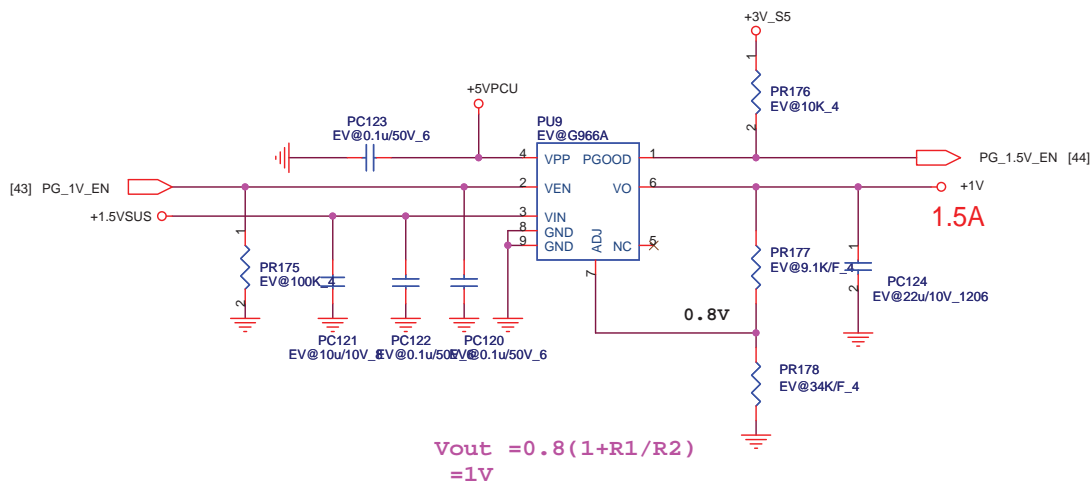
	S3	S5	+1.5VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF



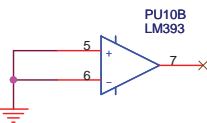
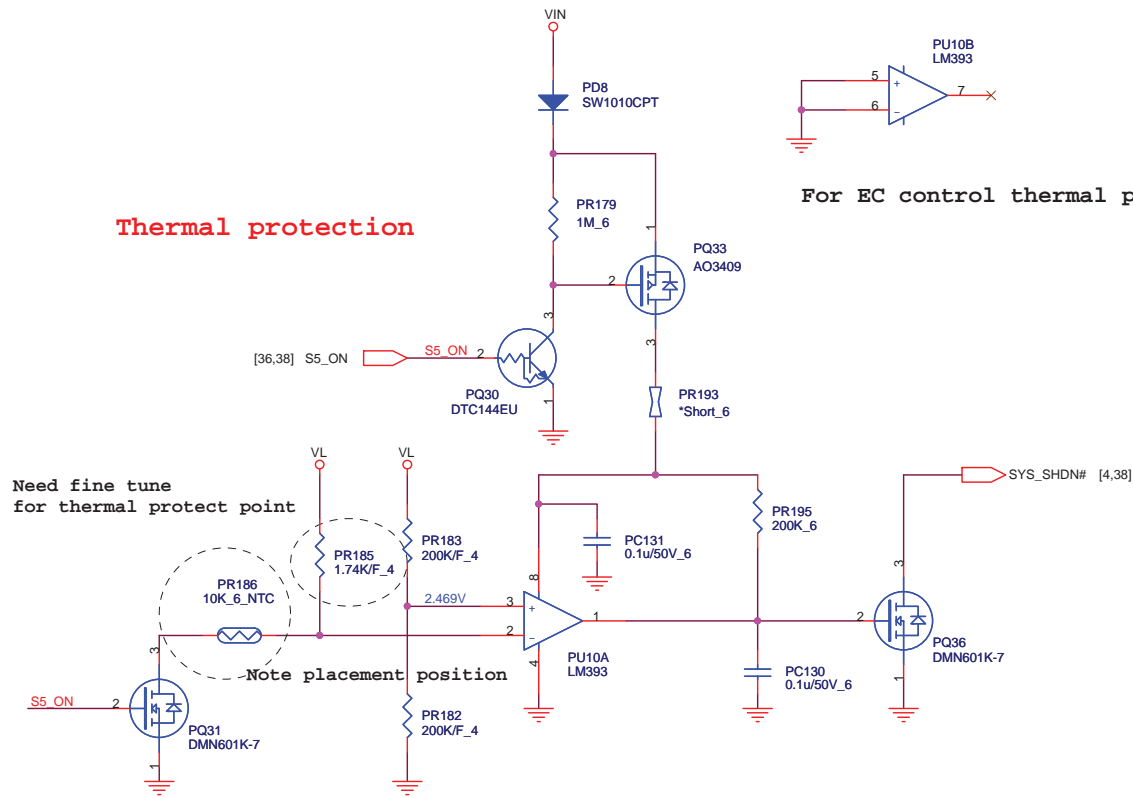








**Thermal protection**



For EC control thermal protection (output 3.3V)

