Columbia/Tangiz Block Diagram

Project code: 91.4T301.001
PCB P/N : 48.4T301.0SA
REVISION : 06236-SA

CLK GEN.
ICS 9LPRS502
(RTM875T-605) 3
71.09502.00W

Mobile CPU
Merom 479
2G/2.33G
2.0G : 71.MEROM.A0U
2.33G : 71.MEROM.B0U
4, 5

G792
20

HOST BUS 667/800MHz@1.05V

DDR2
533/667 MHz
12,13

DDR2
533/667 MHz
12,13

533/667MHz

533/667MHz

Crestline
AGTL+ CPU I/F
DDR Memory I/F
INTEGRATED GRAHPICS
LVDS, CRT I/F
71.CREST.00U
6,7,8,9,10,11

X4 DMI
400MHz

C-Link0

TV Out 14
CRT 15
LCD 14
DVI 44
VGA Borad 28

PCB STACKUP
TOP
VCC
S
S
GND
BOTTOM

Line In
MIC In
14
31
INT.SPKR
Line Out
(No-SPDIF)

Codec
ALC268
30

AZALIA

OP AMP
G1431Q 31

OP AMP
G1412 31

MODEM
MDC Card
22

RJ11

ICH8M
6 PCIe ports
PCI/PCI BRIDGE
ACPI 1.1
3 SATA
1 PATA 66/100
10 USB 2.0/1.1 ports
ETHERNET (10/100/1000MbE)
High Definition Audio
LPC I/F
Serial Peripheral I/F
Matrix Storage Technology(DO)
Active Managemnet Technology(DO)
71.0ICH8.A0U
16,17,18,19

PCI BUS

TI
PCI7412
Cardbus
Cardreader
25/26

PCMCIA I/F

PWR SW
CP2211F 26

PCMCIA
SLOT
Support
TypeII 27

1394
CONN 27

MS/MS Pro/xD/
MMC/SD
5 in 1 27

LAN
GIGA
BCM5787M 23

TXFM 24

RJ45 24

PCIex1

Mini Card
Kedron a/b/g/n 29

LPC BUS

New card 29

PCI Express

P2231NFC1 29

SATA

HDD 21

PATA

CDROM 21

USB

MINI USB
BlueTooth 22

Finger print 34

USB
4 Port 22

CAMERA 13

KBC
Winbond
WPC8768L 32

SPI I/F

BIOS
W25X80-VSS 34

LPC
DEBUG
CONN. 35

Touch
Pad 33

INT.
KB 33

FIR 32

SYSTEM DC/DC MAX8744 38	
INPUTS	OUTPUTS
DCBATOUT	5V_S5(6A) 3D3V_S5(7A)

SYSTEM DC/DC Max8717 39	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0(9.5A) 1D8V_S3(8.5A)

TPS51100 41	
1D8V_S3	DDR_VREF_S0 (1.5A) DDR_VREF_S3

APL5915 41	
1D8V_S3	1D25V_S0 (2A)

APL531230	
3D3V_S0	2D5V_S0 (300mA)

APW5912 40	
3D3V_S5	1D5V_S3 (7.5A)

ISL CHARGER ISL6255 41	
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 4.0A UP+5V 5V 100mA

CPU DC/DC MAX8770 35,36	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 0~1.3V 47A

UMA

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Title: BLOCK DIAGRAM

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ICH8M Functional Strap Definitions

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h)
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#	PCIE config2 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desttop and mobile.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#/ SPI_CS1#	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
INTVRMEN	Integrated VccSus1_05, VccSus1_5 and VccCL1_5 VRM Enable/Disable. Always sampled.	Enables integrated VccSus1_05, VccSus1_5 and VccCL1_5 VRM's when sampled high
LAN100_SLP	Integrated VccLAN1_05 and VccCL1_05 VRM Enable/Disable. Always sampled.	Enables integrated VccLAN1_05 and VccCL1_05 VRM's when sampled high
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH8 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	This signal has a weak internal pull-up. Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be used in manufacturing environments.

ICH8M Integrated Pull-up and Pull-down Resistors

SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 10K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH_[3:0]	PULL-UP 20K
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
CL_RST#	PULL-UP 13K

Crestline Strapping Signals and Configuration

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	001 = FSB533 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 **1 = DMI x4** (Default)
CFG[8:6]	Reserved	
	Low Power PCI Express	0 = Normal mode **1 = Low Power mode** (Default)
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes,15->0,14->1 ect.. **1= Normal operation(Default):Lane Numbered in order**
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled **11 = Normal Operation** (Default)
CFG[15:14]	Reserved	Reserved
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG[18:17]	Reserved	
CFG19	DMI Lane Reversal	**0 = Normal operation (Default):lane Numbered in order** 1 =Reverse Lane,4->0,3->1 ect...
CFG20	SDVO/PCIE Concurrent	**0 = Only SDVO or PCIE x1 is operational (Default)** 1 =SDVO and PCIE x1 are operating simultaneously via the PEG port
SDVOCRTL _DATA	SDVO Present	**0 = No SDVO Card present** (Default) 1= SDVO Card present

NOTE: All strap signals are sampled with respect to the leading edge of the Crestline GMCH PWORK in signal.

History

ICH8M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm

PCI Routing

page 17

	IDSEL	INT	REQ	GNT
TI7412	AD22	G:CARDBUS B:1394 F:Flash Media G:SD Host	0	0

PCIE Routing

LANE1	LAN BCM5787M
LANE2	MiniCard WLAN
LANE3	NewCard WLAN

USB Table

USB	
Pair	Device
0	USB1
1	NC
2	USB2
3	FT
4	USB3
5	BLUETOOTH
6	WEBCAM
7	USB4
8	MINICARD
9	NEW1

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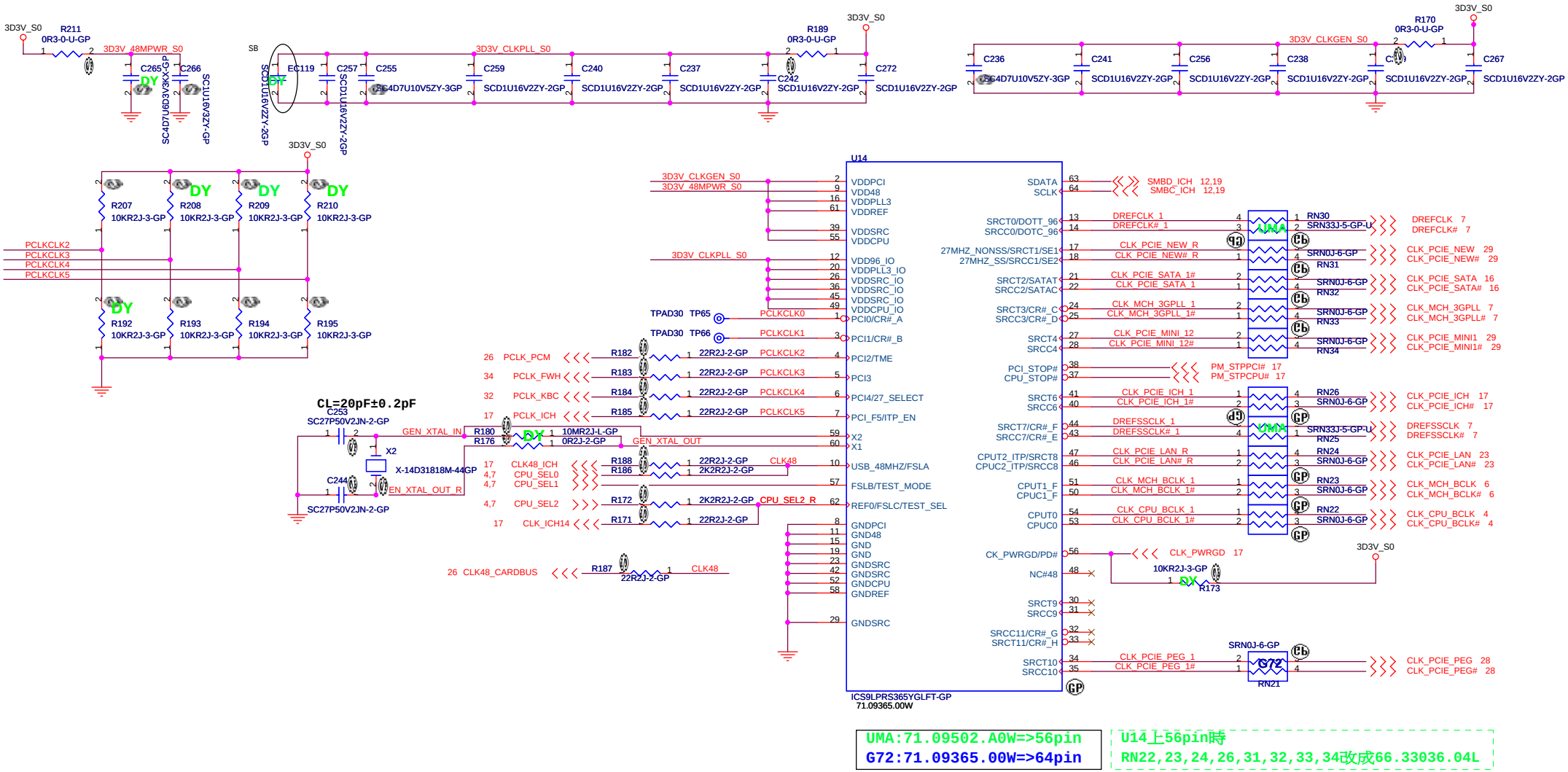

ICS9LPR502HGLFT-GP setting table

PIN NAME	DESCRIPTION
PCI0/CR#_A	Byte 5, bit 7 0 = PCI0 enabled (default) 1= CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1= CR#_A controls SRC2 pair
PCI1/CR#_B	Byte 5, bit 5 0 = PCI1 enabled (default) 1= CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR#_B controls SRC1 pair (default) 1= CR#_B controls SRC4 pair
PCI2/TME	0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed
PCI4/SRC5_EN	0 = Pin29 as CPU_STOP# , pin 30 as PCI_STOP#. 1 = Pins29,30 as SRC-5 differential pair.
PCI_F5/ITP_EN	0 =SRC8/SRC8# 1 = ITP/ITP#

RTM875T-605 setting table

PIN NAME	DESCRIPTION
PCI0/CR#_A	Byte 5, bit 7 0 = PCI0 enabled (default) 1= CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1= CR#_A controls SRC2 pair
PCI1/CR#_B	Byte 5, bit 5 0 = PCI1 enabled (default) 1= CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR#_B controls SRC1 pair (default) 1= CR#_B controls SRC4 pair
PCI2/TME	0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed
PCI3/SRC-5_EN	0 = Pin29 as CPU_STOP# , pin 30 as PCI_STOP#. 1 = Pins29,30 as SRC-5 differential pair.
PCI4/27M_SEL	0 = Pin17 as SRC-1, Pin18 as SRC-1#, Pin13 as DOT96, Pin14 as DOT96# 1 = Pin17 as 27MHz, Pin 18 as 27MHz_SS, Pin13 as SRC-0, Pin14 as SRC-0#
PCI_F5/ITP_EN	0 =SRC8/SRC8# 1 = ITP/ITP#

SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	X
0	1	1	166M	667M
0	1	0	200M	800M

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Title: Clock Generator

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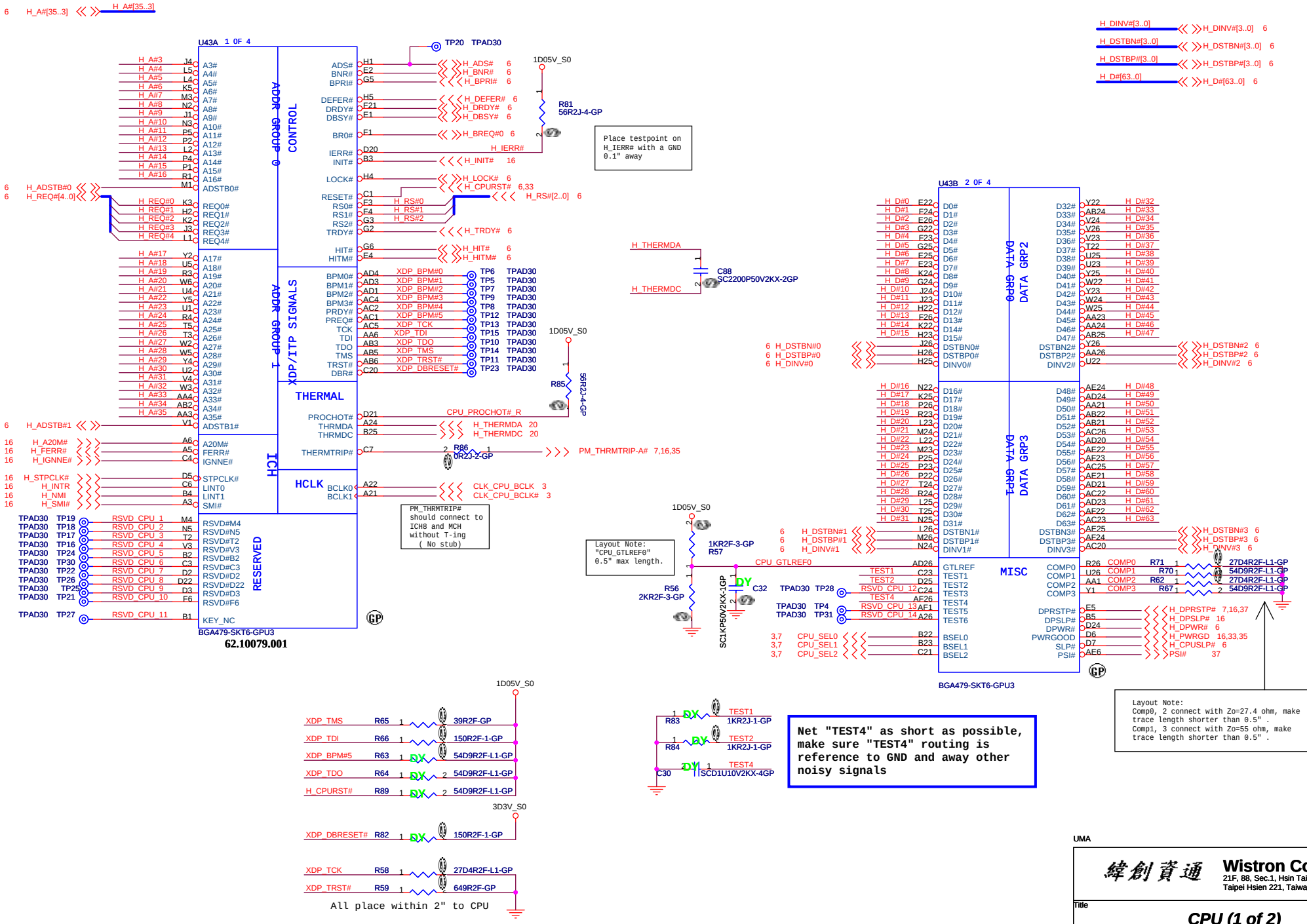
U43A 1 OF 4
ADDR GROUP 0
CONTROL
ADDR GROUP 1
XDP/ITP SIGNALS
THERMAL
HCLK
ICH
RESERVED
BGA479-SKT6-GPU3
62.10079.001
U43B 2 OF 4
DATA GRP2
DATA GRP0
DATA GRP1
DATA GRP3
MISC
BGA479-SKT6-GPU3
Place testpoint on H_IERR# with a GND 0.1" away
PM_THRMTRIP# should connect to ICH8 and MCH without T-ing (No stub)
Layout Note: "CPU_GTLREF0" 0.5" max length.
Net "TEST4" as short as possible, make sure "TEST4" routing is reference to GND and away other noisy signals
All place within 2" to CPU
Layout Note: Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5" . Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5" .
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CPU (1 of 2)
Columbia/Tangiz
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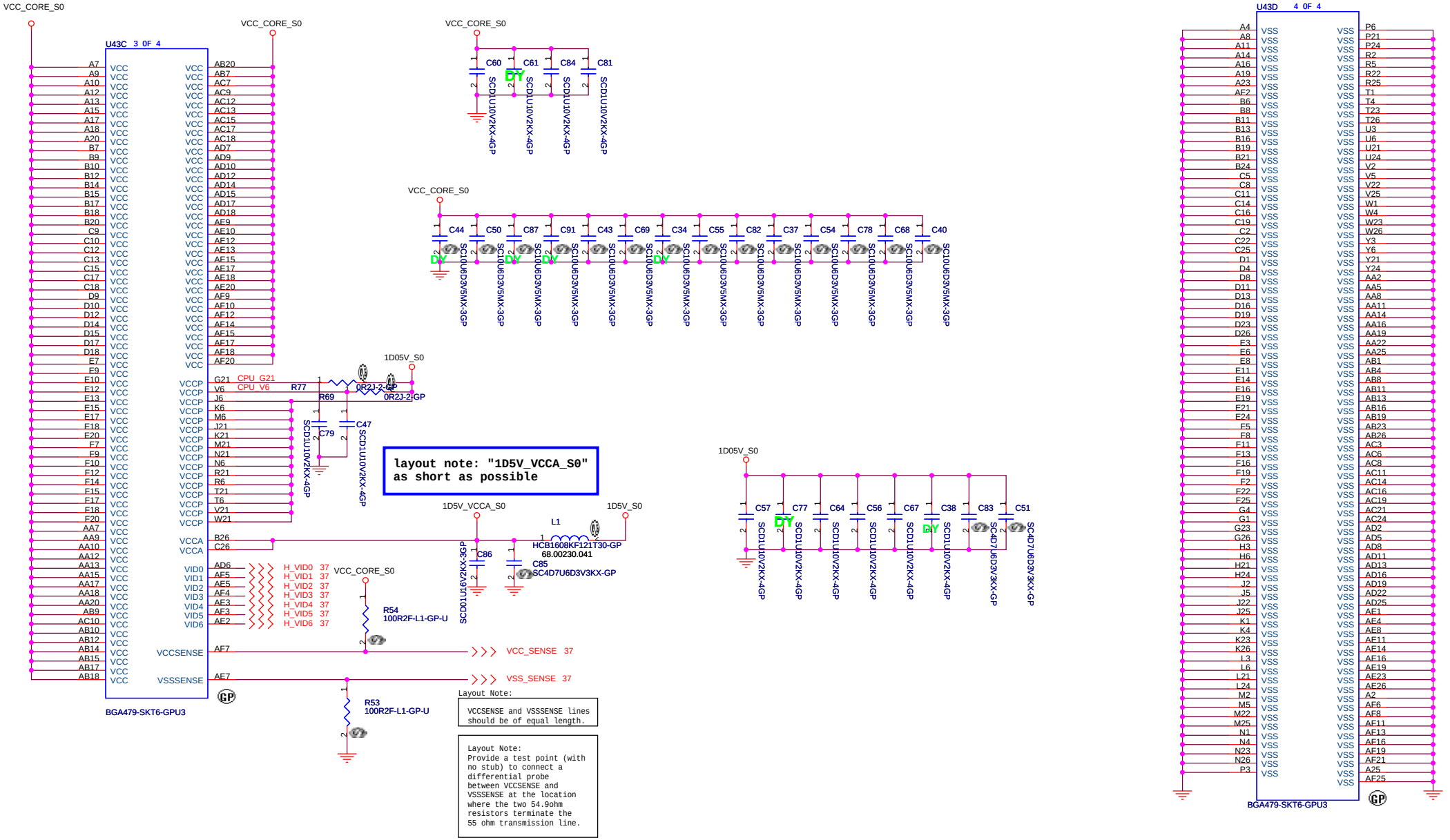

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Title	***CPU (2 of 2)***	
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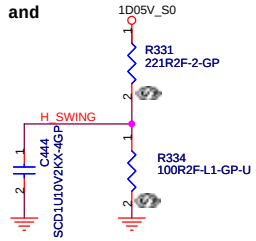
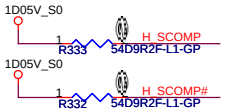
H_SWING routing Trace width and Spacing use 10 / 20 mil

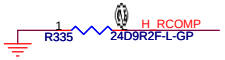
H_SWING Resistors and Capacitors close MCH 500 mil (MAX)



H_SCOMP and H_SCOMP# Resistors and Capacitors close MCH 500 mil (MAX)

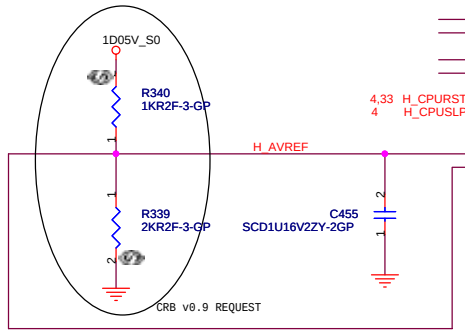


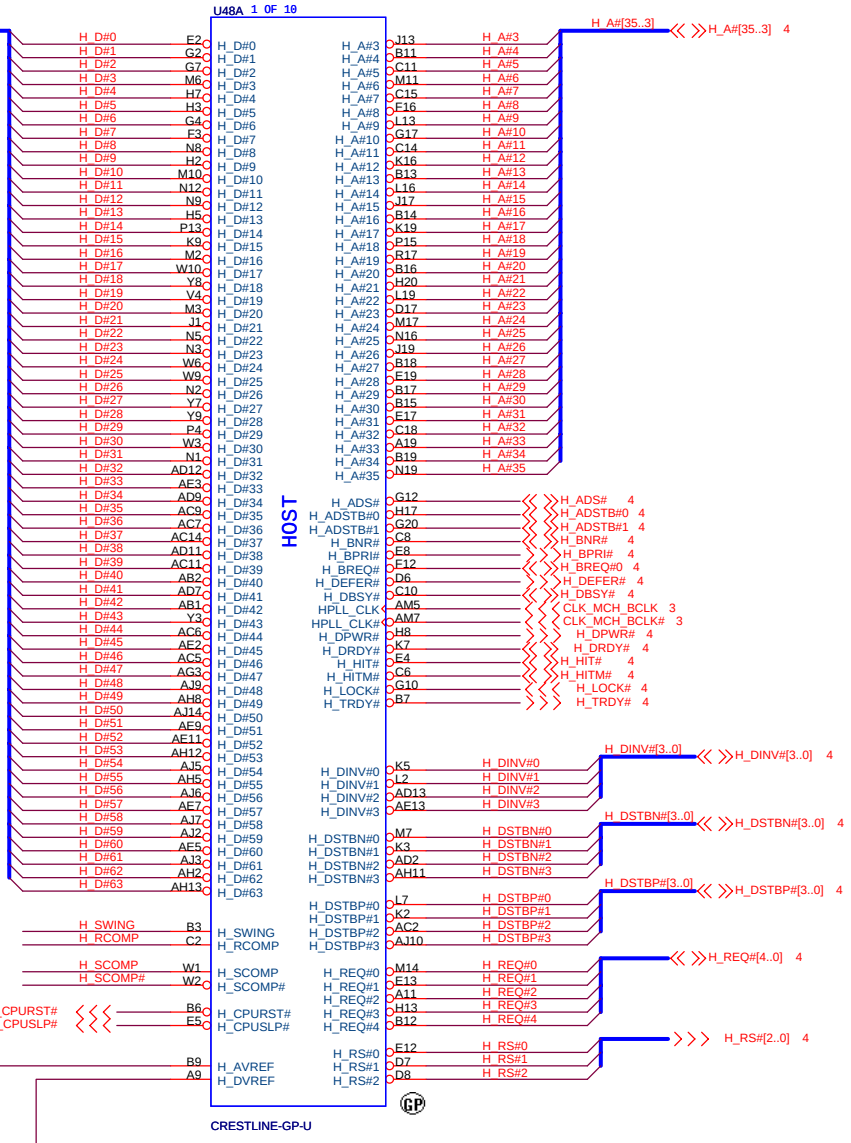
H_RCOMP routing Trace width and Spacing use 10 / 20 mil



Place them near to the chip (< 0.5")

H_REF Decoupling Crestline close Crestline 100 mil





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RSVD
RSVD#P36
RSVD#P37
RSVD#R35
RSVD#N35
RSVD#AR12
RSVD#AR13
RSVD#AM12
RSVD#AN13
RSVD#J12
RSVD#AR37
RSVD#AM36
RSVD#AL36
RSVD#AM37
RSVD#D20
RSVD#H10
RSVD#B51
RSVD#BJ20
RSVD#BK22
RSVD#BF19
RSVD#BH20
RSVD#BK18
RSVD#BJ18
RSVD#BF23
RSVD#BG23
RSVD#BC23
RSVD#BD24
RSVD#BH39
RSVD#AW20
RSVD#BK20
RSVD#B44
RSVD#C44
RSVD#A35
RSVD#B37
RSVD#B36
RSVD#B34
RSVD#C34

DDR MUXING
SM_CK0 SM_CK1 SM_CK2 SM_CK3
SM_CK#0 SM_CK#1 SM_CK#2 SM_CK#3
SM_CKE0 SM_CKE1 SM_CKE2 SM_CKE3
SM_CS#0 SM_CS#1 SM_CS#2 SM_CS#3
SM_ODT0 SM_ODT1 SM_ODT2 SM_ODT3
SM_RCOMP_VOH SM_RCOMP_VOL SM_RCOMP SM_RCOMP#
SM_VREF#AR49 SM_VREF#AW4
M_CLK_DDR0 M_CLK_DDR1 M_CLK_DDR2 M_CLK_DDR3
M_CLK_DDR#0 M_CLK_DDR#1 M_CLK_DDR#2 M_CLK_DDR#3
M_CKE0 M_CKE1 M_CKE2 M_CKE3
M_CS0# M_CS1# M_CS2# M_CS3#
M_ODT0 M_ODT1 M_ODT2 M_ODT3
SM_RCOMP_VOH SM_RCOMP_VOL
M_RCOMPP M_RCOMPN
DDR_VREF_S3

CLK
DPLL_REF_CLK DPLL_REF_CLK# DPLL_REF_SSCLK DPLL_REF_SSCLK#
DREFCLK DREFCLK# DREFSSCLK DREFSSCLK#
PEG_CLK PEG_CLK#
CLK_MCH_3GPLL CLK_MCH_3GPLL#

DMI
DMI_RXN0 DMI_RXN1 DMI_RXN2 DMI_RXN3
DMI_RXP0 DMI_RXP1 DMI_RXP2 DMI_RXP3
DMI_TXN0 DMI_TXN1 DMI_TXN2 DMI_TXN3
DMI_TXP0 DMI_TXP1 DMI_TXP2 DMI_TXP3

CFG
CFG0 CFG1 CFG2 CFG3 CFG4 CFG5 CFG6 CFG7 CFG8 CFG9 CFG10 CFG11 CFG12 CFG13 CFG14 CFG15 CFG16 CFG17 CFG18 CFG19 CFG20
CPU_SEL0 CPU_SEL1 CPU_SEL2

GRAPHICS VID
GFX_VID0 GFX_VID1 GFX_VID2 GFX_VID3 GFX_VR_EN
TP48 TP51 TP116 TP49 TP50
TPAD28

PM
PM_BM_BUSY# PM_DPRSTP# PM_EXT_TS#0 PM_EXT_TS#1 PWROK RSTIN# THERMTRIP# DPRSLPVR
H_DPRSTP_MCH PM_EXTTS#0 PM_EXTTS#1 RSTIN# NB_THERMTRIP# PM_DPRSLPVR

ME
CL_CLK CL_DATA CL_PWROK CL_RST# CL_VREF
CL_CLK0 CL_DATA0 CL_RST#0
CLPWROK_MCH MCH_CLVREF

MISC
SDVO_CTRL_CLK SDVO_CTRL_DATA CLKREQ# ICH_SYNC#
CLK_3GPLLREQ# MCH_ICH_SYNC#
TEST1 TEST2 TEST2_GMCH

NC
NC#BJ51 NC#BK51 NC#BK50 NC#BL50 NC#BL49 NC#BL3 NC#BL2 NC#BK1 NC#BJ1 NC#E1 NC#A5 NC#C51 NC#B50 NC#A50 NC#A49 NC#BK2

CRESTLINE-GP-U

UMA
U48C 3 OF 10

LVDS
L_BKLT_CTRL L_BKLT_EN L_CTRL_CLK L_CTRL_DATA L_DDC_CLK L_DDC_DATA L_VDD_EN
LVDS_IBG LVDS_VBG LVDS_VREFH LVDS_VREFL
LVDSA_CLK# LVDSA_CLK
LVDSA_DATA#0 LVDSA_DATA#1 LVDSA_DATA#2 LVDSA_DATA#3
LVDSA_DATA0 LVDSA_DATA1 LVDSA_DATA2 LVDSA_DATA3
LVDSB_DATA#0 LVDSB_DATA#1 LVDSB_DATA#2
LVDSB_DATA0 LVDSB_DATA1 LVDSB_DATA2
LVDSB_CLK# LVDSB_CLK

TV
TVA_DAC TVB_DAC TVC_DAC
TVA_RTN TVB_RTN TVC_RTN
TV_DCONSEL0 TV_DCONSEL1

VGA
CRT_BLUE CRT_BLUE# CRT_GREEN CRT_GREEN# CRT_RED CRT_RED#
CRT_DDC_CLK CRT_DDC_DATA CRT_VSYNC CRT_TVO_IREF CRT_HSYNC

PCI_EXPRESS GRAPHICS
PEG_COMPI PEG_COMPO
PEG_RX#0 PEG_RX#1 PEG_RX#2 PEG_RX#3 PEG_RX#4 PEG_RX#5 PEG_RX#6 PEG_RX#7 PEG_RX#8 PEG_RX#9 PEG_RX#10 PEG_RX#11 PEG_RX#12 PEG_RX#13 PEG_RX#14 PEG_RX#15
PEG_RXN0 PEG_RXN1 PEG_RXN2 PEG_RXN3 PEG_RXN4 PEG_RXN5 PEG_RXN6 PEG_RXN7 PEG_RXN8 PEG_RXN9 PEG_RXN10 PEG_RXN11 PEG_RXN12 PEG_RXN13 PEG_RXN14 PEG_RXN15
PEG_RXN[15..0] 28
PEG_RX0 PEG_RX1 PEG_RX2 PEG_RX3 PEG_RX4 PEG_RX5 PEG_RX6 PEG_RX7 PEG_RX8 PEG_RX9 PEG_RX10 PEG_RX11 PEG_RX12 PEG_RX13 PEG_RX14 PEG_RX15
PEG_RXP0 PEG_RXP1 PEG_RXP2 PEG_RXP3 PEG_RXP4 PEG_RXP5 PEG_RXP6 PEG_RXP7 PEG_RXP8 PEG_RXP9 PEG_RXP10 PEG_RXP11 PEG_RXP12 PEG_RXP13 PEG_RXP14 PEG_RXP15
PEG_RXP[15..0] 28
PEG_TX#0 PEG_TX#1 PEG_TX#2 PEG_TX#3 PEG_TX#4 PEG_TX#5 PEG_TX#6 PEG_TX#7 PEG_TX#8 PEG_TX#9 PEG_TX#10 PEG_TX#11 PEG_TX#12 PEG_TX#13 PEG_TX#14 PEG_TX#15
GTXN0 GTXN1 GTXN2 GTXN3 GTXN4 GTXN5 GTXN6 GTXN7 GTXN8 GTXN9 GTXN10 GTXN11 GTXN12 GTXN13 GTXN14 GTXN15
PEG_TXN[15..0] 28
PEG_TX0 PEG_TX1 PEG_TX2 PEG_TX3 PEG_TX4 PEG_TX5 PEG_TX6 PEG_TX7 PEG_TX8 PEG_TX9 PEG_TX10 PEG_TX11 PEG_TX12 PEG_TX13 PEG_TX14 PEG_TX15
GTXP0 GTXP1 GTXP2 GTXP3 GTXP4 GTXP5 GTXP6 GTXP7 GTXP8 GTXP9 GTXP10 GTXP11 GTXP12 GTXP13 GTXP14 GTXP15
PEG_TXP[15..0] 28

CRESTLINE-GP-U

For Calero: 255 ohm
Crestline: 1.3k ohm
CRT_IREF routing Trace width use 20 mil

For Discrete change R137, R139 & R142 to 0 ohm

SB

G72

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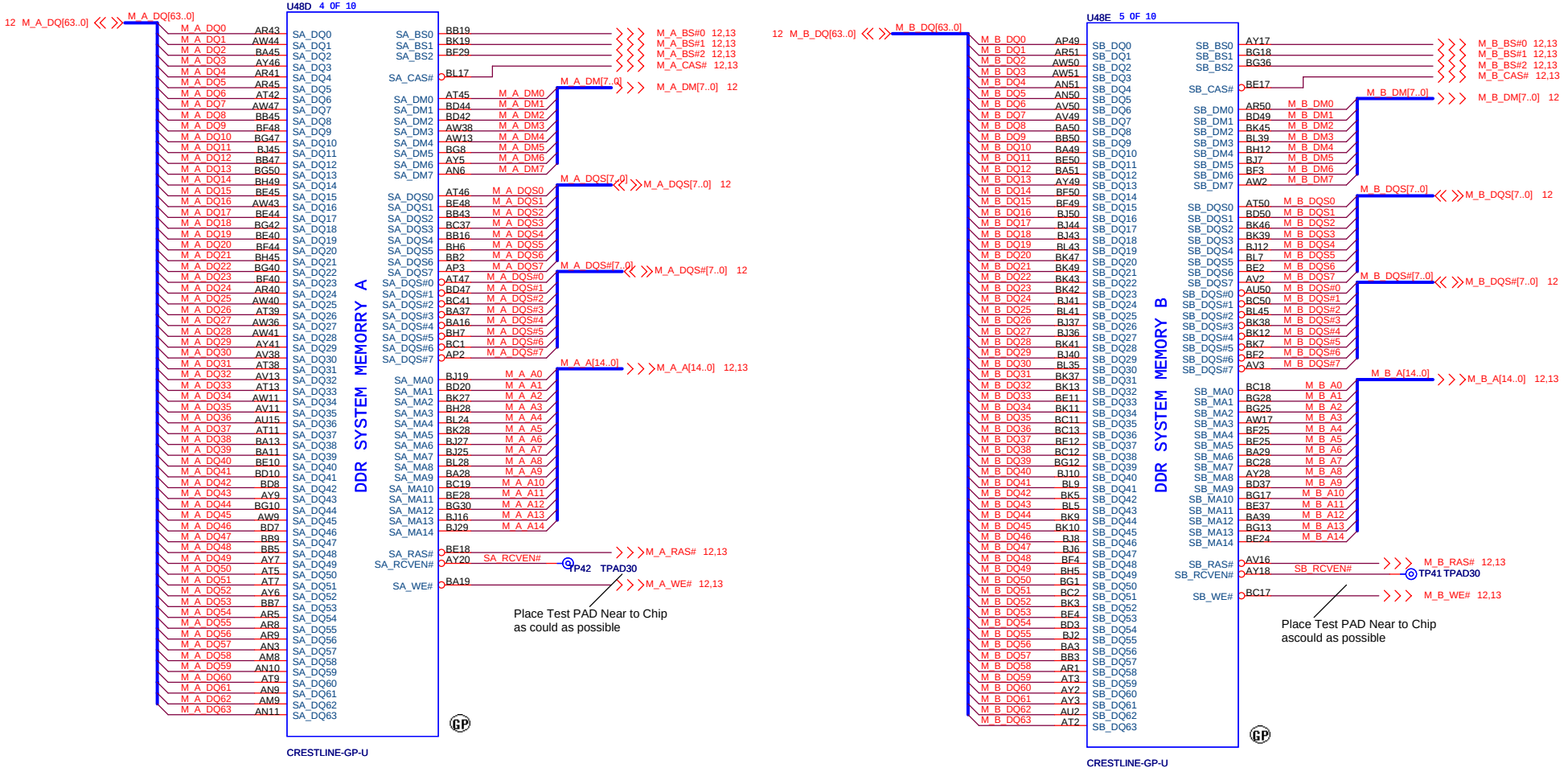

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VCC_NCTF + VCC=1573mA

1573mA

U48F 6 OF 10

VCC CORE

POWER

R143 0R2J-2-GP

3138mA

VCC SM

VCC GFX NCTF

VCC GFX

VCC SM LF

CRESTLINE-GP-U

SB:Remove R123,R132,R136,R144

VCC_AXG_NCTF + VCC_AXG=7700mA

UMA

SB:DIS remove 0 ohm on C129,C210,C158,C161

FOR VCC CORE AND VCC NCTF

308 mils from the Edge

Coupling CAP

FOR VCC CORE

Coupling CAP 370 mils from the Edge

U48G 7 OF 10

VCC NCTF

VSS NCTF

VSS SCB

VSS AXM

VSS AXM NCTF

FOR VCC AXM NCTF AND VCC AXM

Place on the Edge

VCC_AXM_NCTF + VCC_AXM=540mA

Place CAP where LVDS and DDR2 taps

FOR VCC SM

Place on the Edge

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Title: GMCH (4 of 6)

Size: | Document Number: Columbia/Tangiz | Rev: SA

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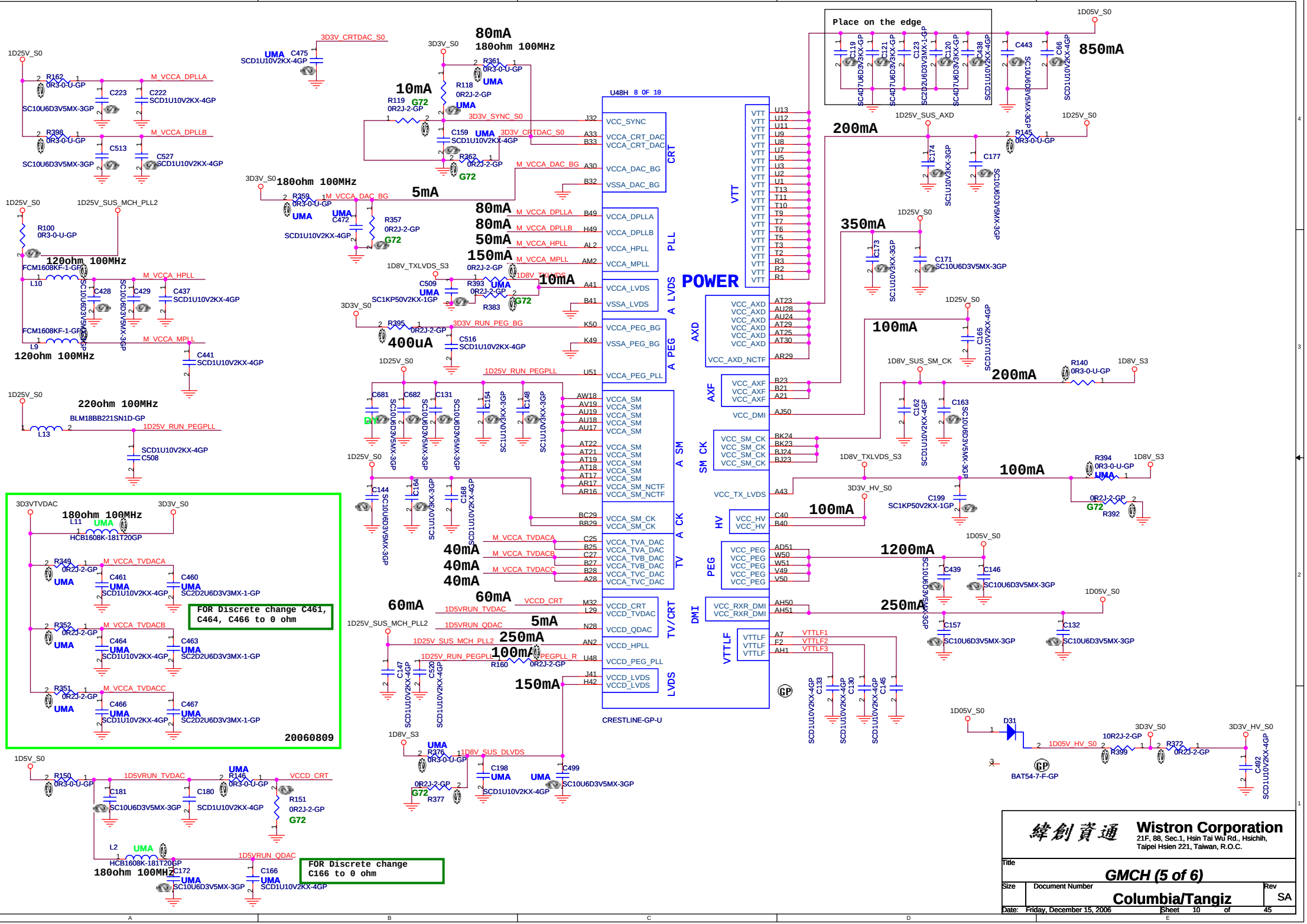
POWER
U48H 8 OF 10
CRESTLINE-GP-U
CRT
PLL
A LVDS
A PEG
A SM
A CK
TV
TV/CRT
LVDS
VTT
AXD
AXF
SM CK
HV
PEG
DMI
VTTLF
Place on the edge
180ohm 100MHz
220ohm 100MHz
120ohm 100MHz
FOR Discrete change C461, C464, C466 to 0 ohm
FOR Discrete change C166 to 0 ohm
20060809
850mA
200mA
350mA
100mA
1200mA
250mA
80mA
10mA
5mA
400uA
50mA
150mA
40mA
60mA
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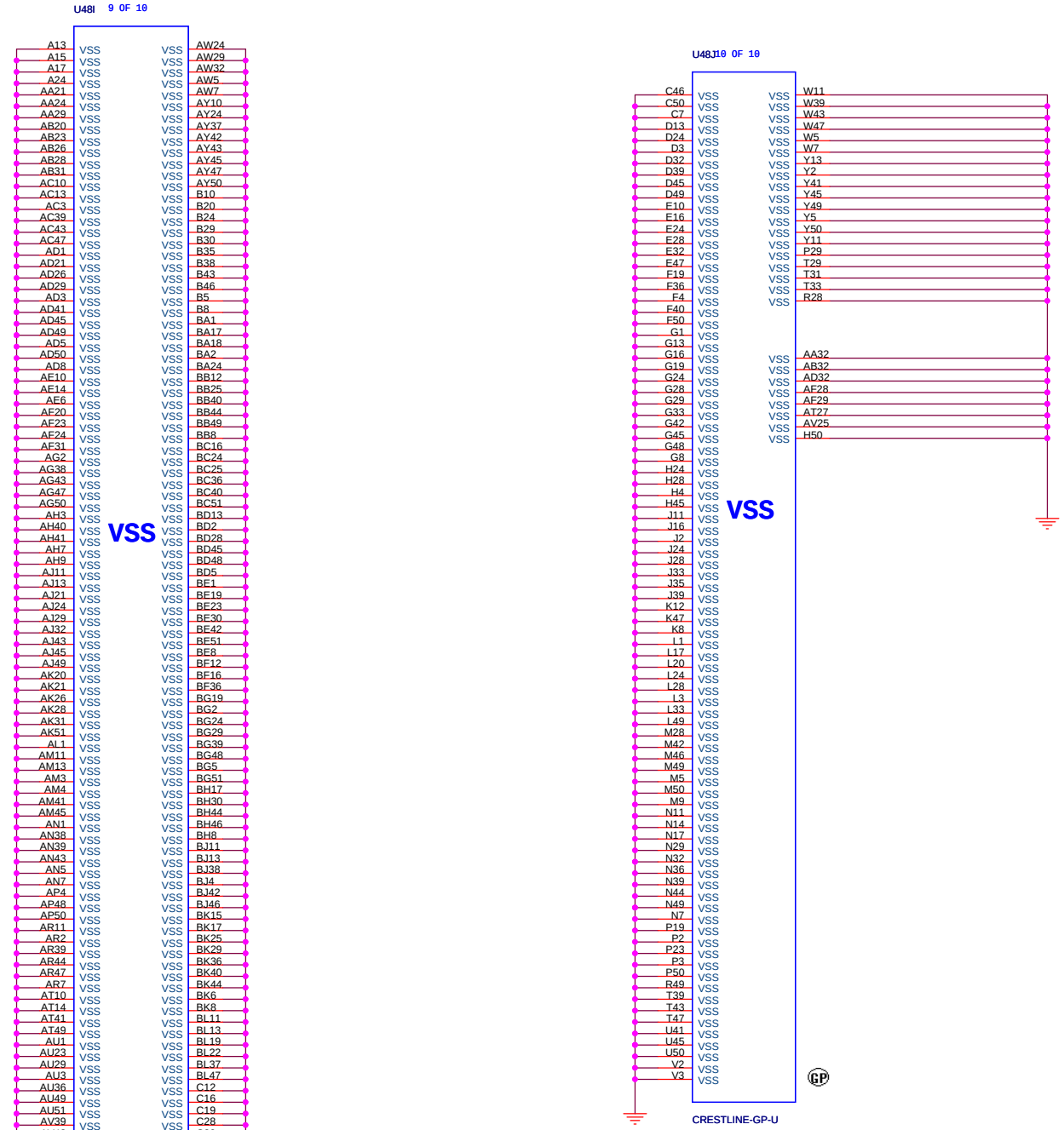
GMCH (5 of 6)
Columbia/Tangiz
Friday, December 15, 2006



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Title: ***GMCH (6 of 6)***

Size	Document Number	Rev
	Columbia/Tangiz	SA

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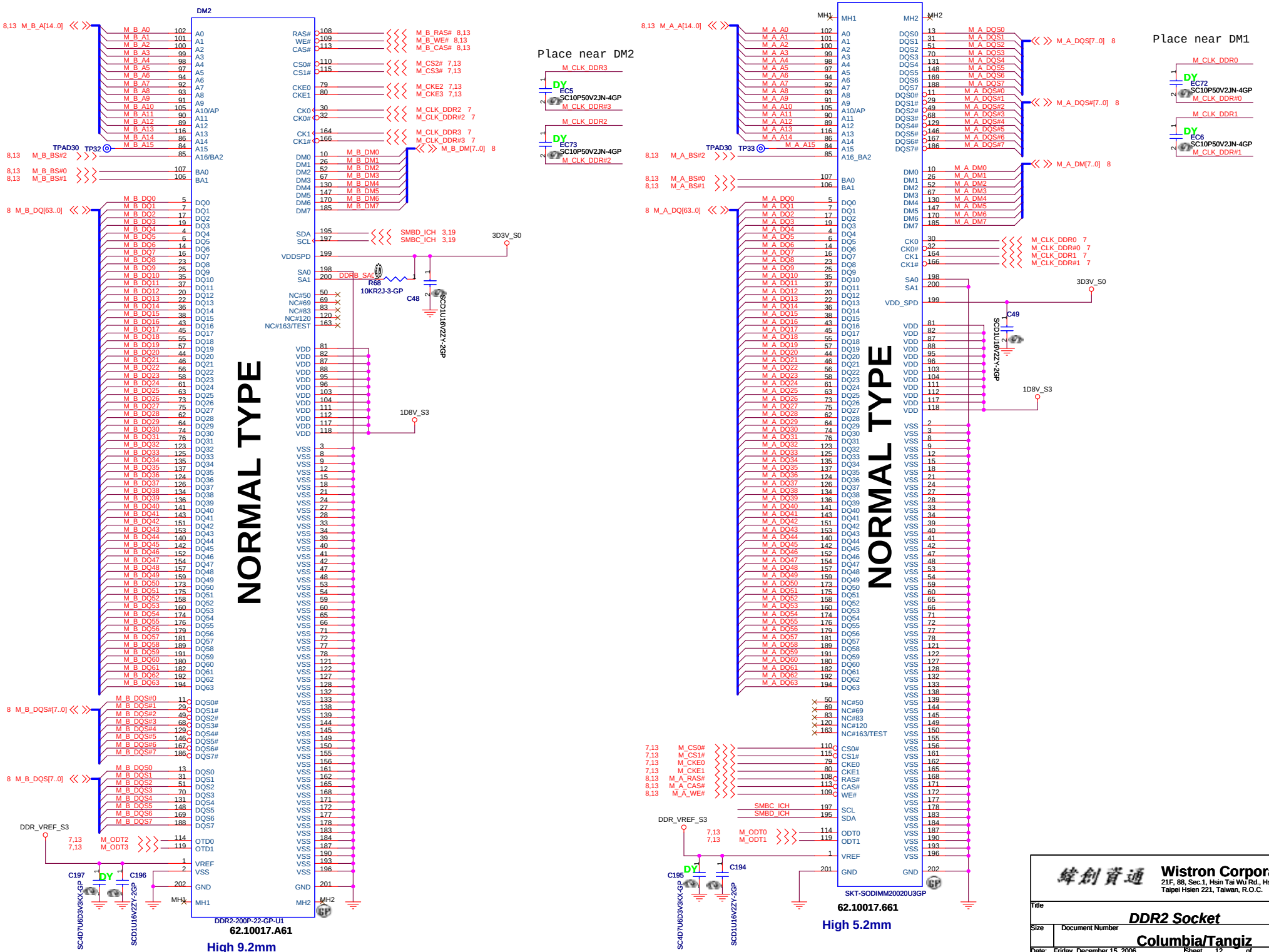
DM2
NORMAL TYPE
DDR2-200P-22-GP-U1
62.10017.A61
High 9.2mm
DM1
NORMAL TYPE
SKT-SODIMM20020U3GP
62.10017.661
High 5.2mm
Place near DM2
Place near DM1
Wistron Corporation
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DDR2 Socket
Columbia/Tangiz
Size
Document Number
Rev
SA
Date: Friday, December 15, 2006
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PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor

DDR_VREF_S0

RN13 SRN56J-5-GP
- M_A_A12 — M_CKE0 7,12
- M_A_A8 — M_A_BS#2 8,12

RN12 SRN56J-5-GP
- M_B_A8
- M_B_A9
- M_B_A5

RN14 SRN56J-5-GP
- M_B_A12 — M_CKE3 7,12
- M_B_BS#2 8,12
- M_CKE2 7,12

RN7 SRN56J-5-GP
- M_B_A3
- M_B_A1
- M_B_A10 — M_B_WE# 8,12

RN1 SRN56J-5-GP
- M_B_A13 — M_ODT2 7,12
- M_ODT3 7,12
- M_B_RAS# 8,12

RN5 SRN56J-5-GP
- M_B_A2
- M_B_A0
- M_B_A4 — M_B_BS#1 8,12

RN9 SRN56J-5-GP
- M_B_A14
- M_B_A11
- M_B_A7
- M_B_A6

RN4 SRN56J-5-GP
- M_B_BS#0 8,12
- M_B_CAS# 8,12
- M_CS3# 7,12
- M_CS2# 7,12

RN3 SRN56J-5-GP
- M_A_A13 — M_ODT0 7,12
- M_CS0# 7,12
- M_A_RAS# 8,12

RN8 SRN56J-5-GP
- M_A_A0
- M_A_A2
- M_A_A4 — M_A_BS#1 8,12

RN2 SRN56J-5-GP
- M_A_CAS# 8,12
- M_ODT1 7,12
- M_CS1# 7,12

RN10 SRN56J-5-GP
- M_A_A9
- M_A_A14
- M_A_A5
- M_A_A3

RN11 SRN56J-5-GP
- M_A_A6
- M_A_A7
- M_A_A11 — M_CKE1 7,12

RN6 SRN56J-5-GP
- M_A_A1
- M_A_A10 — M_A_BS#0 8,12
- M_A_WE# 8,12

M_A_A[14..0] — M_A_A[14..0] 8,12

M_B_A[14..0] — M_B_A[14..0] 8,12

Decoupling Capacitor

Put decap near power(0.9V) and pull-up resistor

DDR_VREF_S0

C110 C134 C117 C109 C103 C115 C125 C112 C97 C118 C128 — SCD1U16V2ZY-2GP — DY

C138 C104 C98 C106 C107 C127 C105 C101 C99 C137 C102 — SCD1U16V2ZY-2GP — DY

Place these Caps near DM1

1D8V_S3

C446 C436 C432 C424 C417 — SC2D2U6D3V3MX-1-GP

C421 C427 C434 C442 — SCD1U16V2ZY-2GP — DY

Place these Caps near DM2

1D8V_S3

C447 C440 C433 C426 C418 — SC2D2U6D3V3MX-1-GP

C445 C435 C431 C423 — SCD1U16V2ZY-2GP — DY

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Title: ***DDR2 Termination Resistor***

Size	Document Number	Rev
	Columbia/Tangiz	SA

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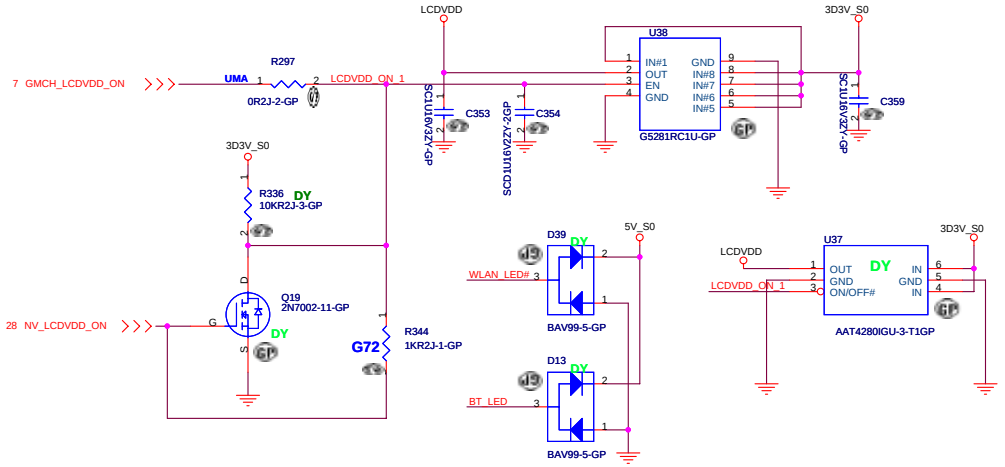
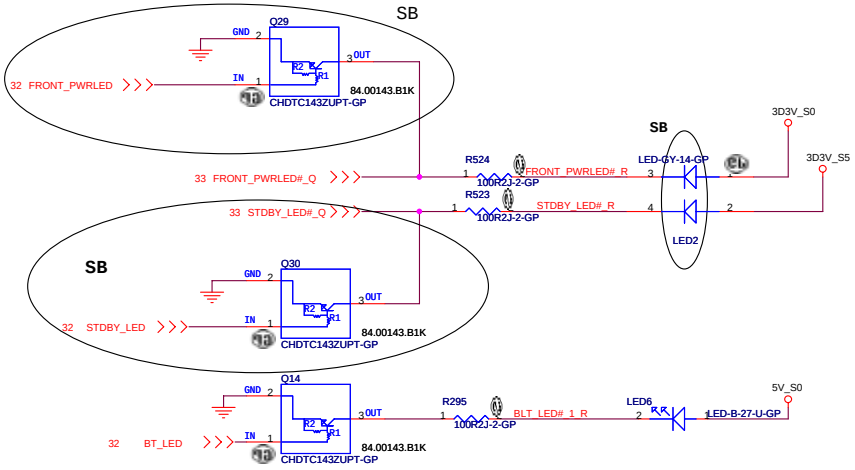
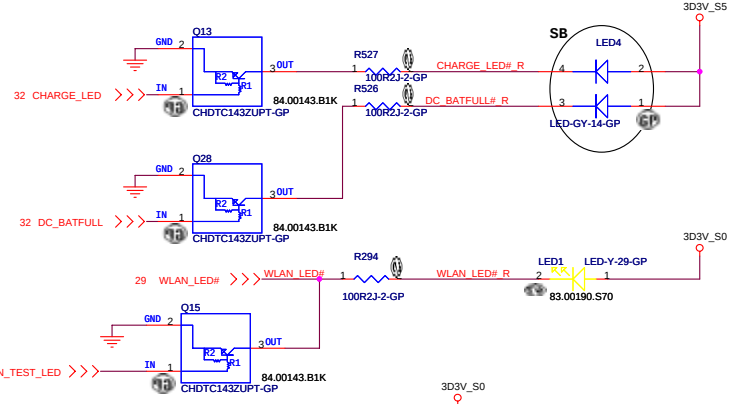
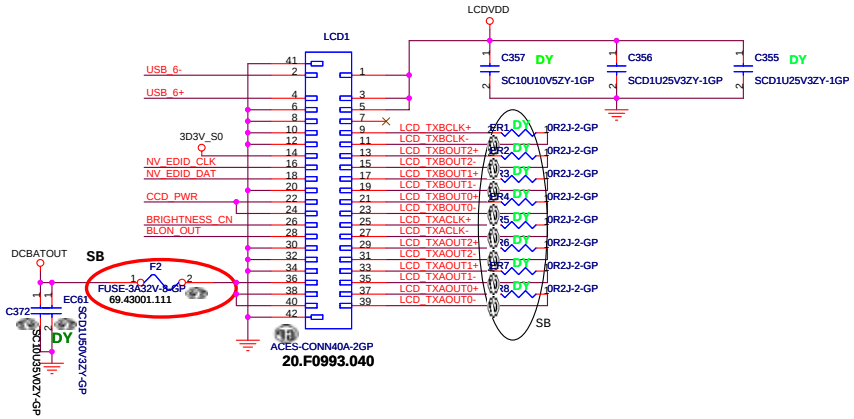
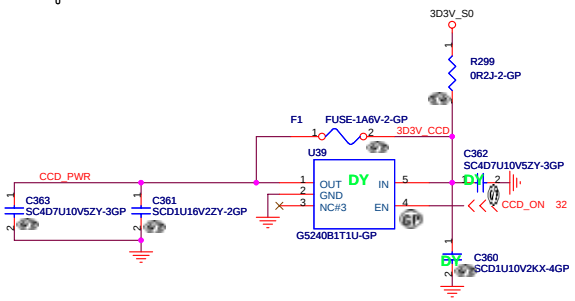
LCD/INVERTER CONN

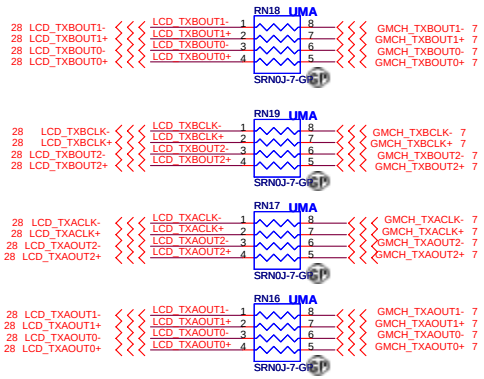


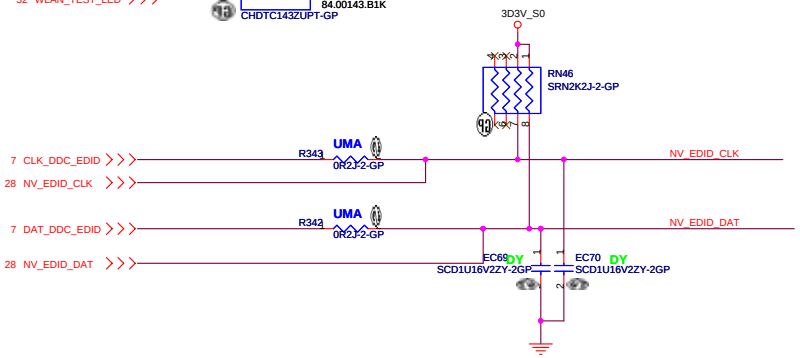


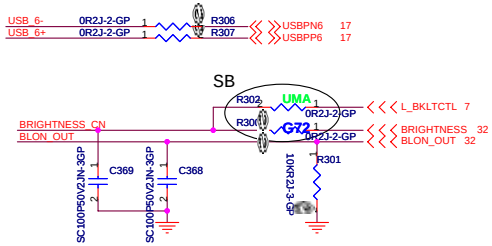












UMA

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Title: LCD CONN & LED

Size: | Document Number: Columbia/Tangiz | Rev: SA

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CRT I/F & CONNECTOR

Layout Note:
Place these resistors close to the CRT-out connector

Ferrite bead impedance: 10 ohm@100MHz

28 NV_RED — R113 UMA 0R2J-2-GP — L8 FCB1608CF-GP — CRT_R
7 GMCH_RED
28 NV_GREEN — R112 UMA 0R2J-2-GP — L7 FCB1608CF-GP — CRT_G
7 GMCH_GREEN
28 NV_BLUE — R111 UMA 0R2J-2-GP — L6 FCB1608CF-GP — CRT_B
7 GMCH_BLUE

R328 150R2F-1-GP, R325 150R2F-1-GP, R323 150R2F-1-GP
C416 SC22P50V2JN-4GP G72, C411 SC22P50V2JN-4GP G72, C407 SC22P50V2JN-4GP G72 SB
C420 SC6D8P50V2DN-GP, C413 SC6D8P50V2DN-GP, C409 SC6D8P50V2DN-GP

Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

CRT1 VIDEO-15-21-U4-GP
MH1, MH2
CRT_R, CRT_G, CRT_B, CRT_HSYNC1, CRT_VSYNC1, 5V_CRT_S0, DAT_DDC1_5, CLK_DDC1_5
C415 SC100P50V2JN-3GP, C405 SC18P50V2JN-1-GP, C419 SCD01U16V2KX-3GP, C406 SC18P50V2JN-1-GP, C414 SC100P50V2JN-3GP

20.20334.015

32 CRT_DEC# — R321 470R2J-2-GP — CRT_DEC_R — C404 SC100P50V2JN-3GP — D1 BAV99-5-GP (5V_S0)

Hsync & Vsync level shift

7 GMCH_HSYNC — R363 UMA 0R2J-2-GP
28 NV_HSYNC
7 GMCH_VSYNC — R364 UMA 0R2J-2-GP
28 NV_VSYNC

5V_S0 — C108 SCD1U16V2ZY-2GP
U44A TSAHCT125PW-GP — CRT_HSYNC1_R — R324 0R2J-2-GP — CRT_HSYNC1
U44B TSAHCT125PW-GP — CRT_VSYNC1_R — R322 0R2J-2-GP — CRT_VSYNC1
C412 SC18P50V2JN-1-GP DY, C408 SC18P50V2JN-1-GP DY

28 NV_DDCDAT — R366 0R2J-2-GP UMA — NV_DDCDAT
7 GMCH_DDCDATA
28 NV_DDCCLK — R365 0R2J-2-GP UMA — NV_DDCCLK
7 GMCH_DDCCLK

3D3V_S0 — RN44 SRN2K2J-2-GP
5V_CRT_S0 — CH751H-40PT D23
3D3V_S0 — SRN10KJ-6-GP RN43
Q16 2N7002DW-1-GP
CRT_DEC#, DAT_DDC1_5, CLK_DDC1_5

DDC_CLK & DATA level shift

TV CONN

28 NV_TV_LUMA — R115 UMA 0R2J-2-GP — R430 150R2F-1-GP — C565 SC33P50V2JN-3GP, L17 IND-1D2UH-5-GP, C570 SC150P50V2JN-3GP, C566 SC270P50V2JN-2GP — LUMA_1
7 TV_DACB

28 NV_TV_CRMA — R116 UMA 0R2J-2-GP — R413 150R2F-1-GP — C545 SC33P50V2JN-3GP, L15 IND-1D2UH-5-GP, C544 SC150P50V2JN-3GP, C546 SC270P50V2JN-2GP — CRMA_1
7 TV_DACC

28 NV_TV_COMP — R114 UMA 0R2J-2-GP — R423 150R2F-1-GP — C554 SC33P50V2JN-3GP, L16 IND-1D2UH-5-GP, C558 SC150P50V2JN-3GP, C555 SC270P50V2JN-2GP — COMP_1
7 TV_DACA

MINDIN7-22-GP TVOUT1

22.10021.I81

5V_S0
D11 BAV99-5-GP D8 — LUMA_1
D9 BAV99-5-GP D9 — CRMA_1
BAV99-5-GP — COMP_1
D5 BAV99-5-GP D3 — CRT_R
BAV99-5-GP D2 — CRT_G
BAV99-5-GP — CRT_B

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Title: *CRT/TV Connector*
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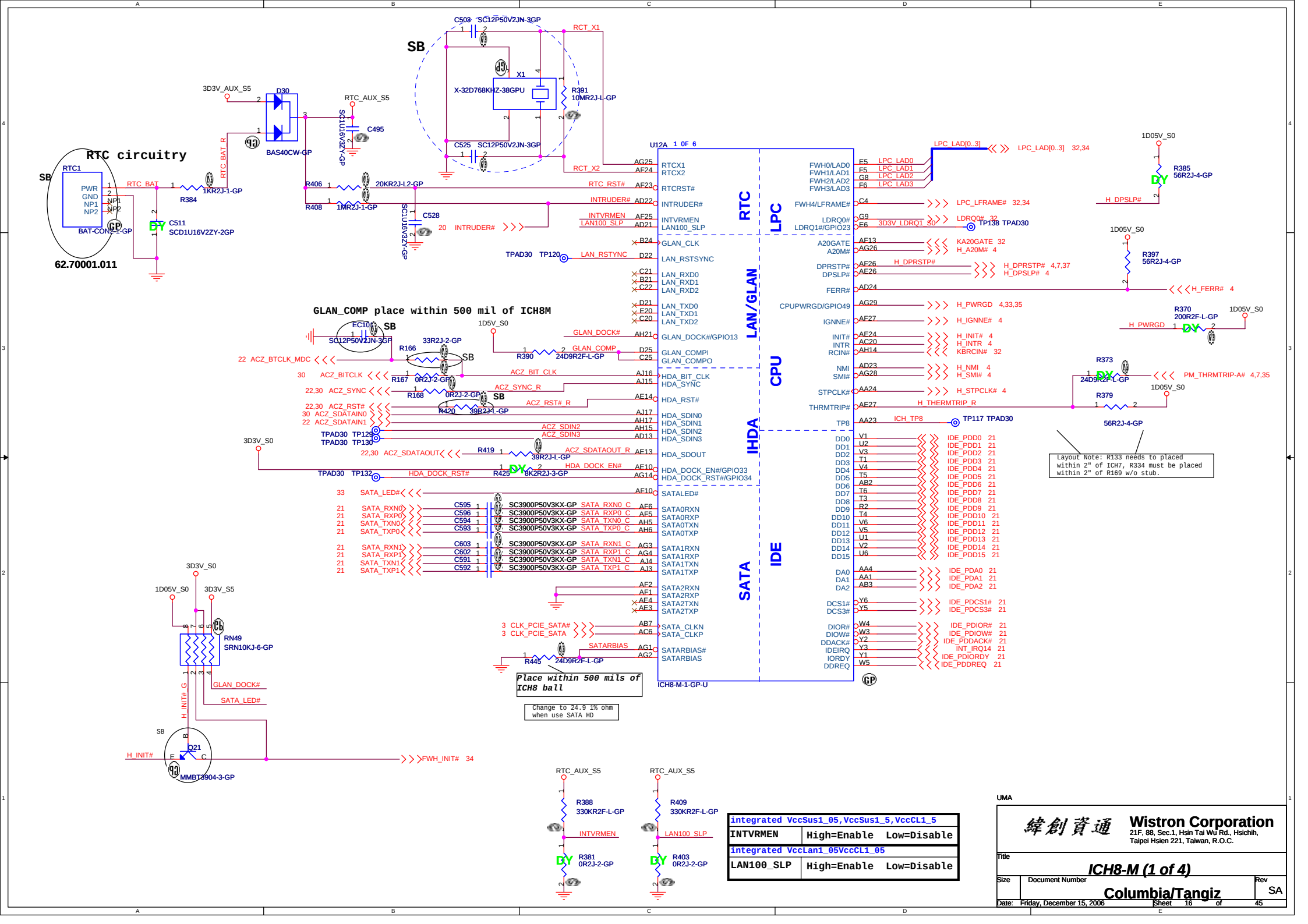
RTC circuitry
62.70001.011
GLAN_COMP place within 500 mil of ICH8M
Place within 500 mils of ICH8 ball
Change to 24.9 1% ohm when use SATA HD
Layout Note: R133 needs to placed within 2" of ICH7, R334 must be placed within 2" of R169 w/o stub.
integrated VccSus1_05,VccSus1_5,VccCL1_5
INTVRMEN High=Enable Low=Disable
integrated VccLan1_05VccCL1_05
LAN100_SLP High=Enable Low=Disable
U12A 1 OF 6
ICH8-M-1-GP-U
RTC
LPC
LAN/GLAN
CPU
IHDA
SATA
IDE
UMA
Wistron Corporation
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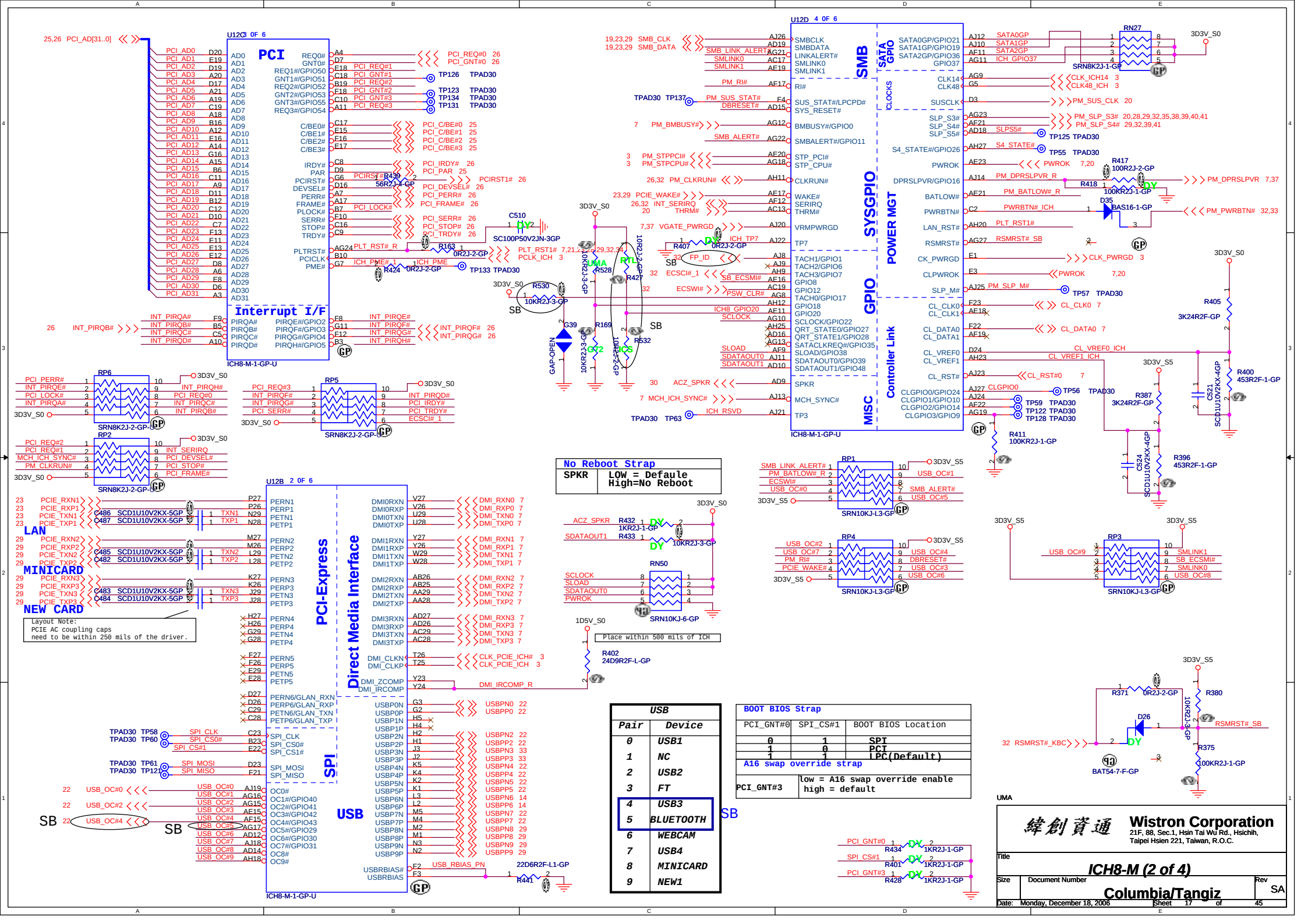
ICH8-M (1 of 4)
Columbia/Tangiz
Friday, December 15, 2006


U12C 3 OF 6
PCI
Interrupt I/F
ICH8-M-1-GP-U
U12D 4 OF 6
SMB
SATA GPIO
CLOCKS
SYSGPIO
POWER MGT
GPIO
Controller Link
MISC
ICH8-M-1-GP-U
U12B 2 OF 6
PCI-Express
Direct Media Interface
SPI
USB
ICH8-M-1-GP-U
No Reboot Strap
SPKR LOW = Defaule High=No Reboot
LAN
MINICARD
NEW CARD
Layout Note:
PCIE AC coupling caps
need to be within 250 mils of the driver.
Place within 500 mils of ICH
USB
Pair Device
0 USB1
1 NC
2 USB2
3 FT
4 USB3
5 BLUETOOTH
6 WEBCAM
7 USB4
8 MINICARD
9 NEW1
BOOT BIOS Strap
PCI_GNT#0 SPI_CS#1 BOOT BIOS Location
0 1 SPI
1 0 PCI
1 1 LPC(Default)
A16 swap override strap
PCI_GNT#3 low = A16 swap override enable high = default
UMA
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Title
ICH8-M (2 of 4)
Size
Document Number
Columbia/Tangiz
Rev
SA
Date: Monday, December 18, 2006
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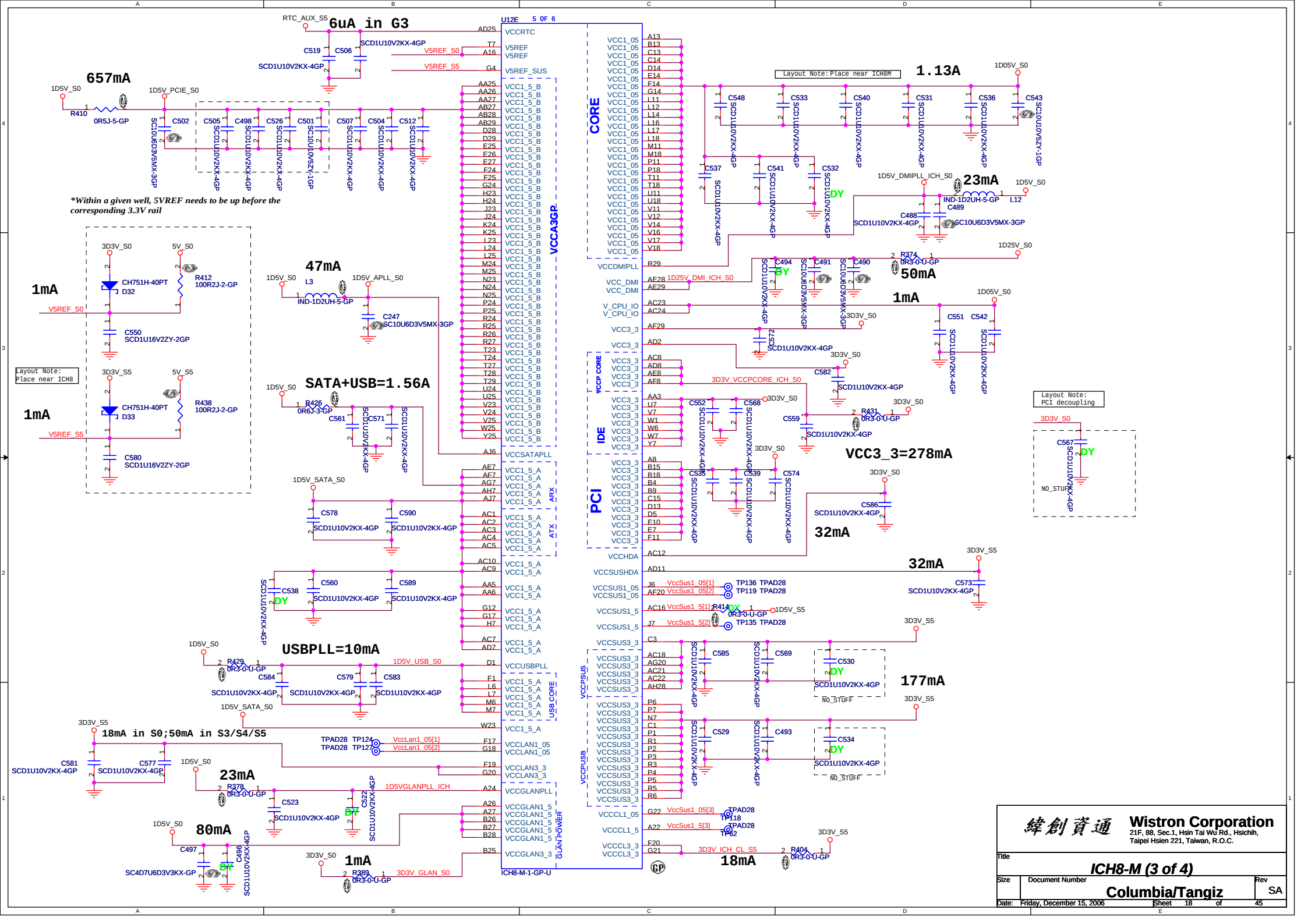
6uA in G3
657mA
1mA
47mA
SATA+USB=1.56A
USBPLL=10mA
18mA in S0;50mA in S3/S4/S5
23mA
80mA
1mA
1mA
1.13A
23mA
50mA
1mA
VCC3_3=278mA
32mA
32mA
177mA
18mA
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
Layout Note: Place near ICH8M
Layout Note: Place near ICH8
Layout Note: PCI decoupling
U12E 5 OF 6
ICH8-M-1-GP-U
CORE
VCCA3GP
IDE
PCI
VCCP CORE
VCCPSUS
VCCPUSB
USB CORE
GLAN POWER
ARX
ATX
Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH8-M (3 of 4)
Size
Document Number
Columbia/Tangiz
Rev
SA
Date: Friday, December 15, 2006
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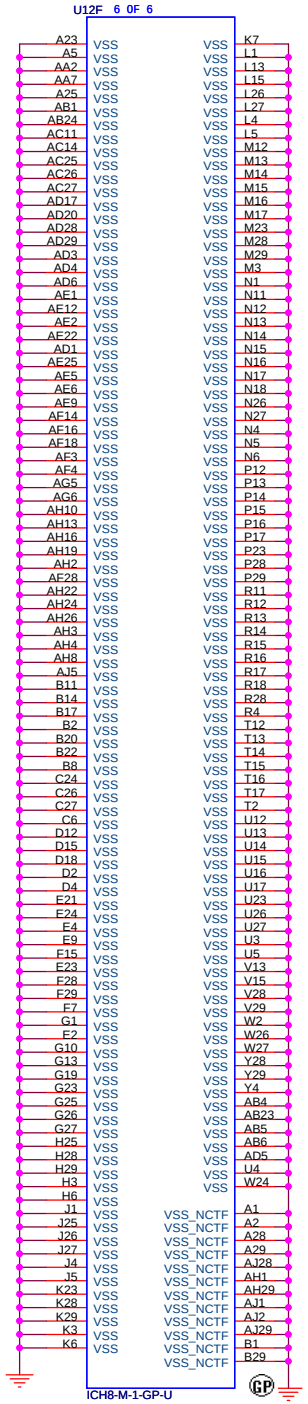

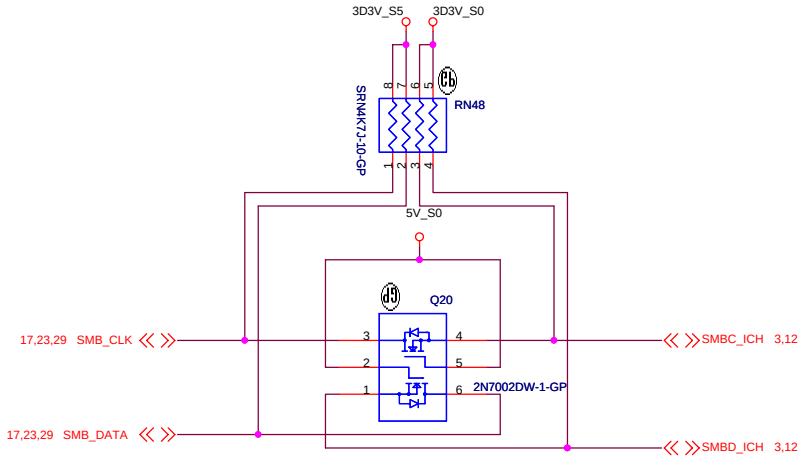

Q13 & Q14 connect SMLINK and SMBUS in S) for SMBus 2.0 compliance

SMBUS

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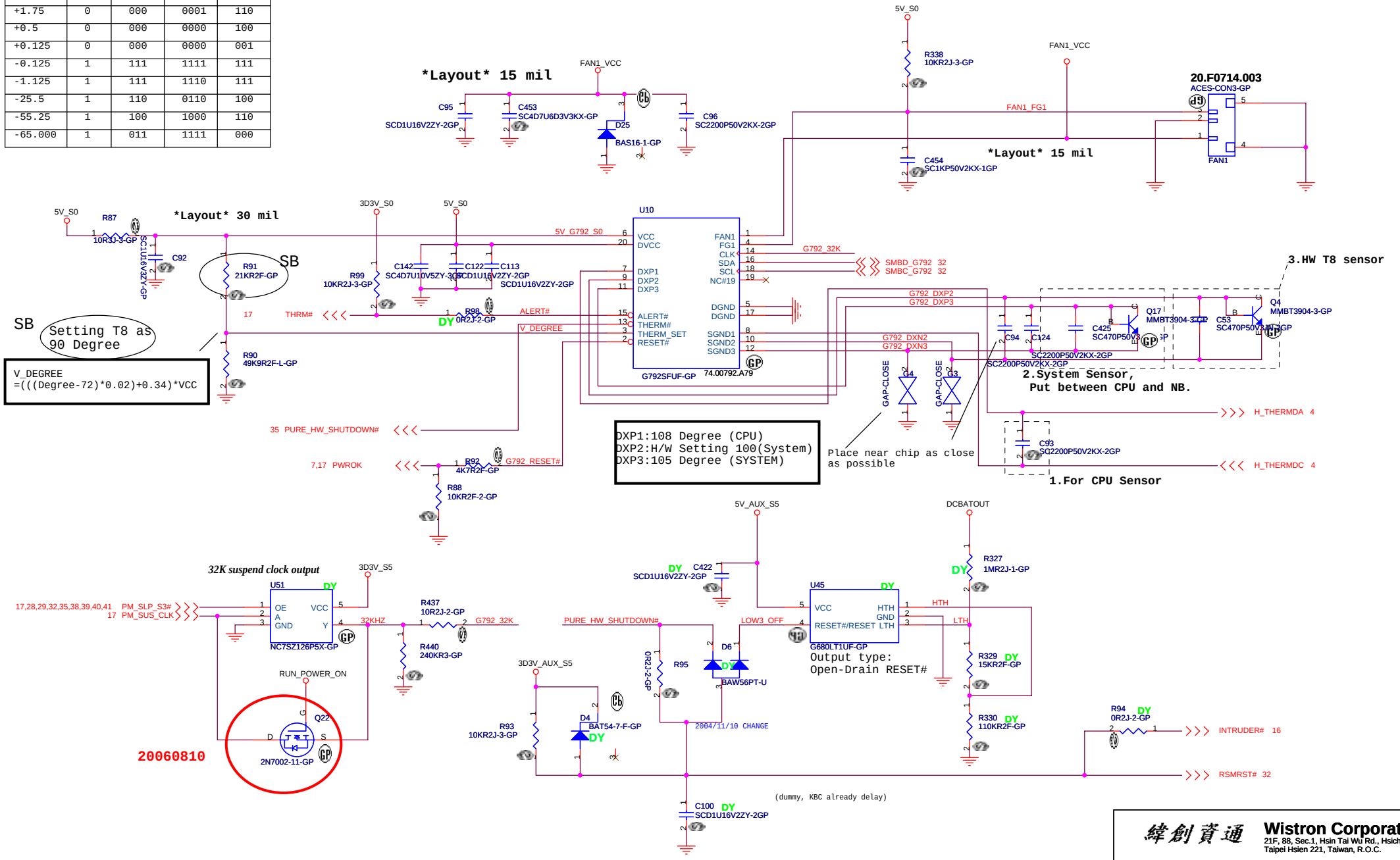
Title	*ICH8-M (4 of 4)*	
Size	Document Number: **Columbia/Tangiz**	Rev: SA
Date: Friday, December 15, 2006	Sheet 19 of 45	

TEMP.	Digital Output Data Bits			
	Sign	MSB	LSB	EXT
+127.875	0	111	1111	111
+126.375	0	111	1110	011
+25.5	0	001	1001	100
+1.75	0	000	0001	110
+0.5	0	000	0000	100
+0.125	0	000	0000	001
-0.125	1	111	1111	111
-1.125	1	111	1110	111
-25.5	1	110	0110	100
-55.25	1	100	1000	110
-65.000	1	011	1111	000



緯創資通 Wistron Corporation
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Title: Thermal/Fan Controllor

Size | Document Number: Columbia/Tangiz | Rev: SA

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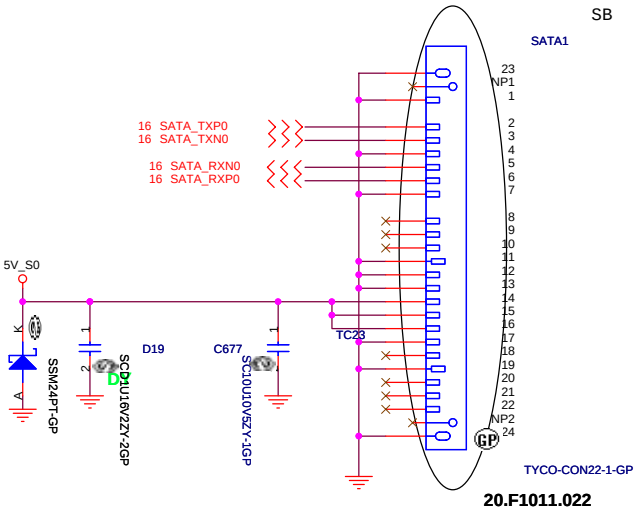
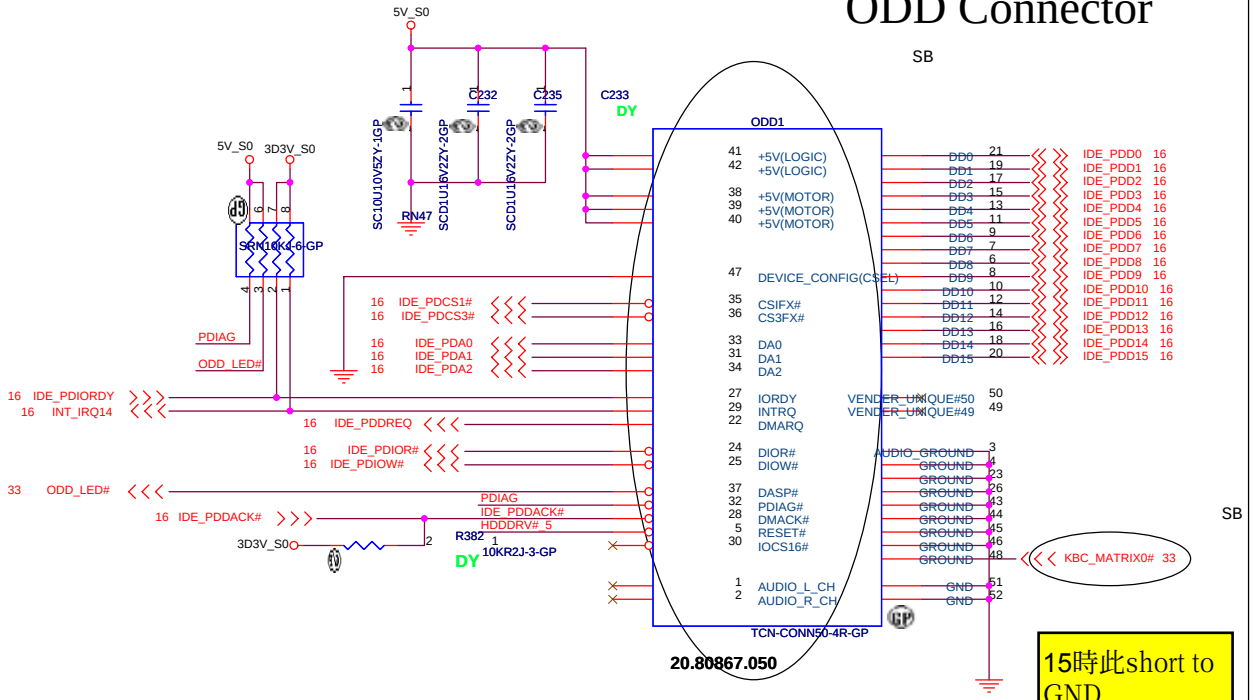
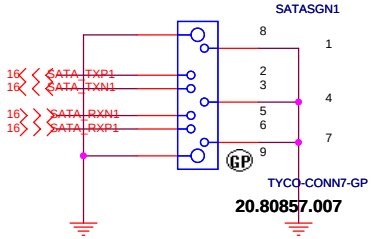
SATA HD Connector

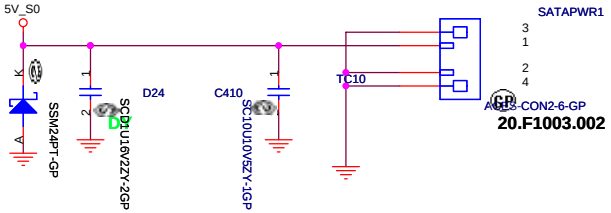


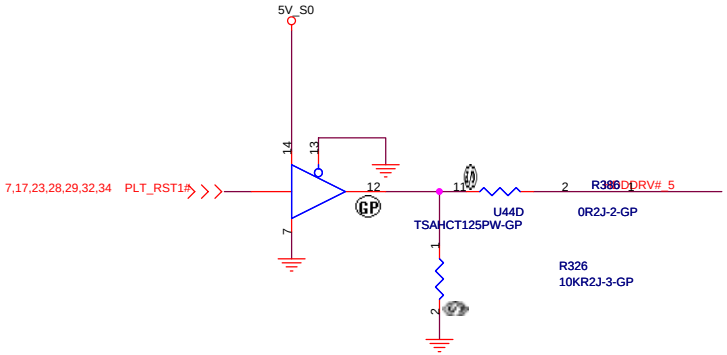
ODD Connector



15時此short to GND
17時反之
都是通過ODD插入時的機構實現.







UMA

緯創資通

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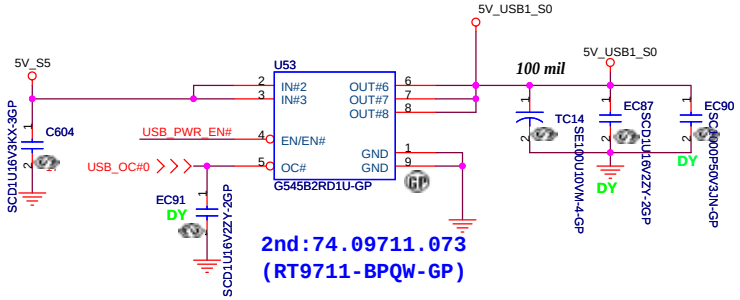
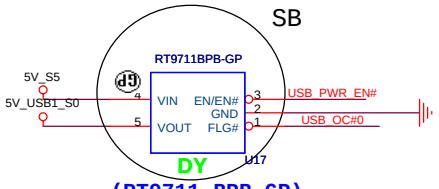
Taipei Hsien 221, Taiwan, R.O.C.

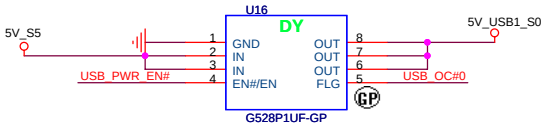
Title: ***HDD and CDROM***

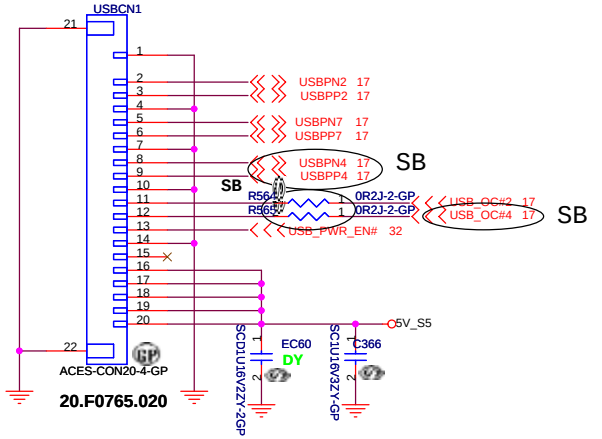
Size | Document Number: **Columbia/Tangiz**

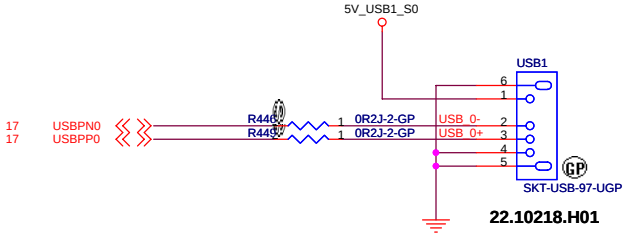
Date: Friday, December 15, 2006 | Sheet 21 of



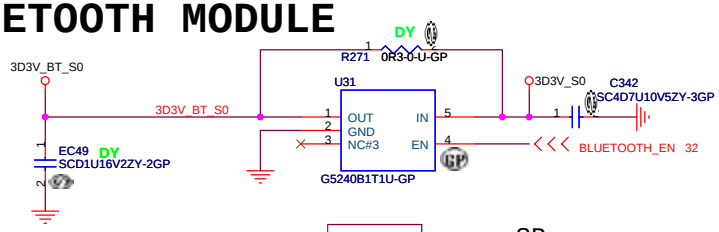




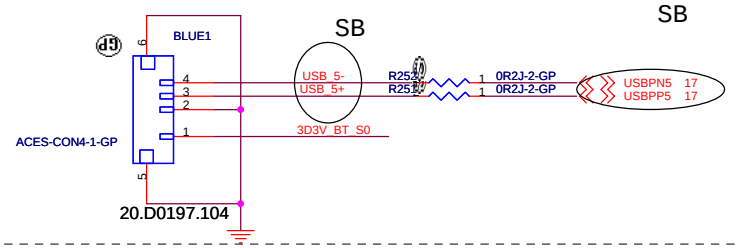




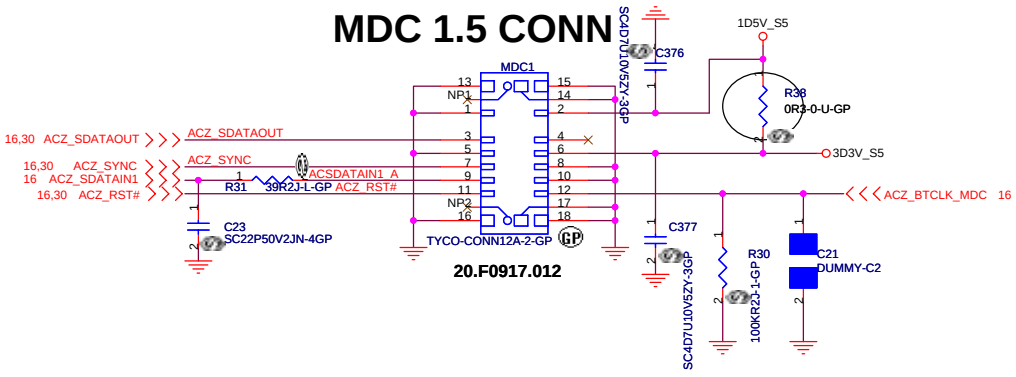
BLUETOOTH MODULE

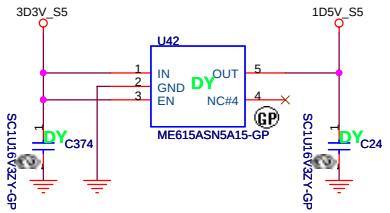


EC21 put near BLUE1 / all USB put one choke near connector by EMI request



MDC 1.5 CONN





UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title: USB / MDC / BLUETOOTH

Size	Document Number	Rev
	Columbia/Tangiz	SA

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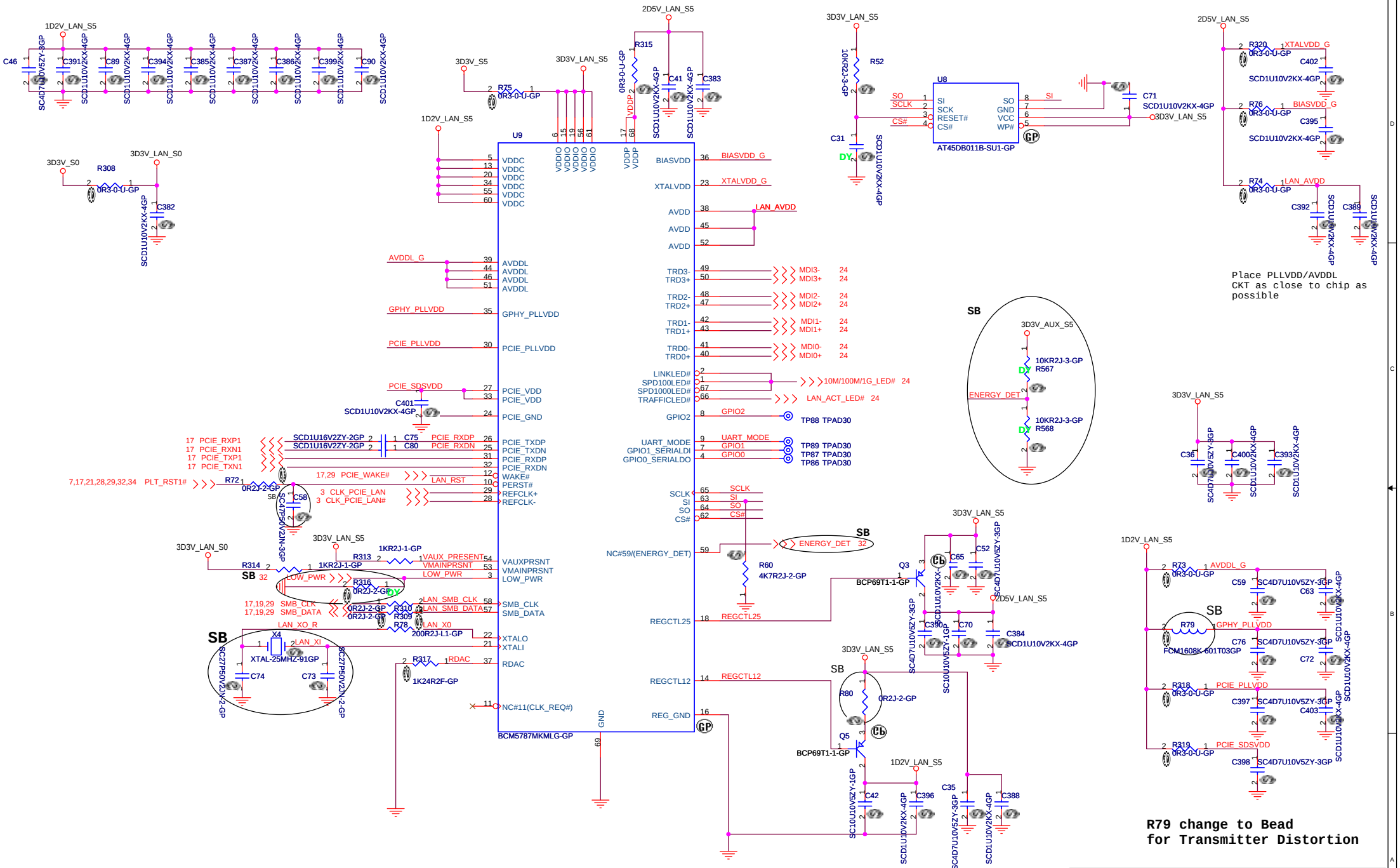
U9
BCM5787MKMLG-GP
U8
AT45DB011B-SU1-GP
Q3
BCP69T1-1-GP
Q5
BCP69T1-1-GP
X4
XTAL-25MHZ-91GP
SB
UMA
Place PLLVDD/AVDDL
CKT as close to chip as
possible
R79 change to Bead
for Transmitter Distortion
Wistron Corporation
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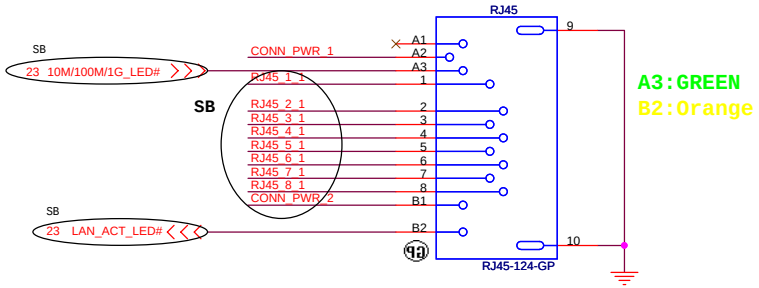
Taipei Hsien 221, Taiwan, R.O.C.
Title
BCM5787MKMLG
Size A3
Document Number
Columbia/Tangiz
Rev SA
Date: Friday, December 15, 2006
Sheet 23 of 45

LAN Connector

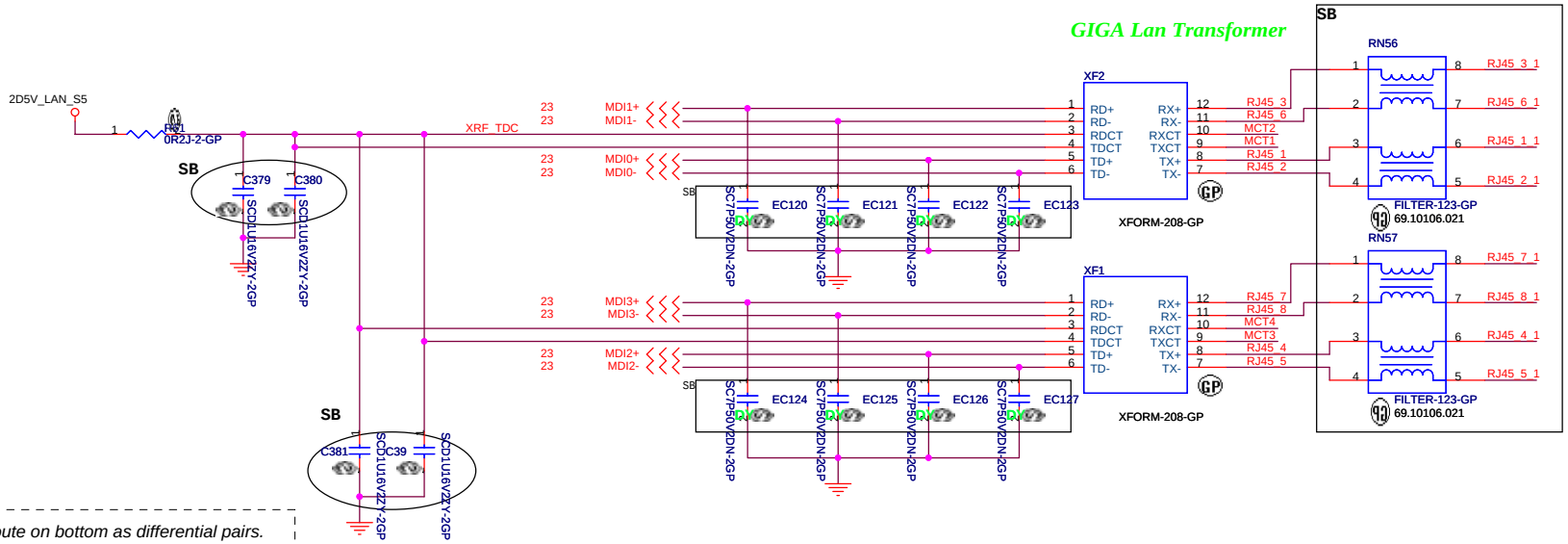
Voltage Rail	4401E	5789	5787
VDDIO_PCI	3D3V_LAN_S5	3D3V_S0	Don't Care
VDDC	1D8V_LAN_S5	1D2V_LAN_S5	
VDDIO	3D3V_LAN_S5	3D3V_LAN_S5	
VESD	3D3V_LAN_S5	3D3V_S0	Don't Care
VDDP	Don't Care	2D5V_S5	
3D3V_2D5V_S5	3D3V_S5	2D5V_S5	
1D8V_1D2V_S5	1D8V_LAN_S5	1D2V_S5	

LAN Connector



22.10277.011

GIGA Lan Transformer



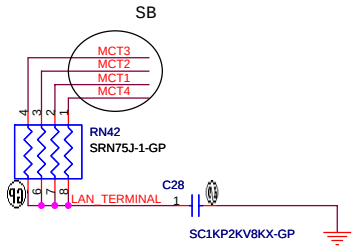
LAN Link: Green(A3), behavior is the same for 10/100/1000 bits

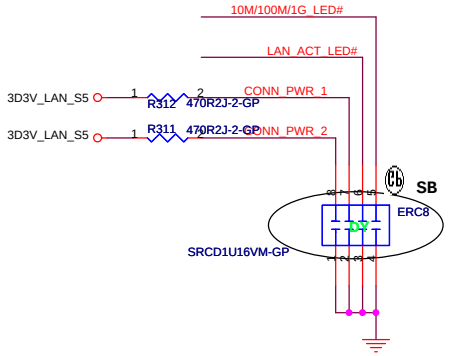
LAN Data: Yellow(B2), when LAN is transfering data.

1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

RJ11 signal must leave the other signal or power plane 100mil.

DOC_TIP,DOC_RING,TIP,RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers





10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6

UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAN Connector**

Size: A3 | Document Number: Columbia/Tangiz | Rev: SA

Date: Friday, December 15, 2006 | Sheet 24 of 45

C782 should close Pin-P15
and Pin-R17.

TI PCI7412

U54A

1 0F 2

71.07412.B0U

PCI7412ZHK-GP

* All 1394 signals must be routed on top side only
* Differential pairs of each ports should have equal trace length
* Stubs must be keep as short as possible

Bypass/Decupoling Capacitors
Should be places as close to
PCI7412 as possible

UMA

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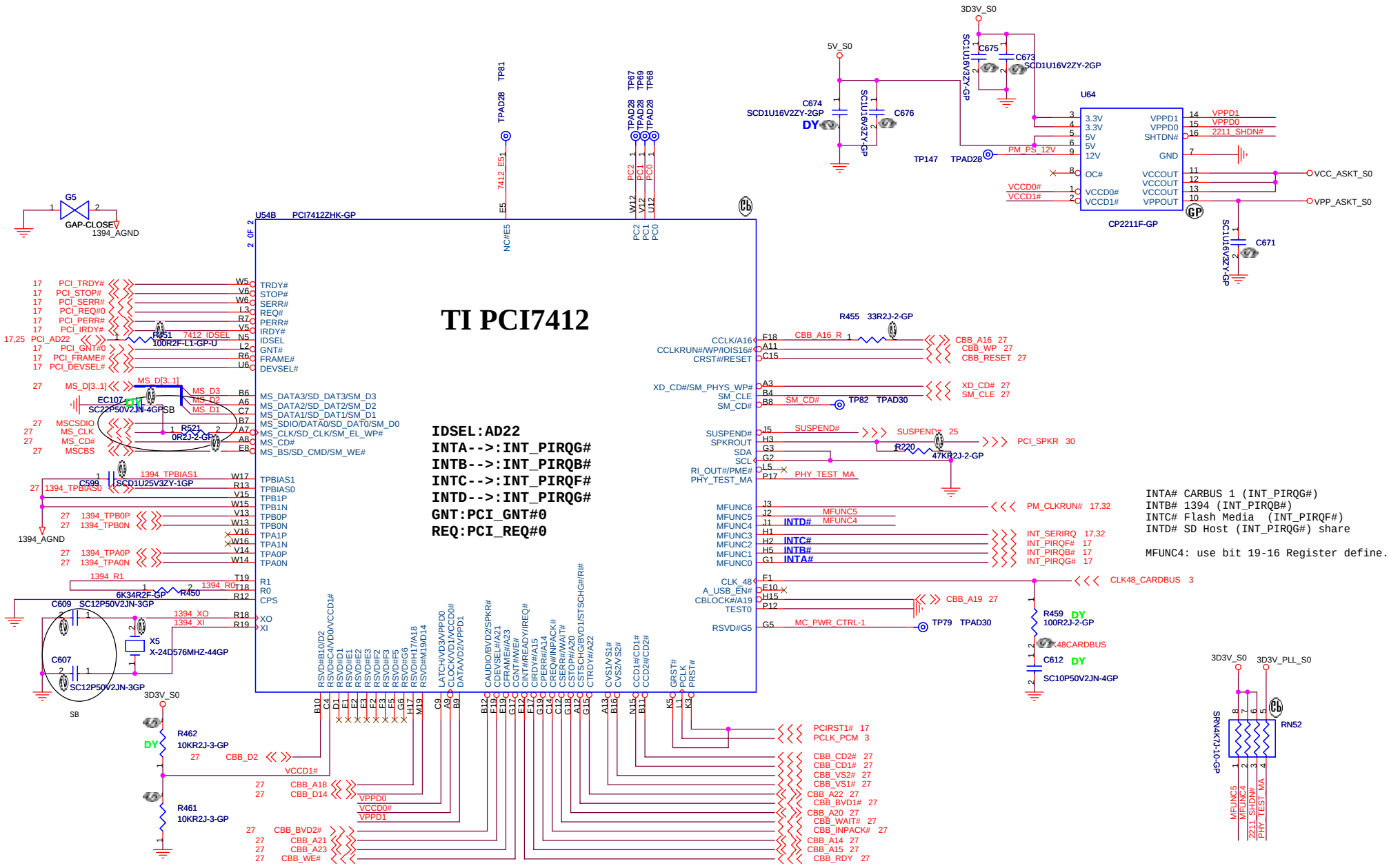
Taipei Hsien 221, Taiwan, R.O.C.

Title: TI PCI7412 (1 of 2)

Size | Document Number: Columbia/Tangiz | Rev: SA

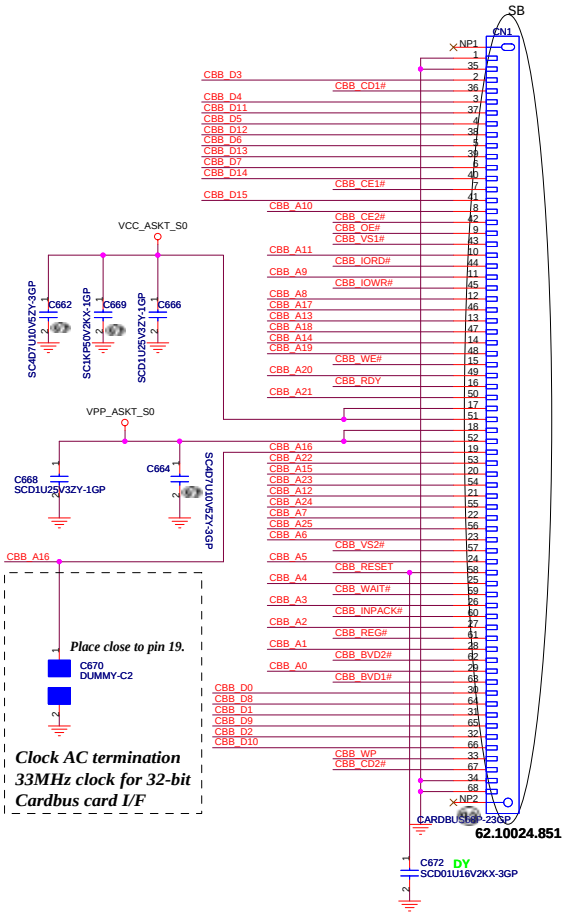
Date: Friday, December 15, 2006 | Sheet 25 of 45



UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	*TI PCI7412 (2 of 2)*	
Size	Document Number: Columbia/Tangiz	Rev: SA
Date: Friday, December 15, 2006	Sheet 26 of 45	

PCMCIA Socket



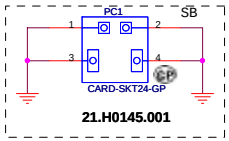
Cardbus I/F

CBB_D[15..0] — CBB_D[15..0] 25,26

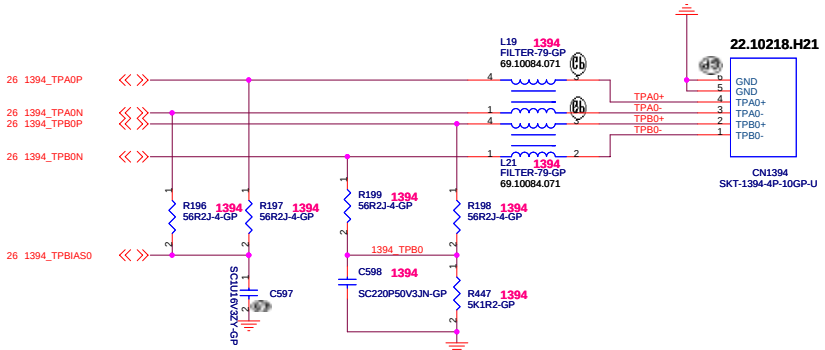
CBB_A[25..0] — CBB_A[25..0] 25,26

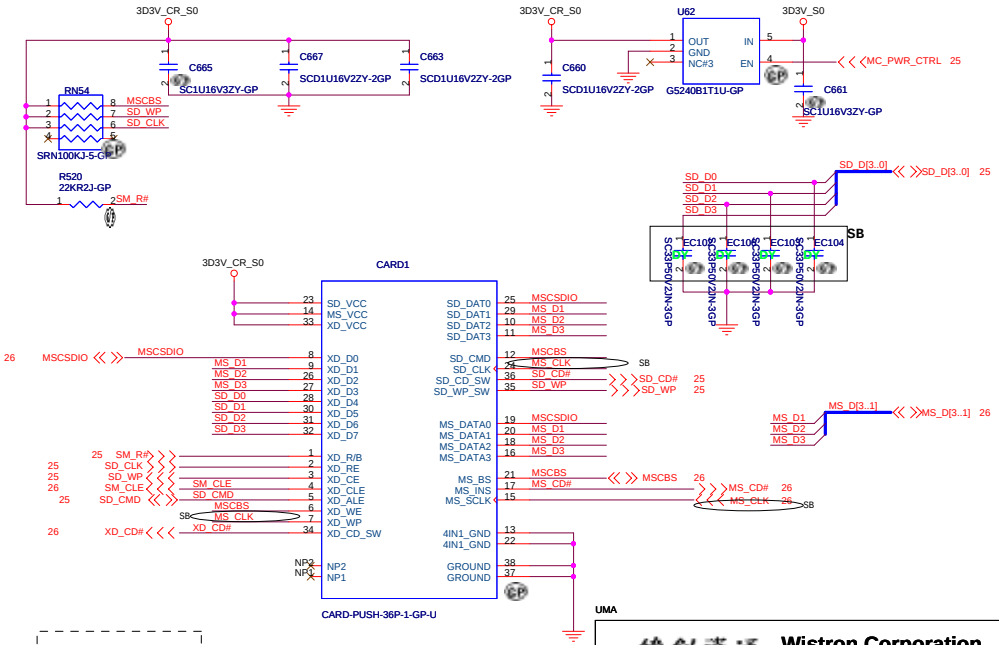
CBB_IORD# 25
CBB_IOWR# 25
CBB_OE# 25
CBB_WE# 26
CBB_REG# 25
CBB_RDY 26
CBB_WP 26
CBB_RESET 26
CBB_WAIT# 26
CBB_INPACK# 26

CBB_CE1# 25
CBB_CE2# 25
CBB_BVD1# 26
CBB_BVD2# 26
CBB_CD1# 26
CBB_CD2# 26
CBB_VS1# 26
CBB_VS2# 26



1394 Connector





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Title: PCMCIA / 1394 / CARD READER

Size | Document Number: Columbia/Tangiz | Rev: SA

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NV SMBus
A(pin143&145) : VGA(CRT) / DOCK
B(pin218&220) : DVI
C(pin208&210) : HDMI / TPI / LVDS

Put near graphic connector

7 PEG_TXP[15..0]
7 PEG_TXN[15..0]
7 PEG_RXP[15..0]
7 PEG_RXN[15..0]

14 LCD_TXBOUT0+
14 LCD_TXBOUT0-
14 LCD_TXBOUT1+
14 LCD_TXBOUT1-
14 LCD_TXBOUT2+
14 LCD_TXBOUT2-
14 LCD_TXBCLK+
14 LCD_TXBCLK-
15 NV_BLUE
15 NV_GREEN
15 NV_RED

LCD_TXACLK- 14
LCD_TXACLK+ 14
LCD_TXAOUT2- 14
LCD_TXAOUT2+ 14
LCD_TXAOUT1- 14
LCD_TXAOUT1+ 14
LCD_TXAOUT0- 14
LCD_TXAOUT0+ 14
NV_EDID_DAT 14
NV_EDID_CLK 14
NV_LCDVDD_ON 14
NV_BLON 32
NV_DVI_DAT 44
NV_DVI_CLK 44

-2

37,38,39,40,41 CPUCORE_ON
17,20,29,32,35,38,39,40,41 PM_SLP_S3#
G72 R347 0R2J-2-GP
G72 R337 0R2J-2-GP
5V_S0
DY
C457 SCD1U25V3KX-GP
TPAD30TP95

15 NV_TV_COMP
15 NV_TV_LUMA
15 NV_TV_CRMA

TP40 TP38 TP35 TP39 TP34 TP37 TP36 TPAD30
TP92 TP91 TP96 TP93 TP94 TP97 TPAD30

3D3V_S0
2D5V_S0
C456 SC10U10V5ZY-1GP G72
C458 SCD1U25V3KX-GP DY

MH1 MH2 231 232
MXM1
TYCO-CONN230A-GP-U1
G72
20.F0871.230

DCBATOUT
C476 C477 DY
SC4D7U25V6KX-1GP C480 C479 C481 DY
SCD1U25V3KX-GP

PEG_RXN15 PEG_RXP15 PEG_RXN14 PEG_RXP14 PEG_RXN13 PEG_RXP13 PEG_RXN12 PEG_RXP12 PEG_RXN11 PEG_RXP11 PEG_RXN10 PEG_RXP10 PEG_RXN9 PEG_RXP9 PEG_RXN8 PEG_RXP8 PEG_RXN7 PEG_RXP7 PEG_RXN6 PEG_RXP6 PEG_RXN5 PEG_RXP5 PEG_RXN4 PEG_RXP4 PEG_RXN3 PEG_RXP3 PEG_RXN2 PEG_RXP2 PEG_RXN1 PEG_RXP1 PEG_RXN0 PEG_RXP0

3 CLK_PCIE_PEG#
3 CLK_PCIE_PEG
TP43 TPAD30 TP47 TPAD30 TP46 TPAD30 TP106 TPAD30

7,17,21,23,29,32,34 PLT_RST1#
R367 0R2J-2-GP G72
C478 SC100P50V2JN-3GP G72
PLT_RST1#_MXM

35 MXM_THER

15 NV_HSYNC
15 NV_VSYNC
15 NV_DDCCLK
15 NV_DDCDAT

TPAD30 TP44 SPDIF_HDMI
TPAD30 TP112 GPU_BUFRST#
TPAD30 TP107 MP_INT
TPAD30 TP99 GPU_PRGM#

TPAD30 TP98 IGP_UTX2#
TPAD30 TP103 IGP_UTX2
TPAD30 TP108 TMDS_GPIO6_SW
TPAD30 TP148

EMI REQUEST

TMDS_A_TX0+_1 ERN4 TMDS_A_TX0+ 44
TMDS_A_TX0-_1 G72 TMDS_A_TX0- 44
SRN33J-5-GP-U
TMDS_A_TX1+_1 ERN3 TMDS_A_TX1+ 44
TMDS_A_TX1-_1 G72 TMDS_A_TX1- 44
SRN33J-5-GP-U
TMDS_A_TX2+_1 ERN2 TMDS_A_TX2+ 44
TMDS_A_TX2-_1 G72 TMDS_A_TX2- 44
SRN33J-5-GP-U
TMDS_A_TXC+_1 ERN1 TMDS_A_TXC+ 44
TMDS_A_TXC-_1 G72 TMDS_A_TXC- 44
SRN33J-5-GP-U

ERN77~ERN80要靠近MXM1

DVI_A_HPD 44

TMDS_B_TX0+ TP115 TPAD30
TMDS_B_TX0- TP114 TPAD30
TMDS_B_TX1+ TP105 TPAD30
TMDS_B_TX1- TP104 TPAD30
TMDS_B_TX2+ TP111 TPAD30
TMDS_B_TX2- TP110 TPAD30
G72_27MHZ TP102 TPAD30
G72_27MHZSS TP113 TPAD30

DVI_B_HPD TP109 TPAD30
TMDS_B_TXC+ TP101 TPAD30
TMDS_B_TXC- TP100 TPAD30

UMA

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Title: Graphic MXM CONN
Size: A3 | Document Number: Columbia/Tangiz | Rev: SA
Date: Friday, December 15, 2006 | Sheet 28 of 45

Mini Card Connector

NEWCARD Connector

SB

SK1

CARDBUS-SKT91-GP

Reserve the symbol for bottom side connector

CARDBUS26P-8GP

NEW1

62.10024.881

Mini Card Connector

SB

MINIC1

SKT-MINI52P-13-GP

62.10043.461

W83L351YG-GP U61

Place them Near to Chip

Place them Near to Connector

Place near MINIC1

UMA

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Title: MINI CARD / NEW CARD

Size | Document Number: Columbia/Tangiz | Rev: SA

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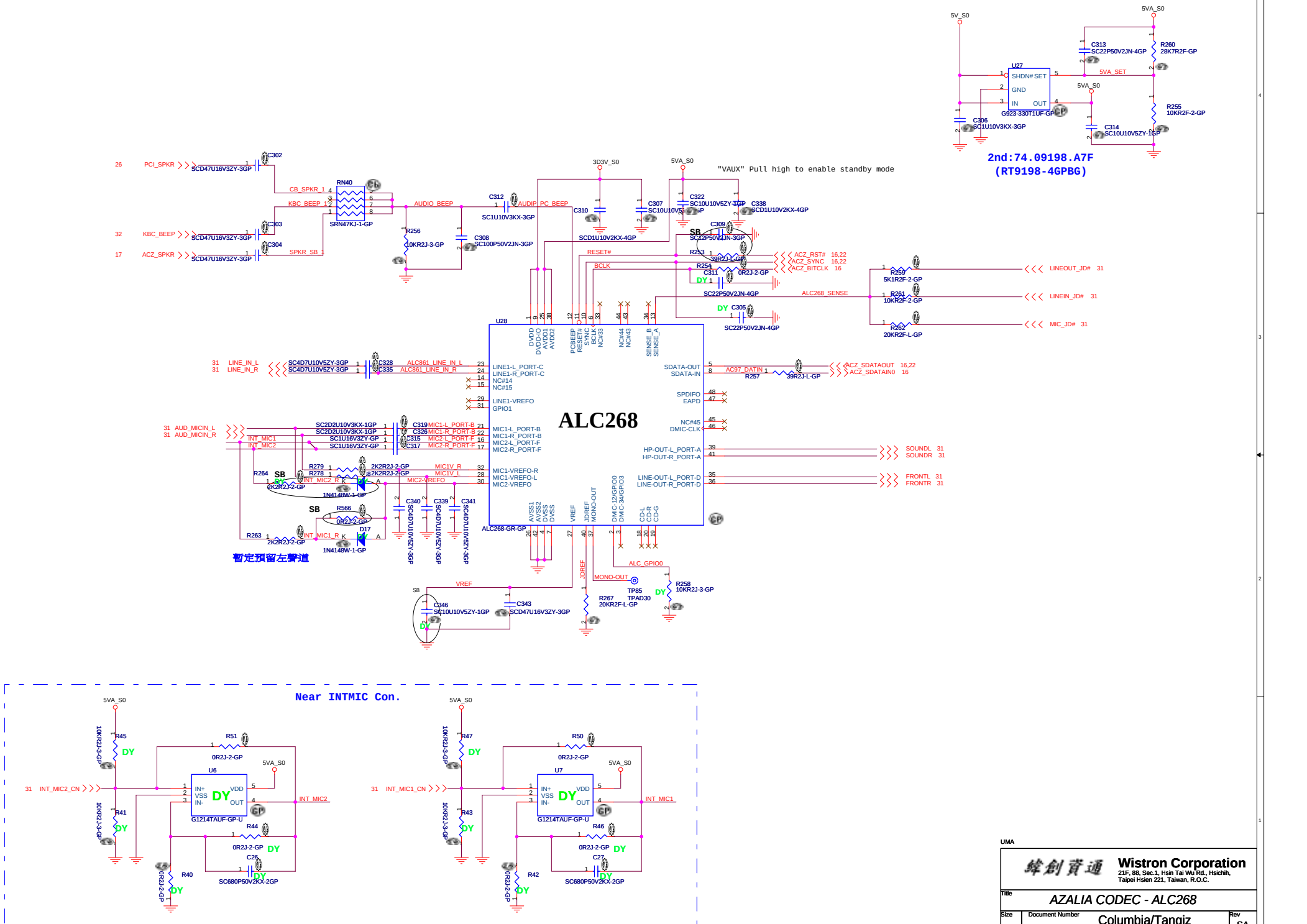
2nd:74.09198.A7F
(RT9198-4GPBG)
"VAUX" Pull high to enable standby mode
ALC268
U28
ALC268-GR-GP
暫定預留左聲道
Near INTMIC Con.
U6
U7
G1214TAUF-GP-U
U27
G923-330T1UF-GP
Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.
UMA
AZALIA CODEC - ALC268
Columbia/Tangiz
Rev SA
Date: Friday, December 29, 2006
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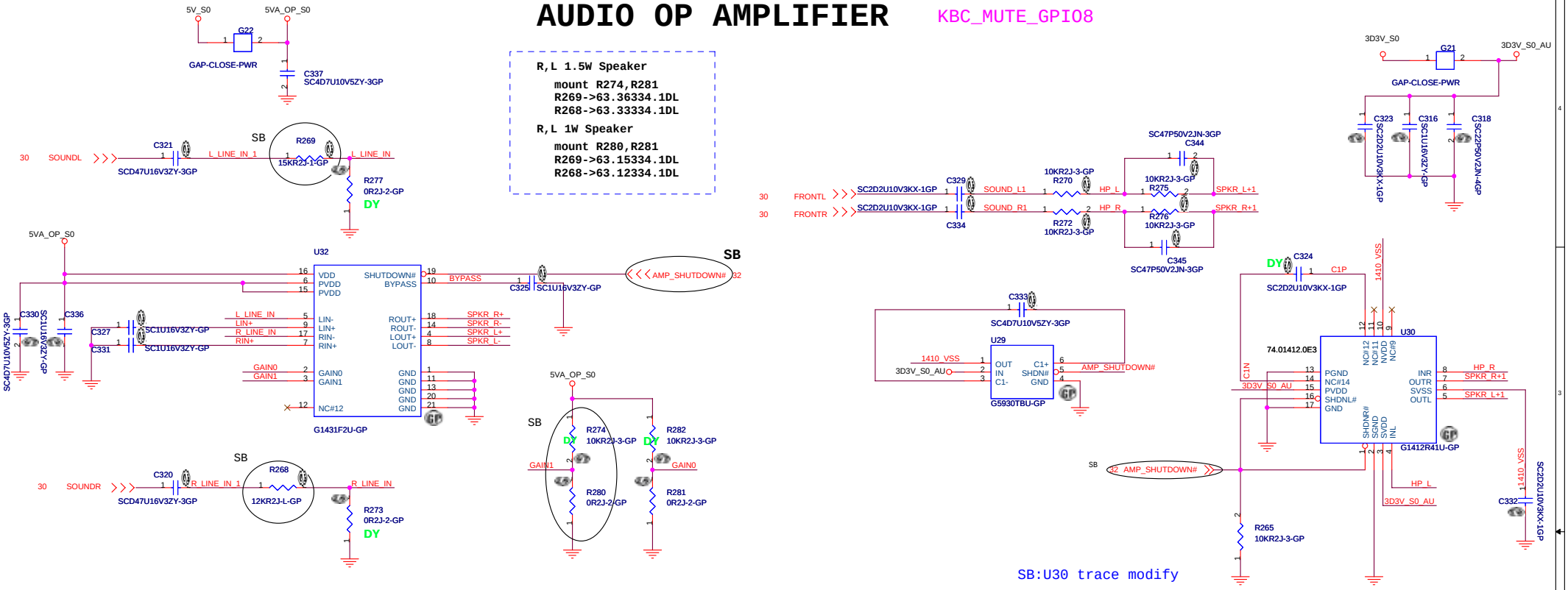
AUDIO OP AMPLIFIER

KBC_MUTE_GPIO8

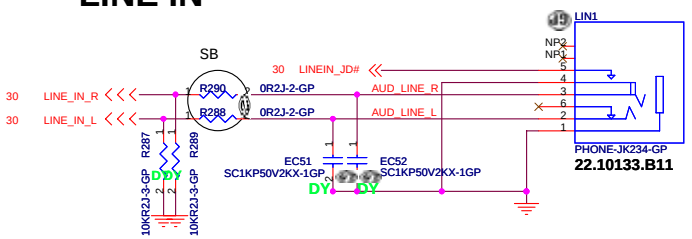
R,L 1.5W Speaker
mount R274,R281
R269->63.36334.1DL
R268->63.33334.1DL

R,L 1W Speaker
mount R280,R281
R269->63.15334.1DL
R268->63.12334.1DL

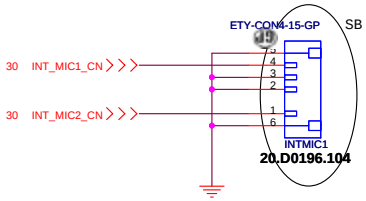


SB:U30 trace modify

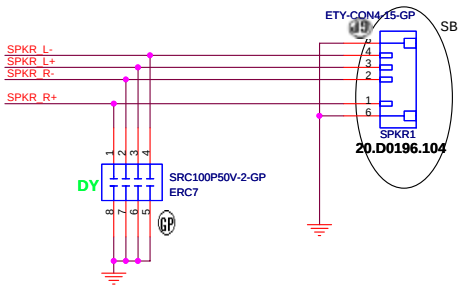
LINE IN



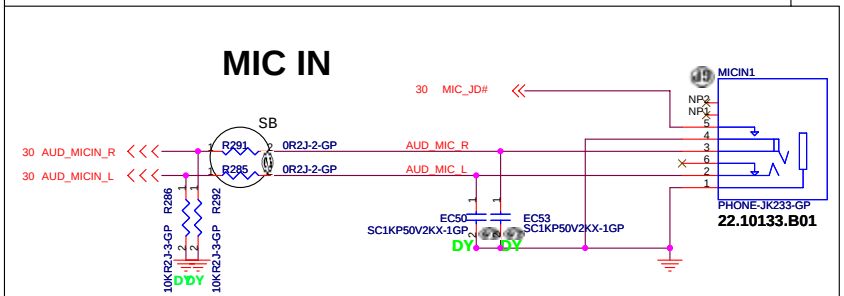
Internal Microphone



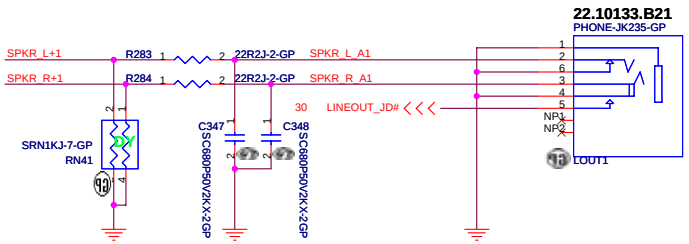
Internal Speaker



MIC IN



LINE OUT



UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title	AUDIO AMP AND JACK	
Size	Document Number: Columbia/Tangiz	Rev: SA
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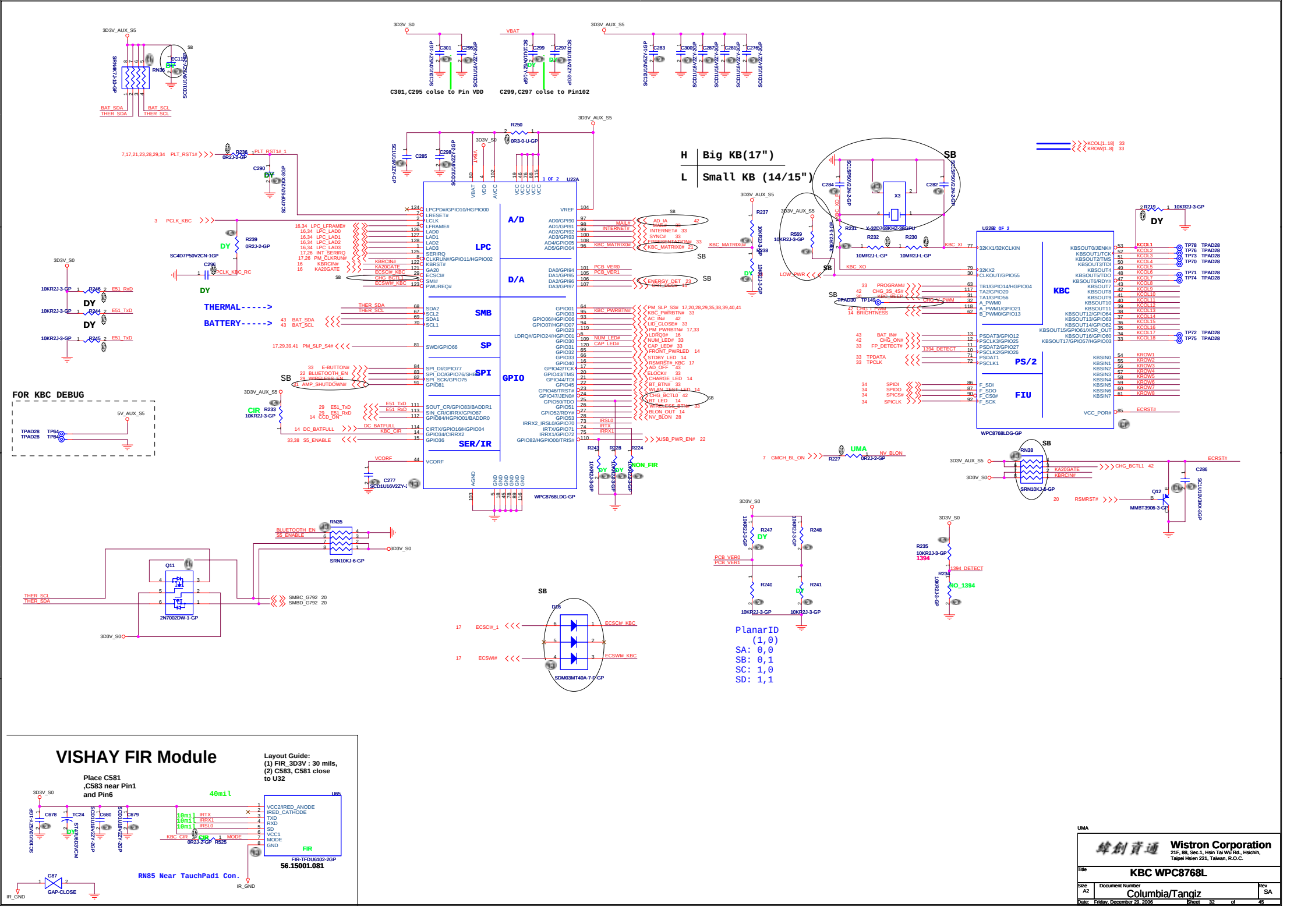
C301,C295 colse to Pin VDD
C299,C297 colse to Pin102
H Big KB(17")
L Small KB (14/15")
FOR KBC DEBUG
THERMAL----->
BATTERY----->
PlanarID
(1,0)
SA: 0,0
SB: 0,1
SC: 1,0
SD: 1,1
VISHAY FIR Module
Place C581
,C583 near Pin1
and Pin6
Layout Guide:
(1) FIR_3D3V : 30 mils,
(2) C583, C581 close
to U32
40mil
RN85 Near TauchPad1 Con.
56.15001.081
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
KBC WPC8768L
Columbia/Tangiz
Date: Friday, December 29, 2006
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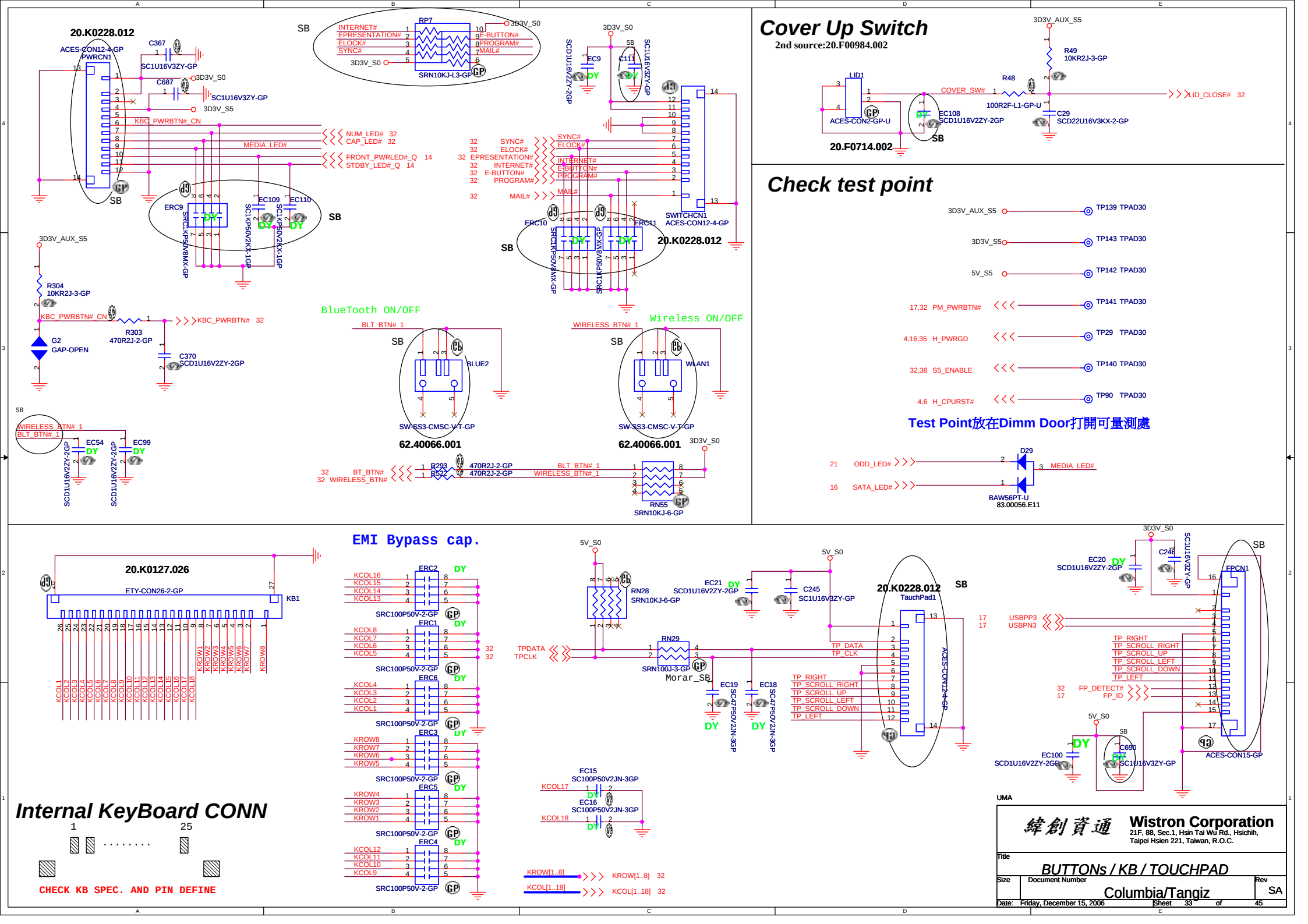
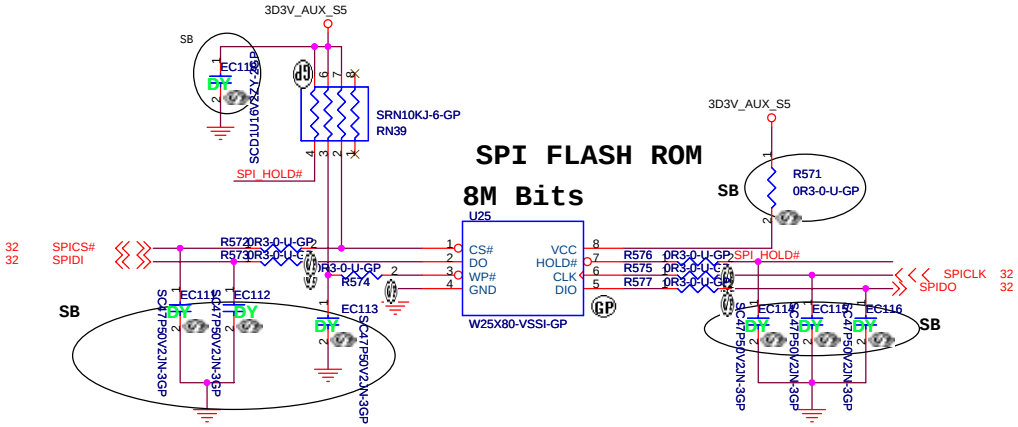
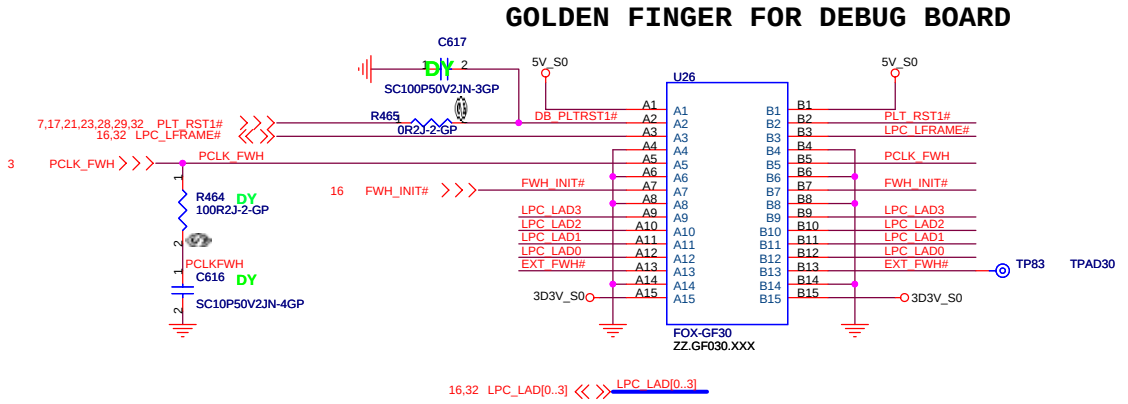

20.K0228.012
ACES-CON12-4-GP
PWRCN1
C367
SC1U16V3ZY-GP
C687
SC1U16V3ZY-GP
3D3V_S0
3D3V_S5
KBC_PWRBTN#_CN
MEDIA_LED#
NUM_LED# 32
CAP_LED# 32
FRONT_PWRLED#_Q 14
STDBY_LED#_Q 14
SB
ERC9
SRC1KP50V8MX-GP
EC109
EC110
SC1KP50V2KX-1GP
SC1KP50V2KX-1GP
3D3V_AUX_S5
R304
10KR2J-3-GP
KBC_PWRBTN#_CN
R303
470R2J-2-GP
KBC_PWRBTN# 32
G2
GAP-OPEN
C370
SCD1U16V2ZY-2GP
WIRELESS_BTN# 1
BLT_BTN# 1
EC54
EC99
SCD1U16V2ZY-2GP
SCD1U16V2ZY-2GP
RP7
INTERNET#
EPRESENTATION#
ELOCK#
SYNC#
E-BUTTON#
PROGRAM#
MAIL#
SRN10KJ-L3-GP
SCD1U16V2ZY-2GP
EC9
C111
SC1U16V3ZY-GP
SYNC#
ELOCK#
INTERNET#
E-BUTTON#
PROGRAM#
MAIL#
SWITCHCN1
ACES-CON12-4-GP
ERC10
ERC11
SRC1KP50V8MX-GP
SRC1KP50V8MX-GP
20.K0228.012
BlueTooth ON/OFF
BLT_BTN# 1
BLUE2
SW-SS3-CMSC-V-T-GP
62.40066.001
Wireless ON/OFF
WIRELESS_BTN# 1
WLAN1
SW-SS3-CMSC-V-T-GP
62.40066.001
3D3V_S0
BT_BTN# 32
WIRELESS_BTN# 32
R293
R322
470R2J-2-GP
470R2J-2-GP
BLT_BTN# 1
WIRELESS_BTN# 1
RN55
SRN10KJ-6-GP
Cover Up Switch
2nd source:20.F00984.002
3D3V_AUX_S5
R49
10KR2J-3-GP
LID1
ACES-CON2-GP-U
COVER_SW#
R48
100R2F-L1-GP-U
LID_CLOSE# 32
EC108
SCD1U16V2ZY-2GP
C29
SCD22U16V3KX-2-GP
20.F0714.002
SB
Check test point
3D3V_AUX_S5 TP139 TPAD30
3D3V_S5 TP143 TPAD30
5V_S5 TP142 TPAD30
17,32 PM_PWRBTN# TP141 TPAD30
4,16,35 H_PWRGD TP29 TPAD30
32,38 S5_ENABLE TP140 TPAD30
4,6 H_CPURST# TP90 TPAD30
Test Point放在Dimm Door打開可量測處
21 ODD_LED#
16 SATA_LED#
D29
MEDIA_LED#
BAW56PT-U
83.00056.E11
20.K0127.026
ETY-CON26-2-GP
KB1
KCOL1
KCOL2
KCOL3
KCOL4
KCOL5
KCOL6
KCOL7
KCOL8
KCOL9
KCOL10
KCOL11
KCOL12
KCOL13
KCOL14
KCOL15
KCOL16
KCOL17
KCOL18
KROW1
KROW2
KROW3
KROW4
KROW5
KROW6
KROW7
KROW8
EMI Bypass cap.
ERC2
ERC1
ERC6
ERC3
ERC5
ERC4
SRC100P50V-2-GP
5V_S0
RN28
SRN10KJ-6-GP
EC21
SCD1U16V2ZY-2GP
C245
SC1U16V3ZY-GP
20.K0228.012
TauchPad1
ACES-CON24-GP
RN29
SRN100J-3-GP
Morar_SB
TPDATA
TPCLK
TP_DATA
TP_CLK
TP_RIGHT
TP_SCROLL_RIGHT
TP_SCROLL_UP
TP_SCROLL_LEFT
TP_SCROLL_DOWN
TP_LEFT
EC19
EC18
SC47P50V2JN-3GP
EC15
SC100P50V2JN-3GP
EC16
SC100P50V2JN-3GP
KROW[1..8] 32
KCOL[1..18] 32
3D3V_S0
EC20
SCD1U16V2ZY-2GP
C246
SC1U16V2ZY-GP
FPCN1
ACES-CON15-GP
USBPP3
USBPN3
FP_DETECT#
FP_ID
EC100
SCD1U16V2ZY-2GP
C690
SC1U16V3ZY-GP
Internal KeyBoard CONN
1
25
CHECK KB SPEC. AND PIN DEFINE
UMA
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
BUTTONs / KB / TOUCHPAD
Size
Document Number
Columbia/Tangiz
Rev
SA
Date: Friday, December 15, 2006
Sheet 33 of 45





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Title: BIOS		
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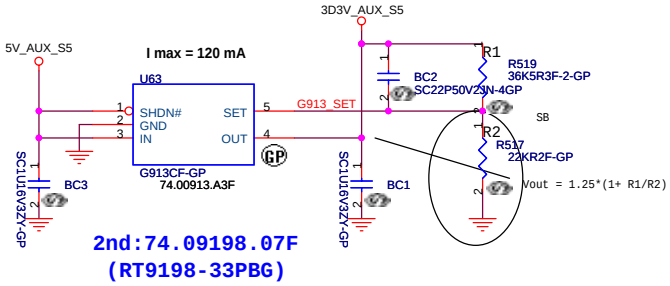
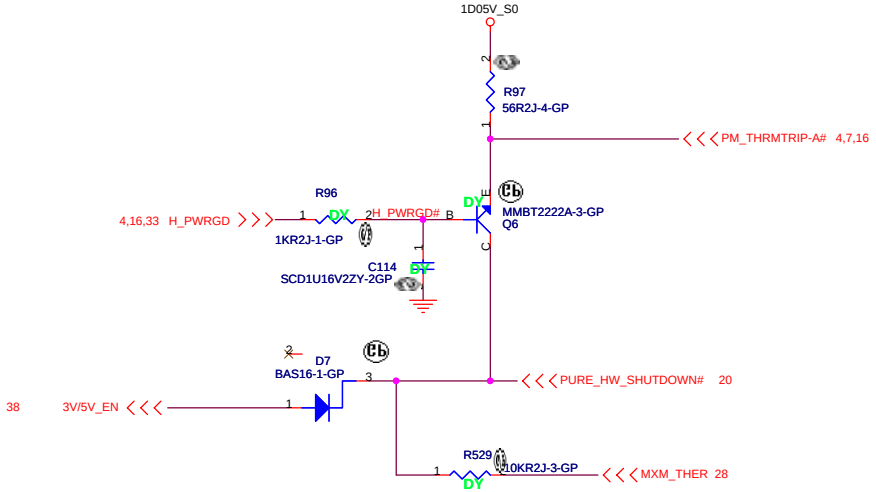
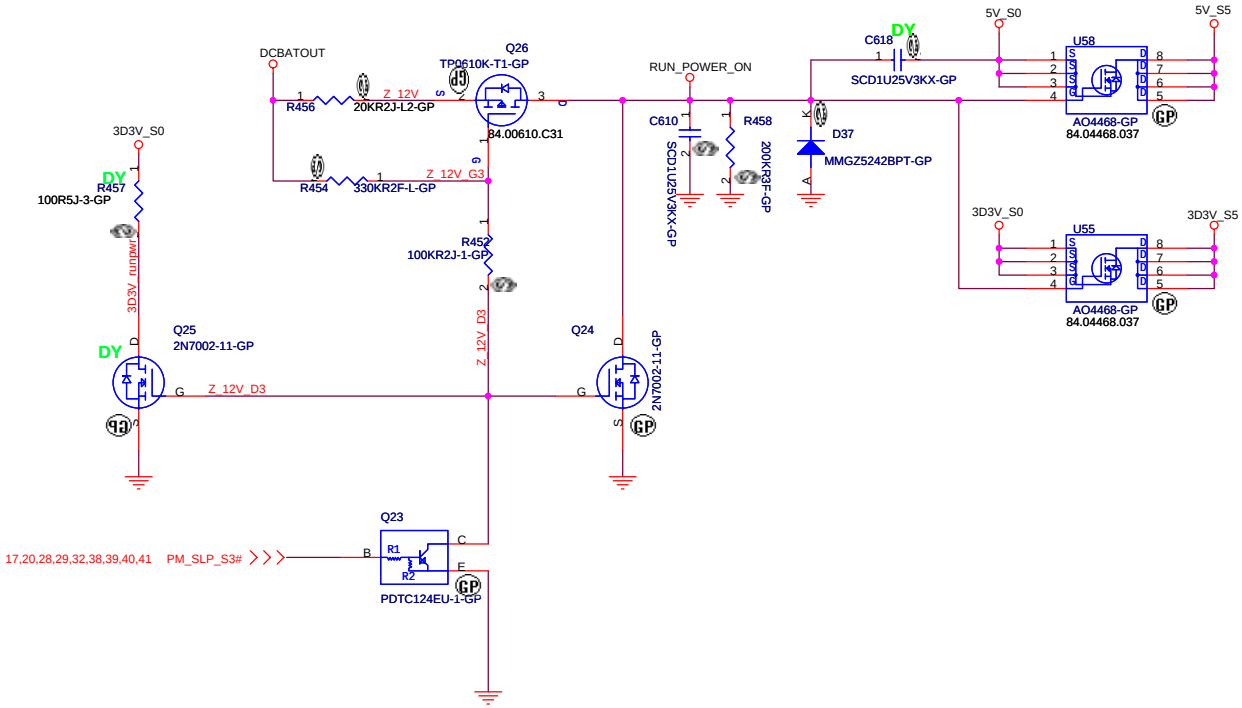
Aux Power 3D3V_AUX_S5





Run Power



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Taipei Hsien 221, Taiwan, R.O.C.

Title: RUN POWER and 3D3V_AUX_S5

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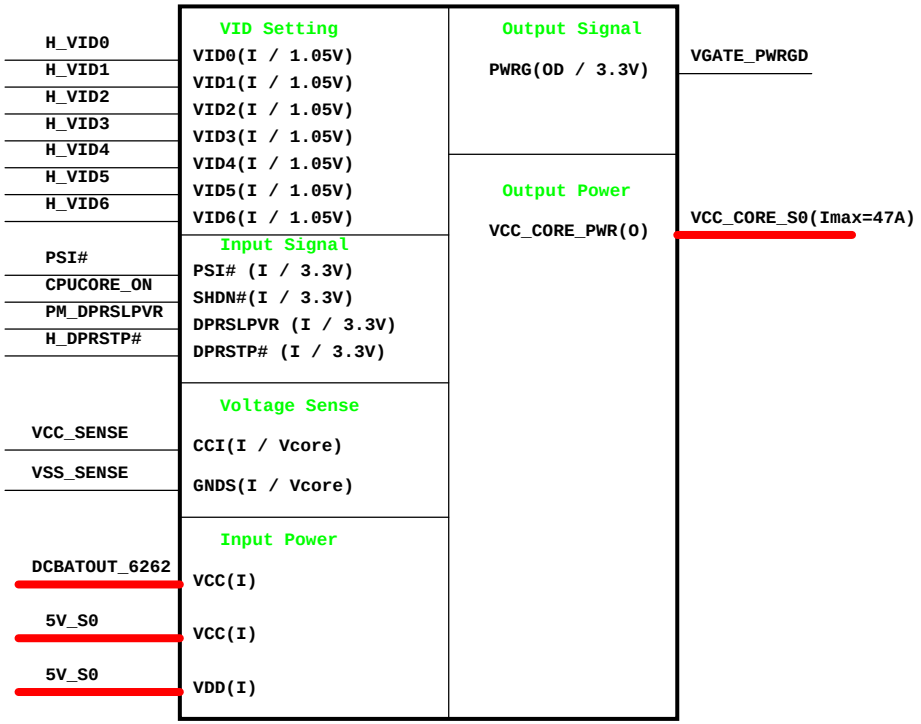
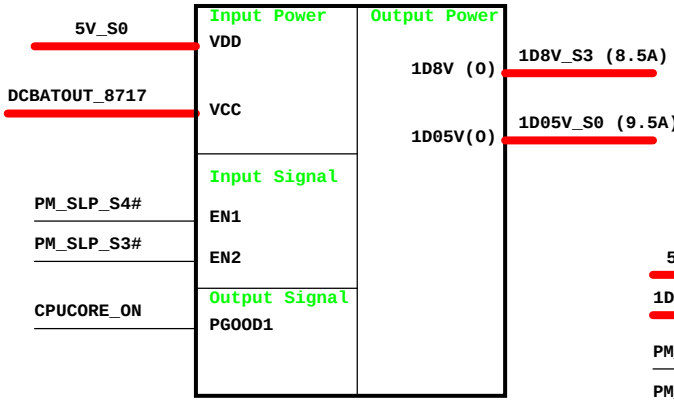
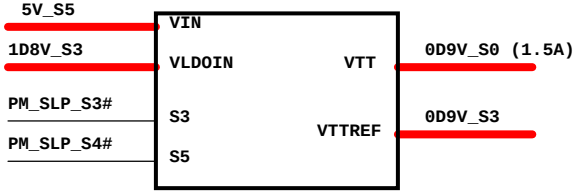
CPU_CORE
MAX8770



MAX8717
1D8V/1D05V

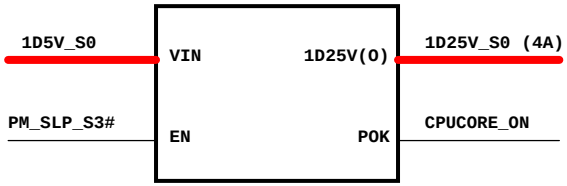


0D9V_S0



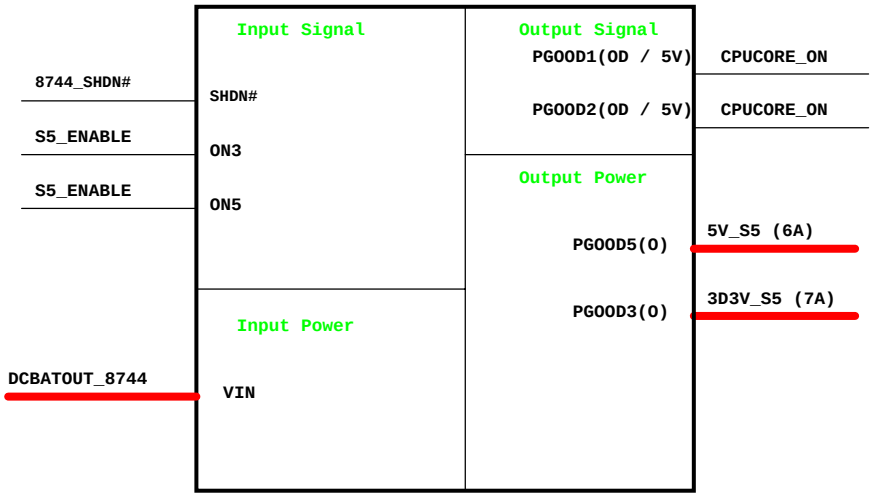
TPS51100

1D25V_S0

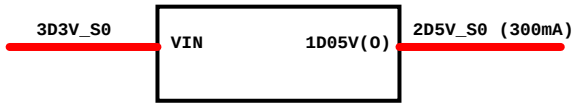


APL5915

MAX8744
5V/3D3V

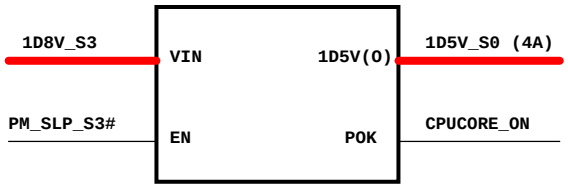


2D5V_S0



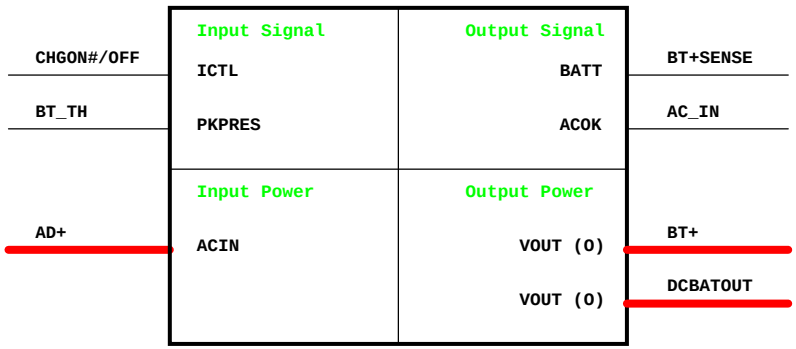
APL5308

1D5V_S0



APL5912

Charger ISL6255



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Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Block Diagram

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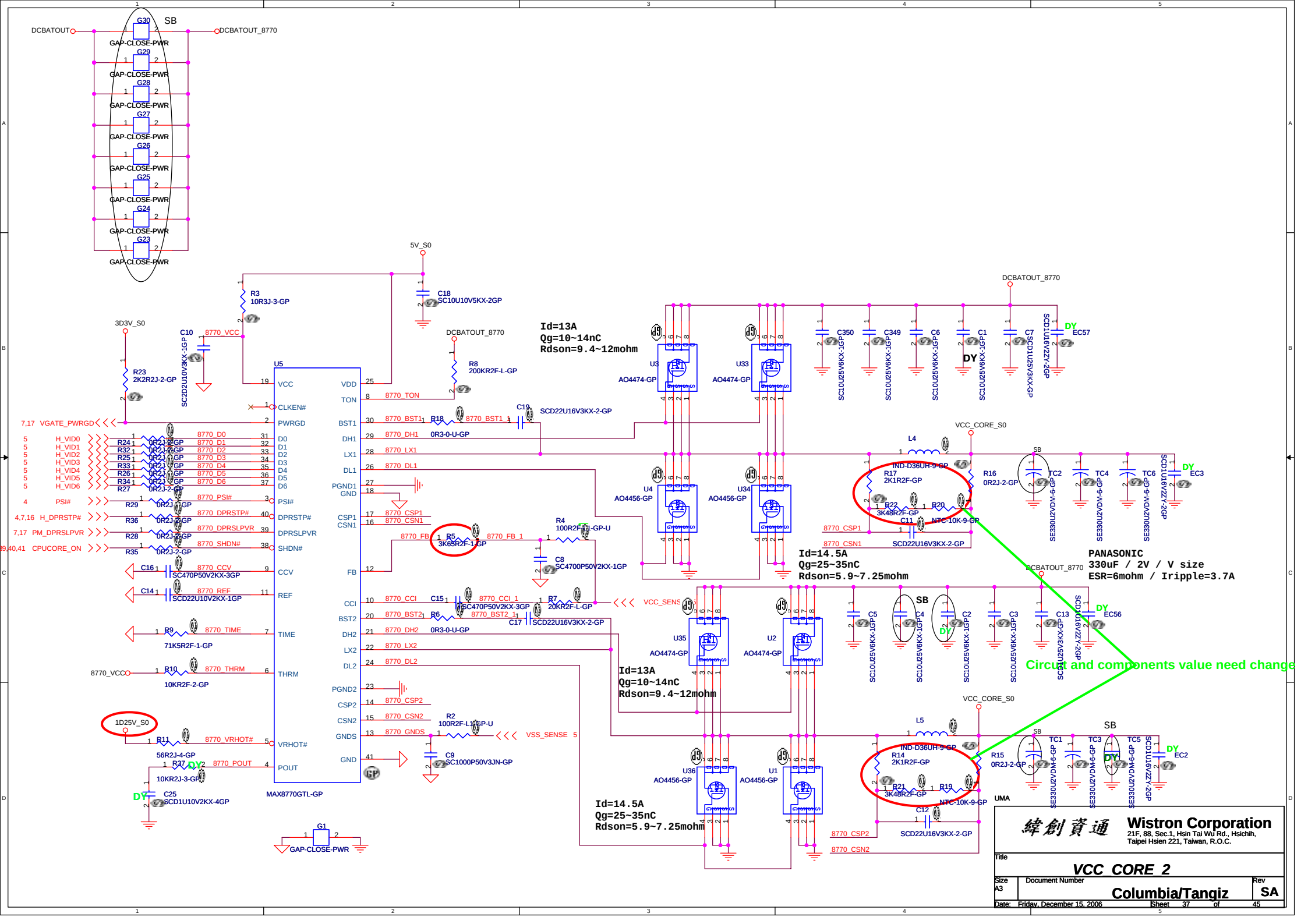
DCBATOUT
DCBATOUT_8770
SB
G30
G29
G28
G27
G26
G25
G24
G23
GAP-CLOSE-PWR
5V_S0
3D3V_S0
1D25V_S0
8770_VCC
R3
10R3J-3-GP
C18
SC10U10V5KX-2GP
C10
SC2D2U10V3KX-1GP
R23
2K2R2J-2-GP
U5
MAX8770GTL-GP
VCC
CLKEN#
PWRGD
D0
D1
D2
D3
D4
D5
D6
PSI#
DPRSTP#
DPRSLPVR
SHDN#
CCV
REF
TIME
THRM
VRHOT#
POUT
VDD
TON
BST1
DH1
LX1
DL1
PGND1
GND
CSP1
CSN1
FB
CCI
BST2
DH2
LX2
DL2
PGND2
CSP2
CSN2
GNDS
R8
200KR2F-L-GP
C19
SCD22U16V3KX-2-GP
R18
0R3-0-U-GP
R4
100R2F-L1-GP-U
R5
3K65R2F-1-GP
C8
SC4700P50V2KX-1GP
C15
SC470P50V2KX-3GP
R6
C17
R7
20KR2F-L-GP
R2
100R2F-L1-GP-U
C9
SC1000P50V3JN-GP
R9
71K5R2F-1-GP
R10
10KR2F-2-GP
R11
56R2J-4-GP
R37
10KR2J-3-GP
C25
SCD1U10V2KX-4GP
G1
Id=13A
Qg=10~14nC
Rdson=9.4~12mohm
U3
U33
U4
U34
AO4474-GP
AO4456-GP
L4
IND-D36UH-9-GP
R17
2K1R2F-GP
R22
3K48R2F-GP
R20
NTC-10K-9-GP
C11
R16
0R2J-2-GP
TC2
TC4
TC6
SE330U2VDM-6-GP
EC3
Id=14.5A
Qg=25~35nC
Rdson=5.9~7.25mohm
PANASONIC
330uF / 2V / V size
ESR=6mohm / Iripple=3.7A
U35
U2
U36
U1
L5
R14
2K1R2F-GP
R21
3K48R2F-GP
R19
NTC-10K-9-GP
C12
R15
0R2J-2-GP
TC1
TC3
TC5
EC2
EC56
EC57
C5
C4
C2
C3
C13
C350
C349
C6
C1
C7
SCD1U25V3KX-GP
SCD1U16V2ZY-2GP
VCC_CORE_S0
DCBATOUT_8770
VCC_SENS
VSS_SENSE
8770_CSP1
8770_CSN1
8770_CSP2
8770_CSN2
Circuit and components value need change
UMA
DY
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
VCC_CORE_2
Size
A3
Document Number
Columbia/Tangiz
Rev
SA
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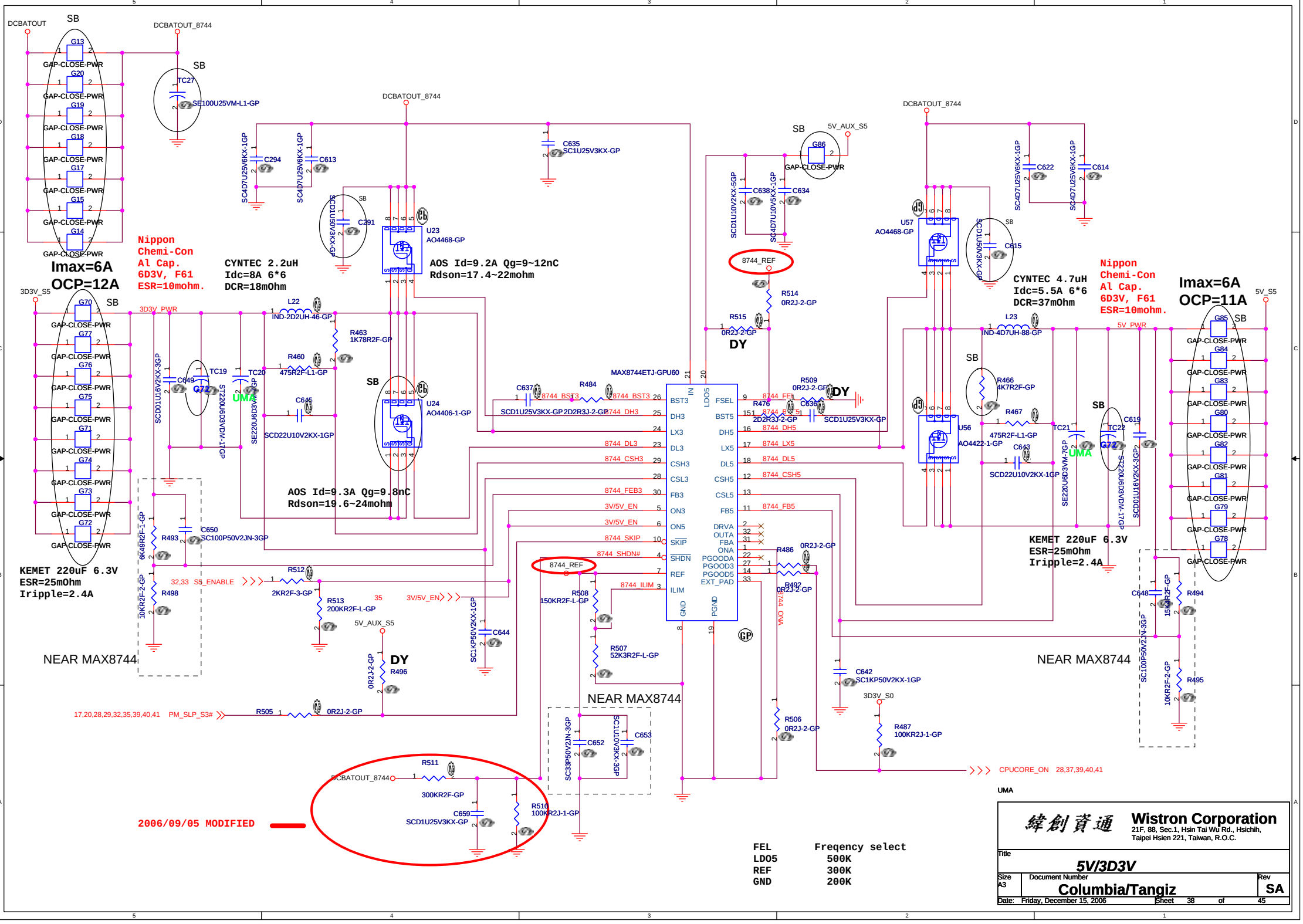
DCBATOUT
SB
DCBATOUT_8744
G13
G20
G19
G18
G17
G15
G14
GAP-CLOSE-PWR
TC27
SE100U25VM-L1-GP
Imax=6A
OCP=12A
Nippon
Chemi-Con
Al Cap.
6D3V, F61
ESR=10mohm.
CYNTEC 2.2uH
Idc=8A 6*6
DCR=18mOhm
AOS Id=9.2A Qg=9~12nC
Rdson=17.4~22mohm
C294
C613
C635
SC1U25V3KX-GP
C291
U23
AO4468-GP
3D3V_S5
G70
G77
G76
G75
G71
G74
G73
G72
3D3V_PWR
L22
IND-2D2UH-46-GP
R463
1K78R2F-GP
R460
475R2F-L1-GP
C649
TC19
TC20
G72
UMA
SE220U6D3VDM-17GP
C645
SCD22U10V2KX-1GP
U24
AO4406-1-GP
AOS Id=9.3A Qg=9.8nC
Rdson=19.6~24mohm
KEMET 220uF 6.3V
ESR=25mOhm
Iripple=2.4A
NEAR MAX8744
R493
C650
SC100P50V2JN-3GP
R498
R512
2KR2F-3-GP
32,33 S5_ENABLE
R513
200KR2F-L-GP
35 3V/5V_EN
5V_AUX_S5
R496
DY
C644
SC1KP50V2KX-1GP
17,20,28,29,32,35,39,40,41 PM_SLP_S3#
R505
0R2J-2-GP
MAX8744ETJ-GPU60
BST3
DH3
LX3
DL3
CSH3
CSL3
FB3
ON3
ON5
SKIP
SHDN
REF
ILIM
GND
IN
LDO5
FSEL
BST5
DH5
LX5
DL5
CSH5
CSL5
FB5
DRVA
OUTA
FBA
ONA
PGOODA
PGOOD3
PGOOD5
EXT_PAD
PGND
8744_BST3
8744_DH3
8744_DL3
8744_CSH3
8744_FEB3
3V/5V_EN
8744_SKIP
8744_SHDN#
8744_ILIM
8744_FE5
8744_BST5
8744_DH5
8744_LX5
8744_DL5
8744_CSH5
8744_FB5
R484
C637
SCD1U25V3KX-GP
2D2R3J-2-GP
R509
0R2J-2-GP
R476
C636
SCD1U25V3KX-GP
R486
0R2J-2-GP
R492
0R2J-2-GP
8744_CNA
8744_REF
R508
150KR2F-L-GP
R507
52K3R2F-L-GP
C642
SC1KP50V2KX-1GP
3D3V_S0
R487
100KR2J-1-GP
R506
0R2J-2-GP
CPUCORE_ON 28,37,39,40,41
R511
300KR2F-GP
C659
SCD1U25V3KX-GP
R510
100KR2J-1-GP
2006/09/05 MODIFIED
SC33P50V2JN-3GP
C652
SC1U10V3KX-GP
C653
FEL Freqency select
LDO5 500K
REF 300K
GND 200K
5V_AUX_S5
G86
GAP-CLOSE-PWR
SCD1U10V2KX-5GP
C638
C634
SC4D7U10V5KX-1GP
U57
AO4468-GP
C622
C614
C615
CYNTEC 4.7uH
Idc=5.5A 6*6
DCR=37mOhm
L23
IND-4D7UH-88-GP
R466
4K7R2F-GP
R467
475R2F-L1-GP
C643
SCD22U10V2KX-1GP
U56
AO4422-1-GP
TC21
TC22
C619
SCD01U16V2KX-3GP
5V_PWR
Imax=6A
OCP=11A
G85
G84
G83
G80
G82
G81
G79
G78
KEMET 220uF 6.3V
ESR=25mOhm
Iripple=2.4A
NEAR MAX8744
C648
R494
R495
UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
5V/3D3V
Size A3
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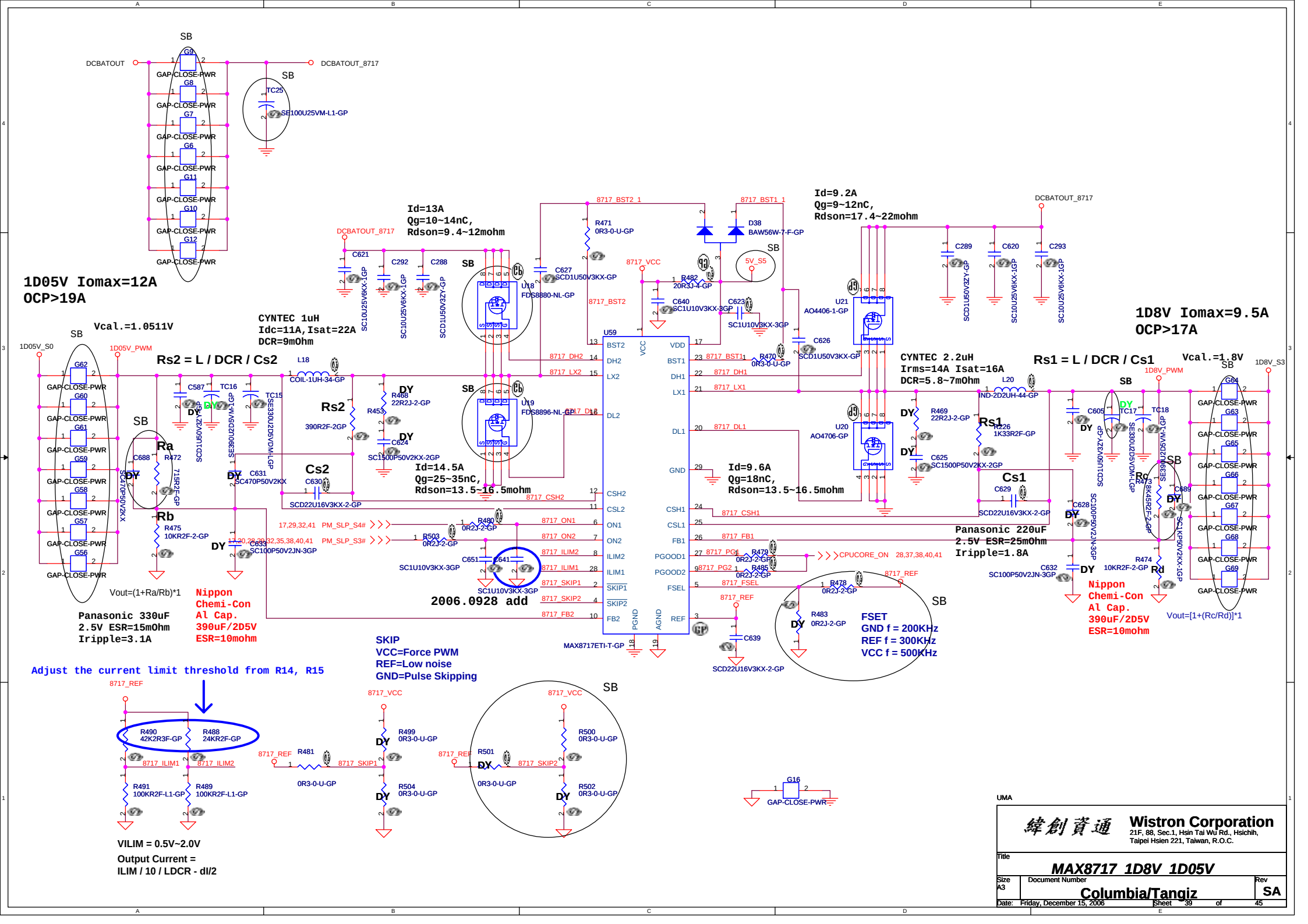
1D05V Iomax=12A
OCP>19A
Vcal.=1.0511V
Rs2 = L / DCR / Cs2
CYNTEC 1uH
Idc=11A,Isat=22A
DCR=9mOhm
Id=13A
Qg=10~14nC,
Rdson=9.4~12mohm
Id=14.5A
Qg=25~35nC,
Rdson=13.5~16.5mohm
Id=9.2A
Qg=9~12nC,
Rdson=17.4~22mohm
Id=9.6A
Qg=18nC,
Rdson=13.5~16.5mohm
1D8V Iomax=9.5A
OCP>17A
CYNTEC 2.2uH
Irms=14A Isat=16A
DCR=5.8~7mOhm
Rs1 = L / DCR / Cs1
Vcal.=1.8V
Vout=(1+Ra/Rb)*1
Vout=[1+(Rc/Rd)]*1
Panasonic 330uF
2.5V ESR=15mOhm
Iripple=3.1A
Nippon
Chemi-Con
Al Cap.
390uF/2D5V
ESR=10mohm
Panasonic 220uF
2.5V ESR=25mOhm
Iripple=1.8A
Nippon
Chemi-Con
Al Cap.
390uF/2D5V
ESR=10mohm
2006.0928 add
SKIP
VCC=Force PWM
REF=Low noise
GND=Pulse Skipping
FSET
GND f = 200KHz
REF f = 300KHz
VCC f = 500KHz
Adjust the current limit threshold from R14, R15
VILIM = 0.5V~2.0V
Output Current =
ILIM / 10 / LDCR - dI/2
MAX8717ETI-T-GP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
MAX8717 1D8V 1D05V
Columbia/Tangiz
Size A3
Rev SA
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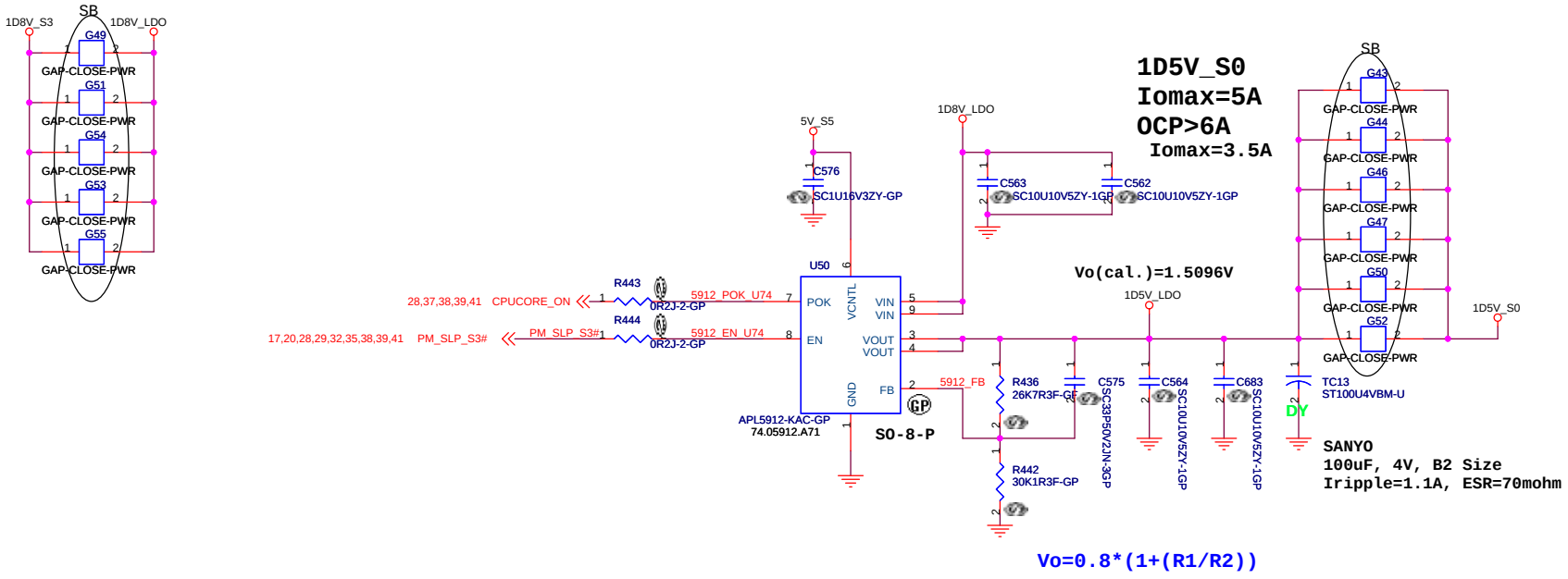

UMA

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title	***APW5912_1D5V***	
Size	Document Number **Columbia/Tangiz**	Rev SA
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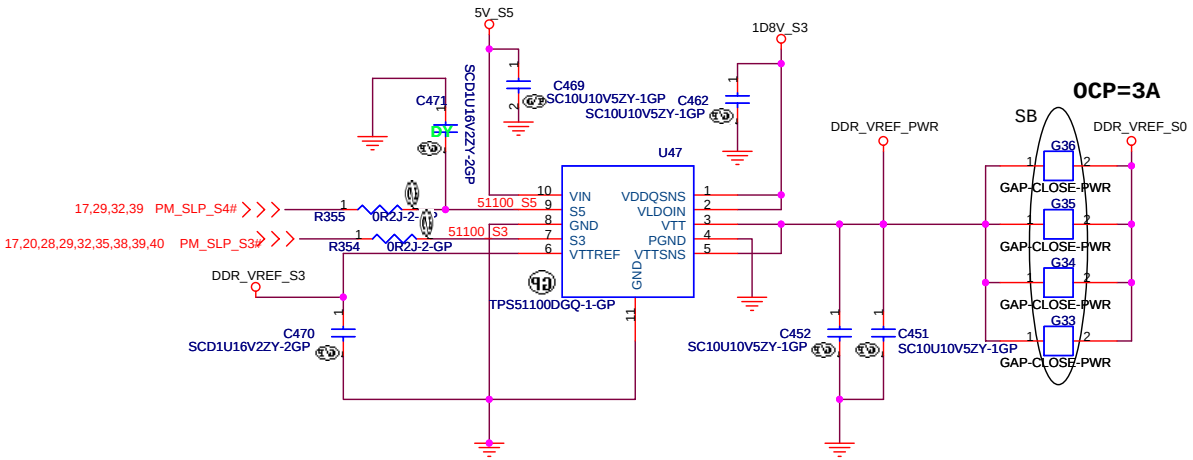
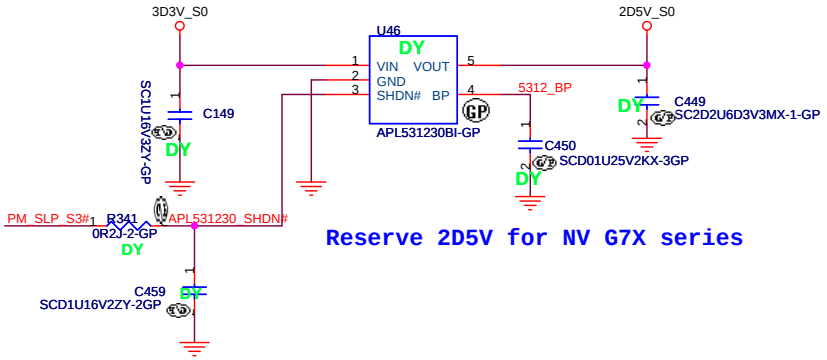
0D9V_S3
Iomax=1.2A

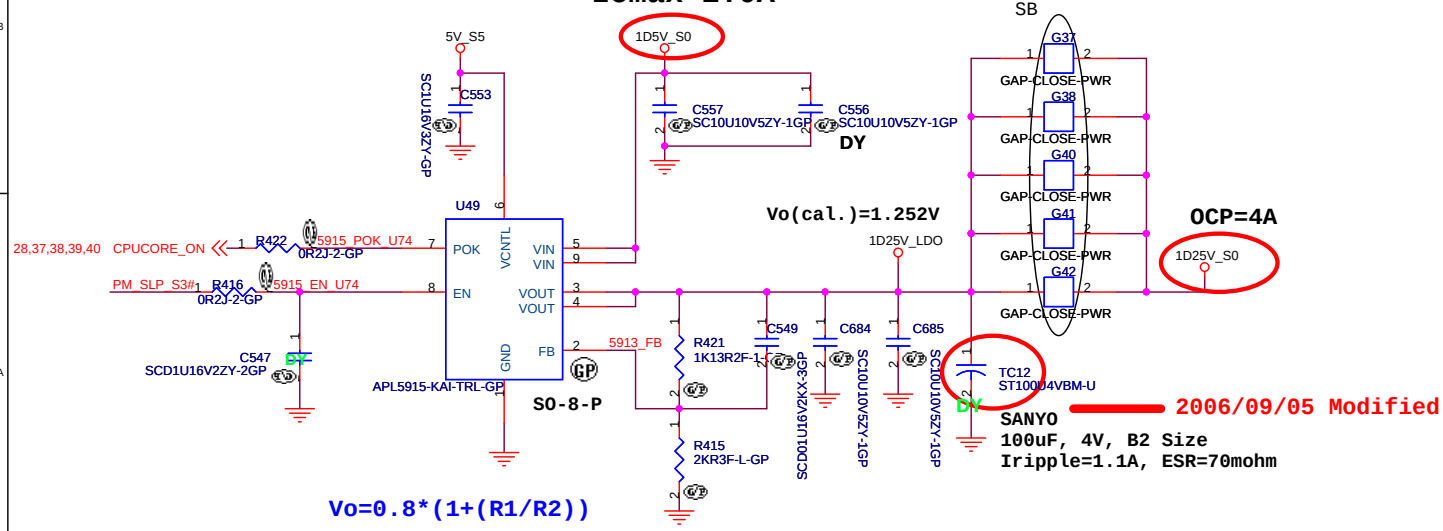


2D5V
Iomax=130mA



Reserve 2D5V for NV G7X series

1D25V_S0
Iomax=2.0A



2006/09/05 Modified

Vo=0.8*(1+(R1/R2))

UMA

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title	1D25V/2D5V//1D05V/0D9V	
Size B	Document Number Columbia/Tangiz	Rev SA
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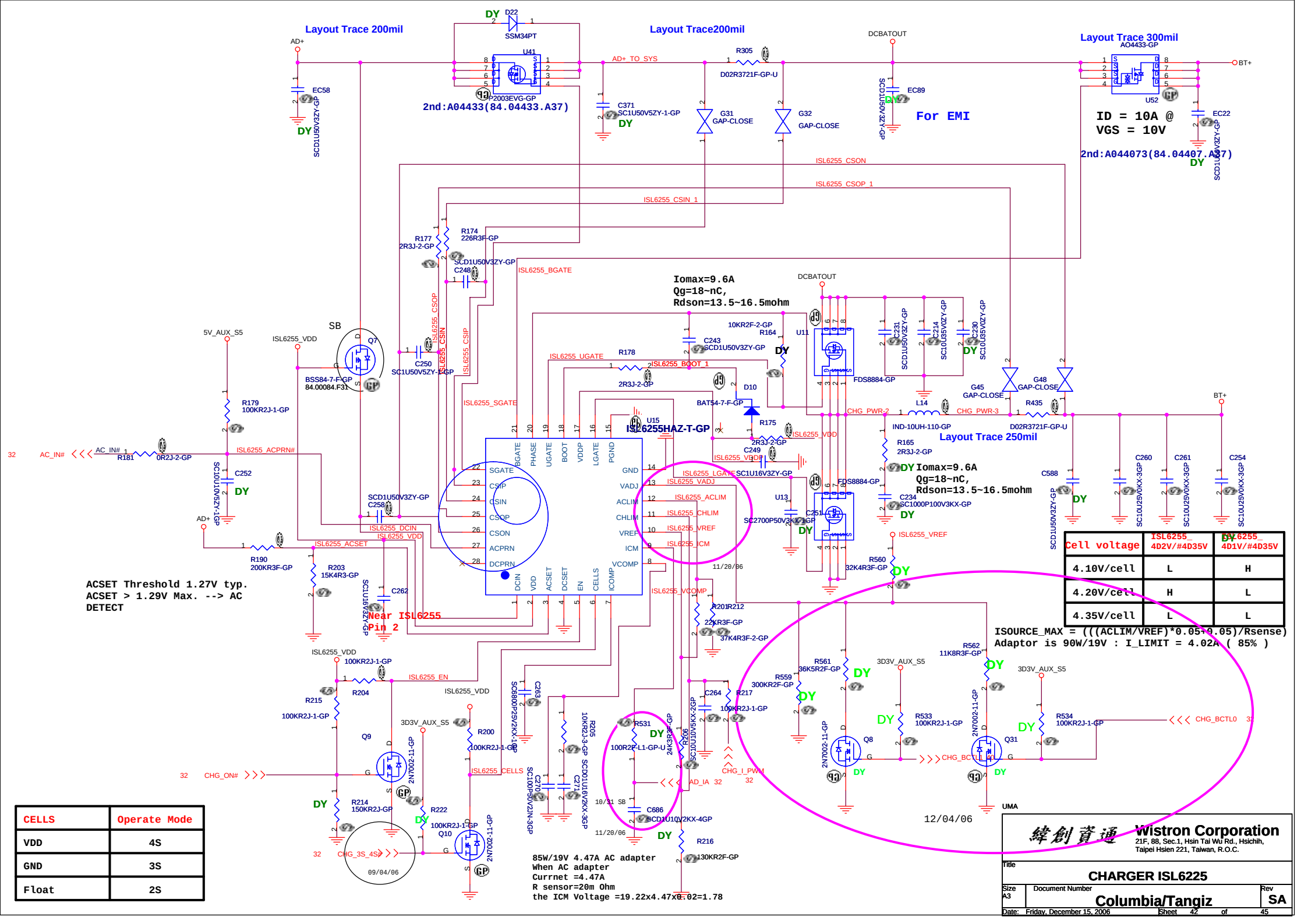

Cell voltage	ISL6255_4D2V/#4D35V	ISL6255_4D1V/#4D35V
4.10V/cell	L	H
4.20V/cell	H	L
4.35V/cell	L	L

CELLS	Operate Mode
VDD	4S
GND	3S
Float	2S

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Title: CHARGER ISL6225

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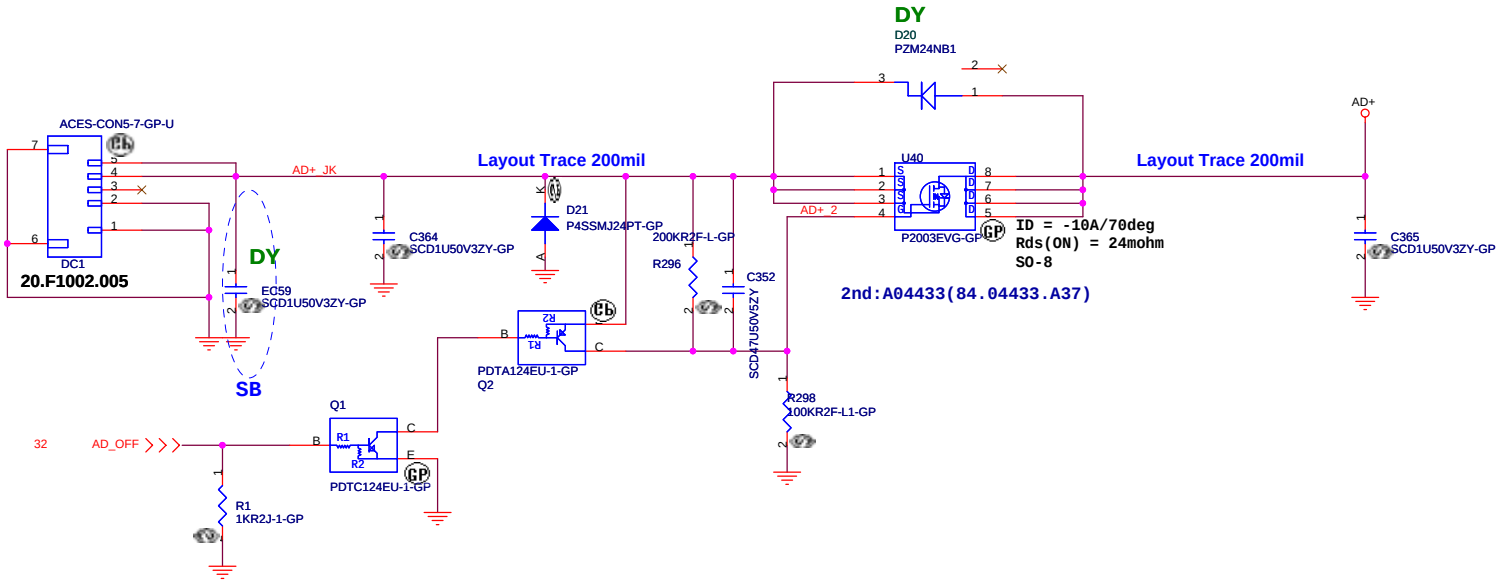
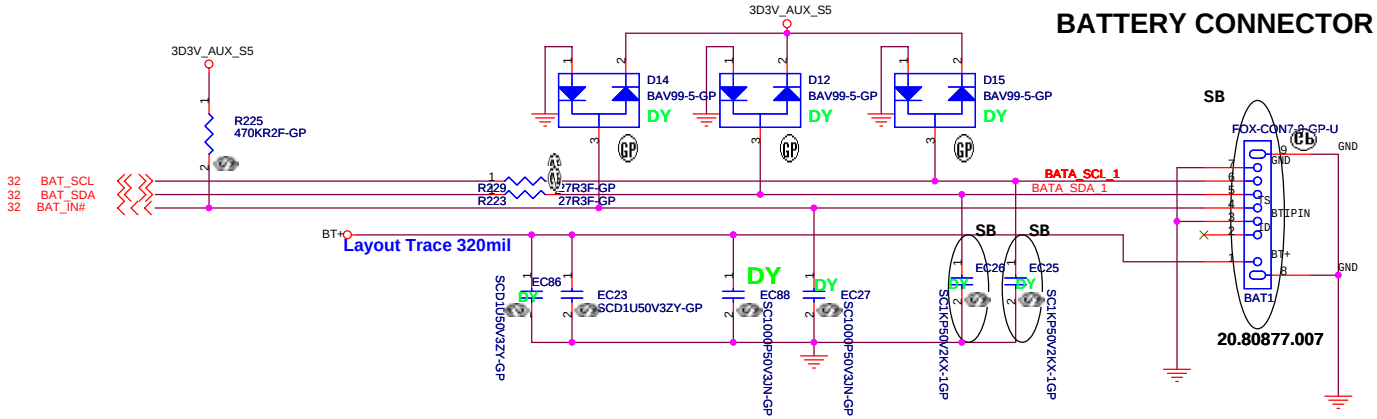
Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



UMA

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Title	AD/BATT CONN	
Size A3	Document Number Columbia/Tangiz	Rev SA
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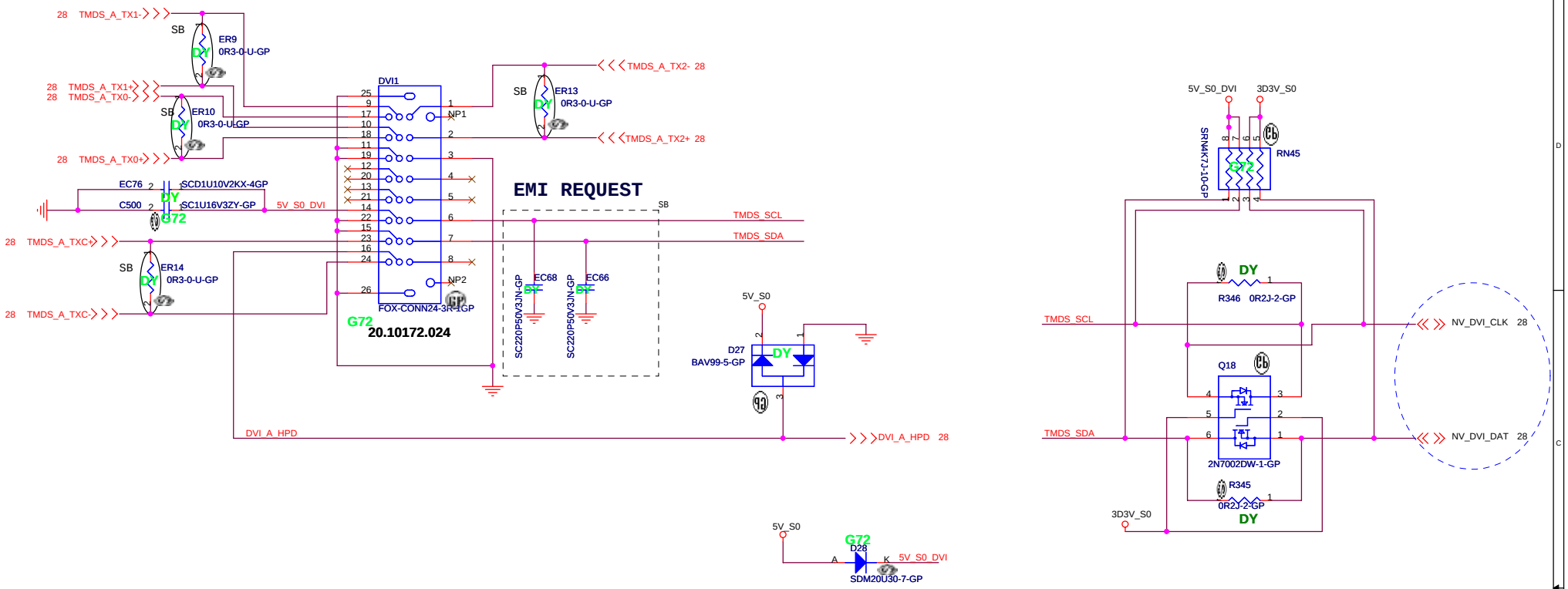

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Title: **DVI CONNECTOR**

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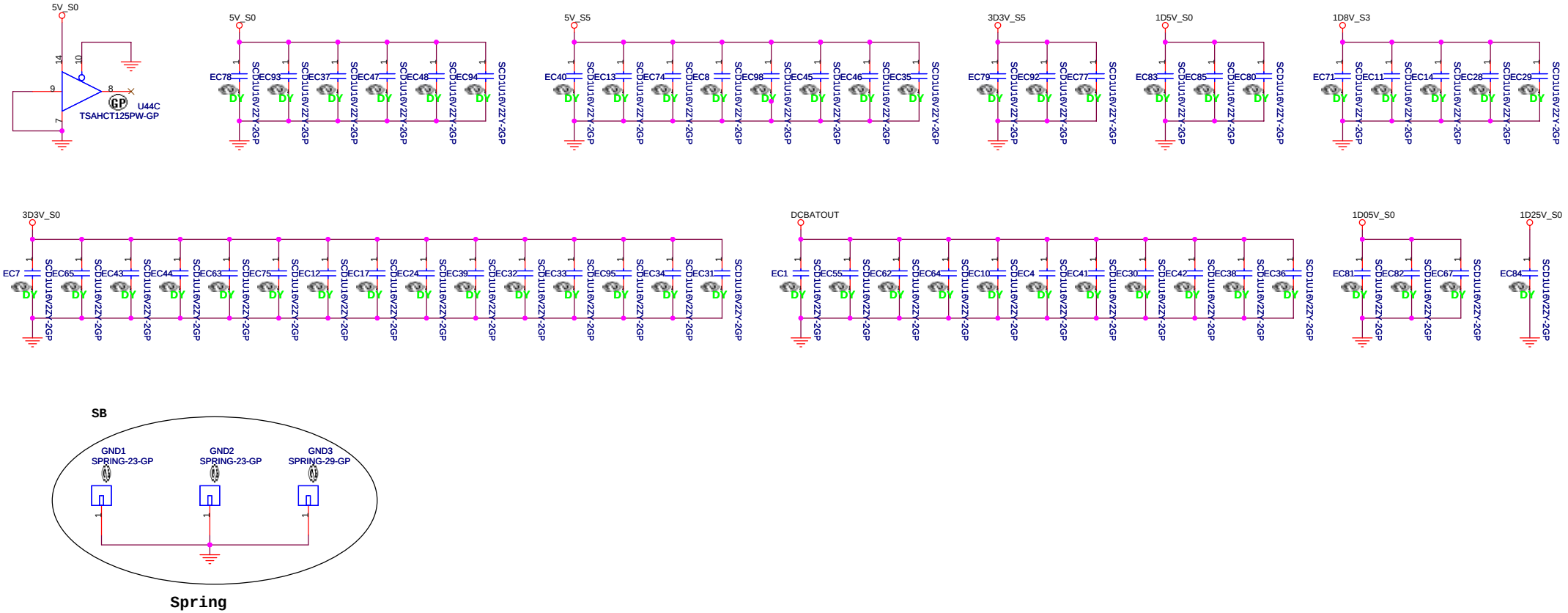

MINI CARD

H3 HOLE — 34.4g502.001
H7 HOLE — 34.4g502.001
H25 HOLE — 34.42Y01.011
H26 HOLE — 34.42Y01.011
H16 HOLE — 34.4G805.001
H17 HOLE — 34.4G805.001
H4 HOLE — 34.42Y01.011
H5 HOLE — 34.42Y01.011
H8 HOLE — 34.42Y01.011
H9 HOLE — 34.42Y01.011

Fan

H24 HOLE — 34.42Y01.011
H6 HOLE — 34.42Y01.011
H12 HOLE — 34.42Y01.011

H15 HOLE, H2 HOLE, H1 HOLE, H20 HOLE, H13 HOLE, H10 HOLE, H19 HOLE, H11 HOLE, H18 HOLE, H21 HOLE, H22 HOLE, H23 HOLE

UMA

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Title: ***EMI/Spring/Boss***

Size | Document Number: **Columbia/Tangiz** | Rev: SA

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