

# Compal confidential

*Los Angeles 10A+/10AG+*

**KTKAE LA-4581P REV4.0 Schematics Document**

Mobile AMD S1G2 /RS780M&RS780MC&RX781/SB700  
2008-12-26 Rev. 4.0

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Issued Date	2008/04/14	Deciphered Date	2009/04/14	Title <b>Cover Sheet</b>		
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Date: Thursday, January 08, 2009				Sheet	1	of 45

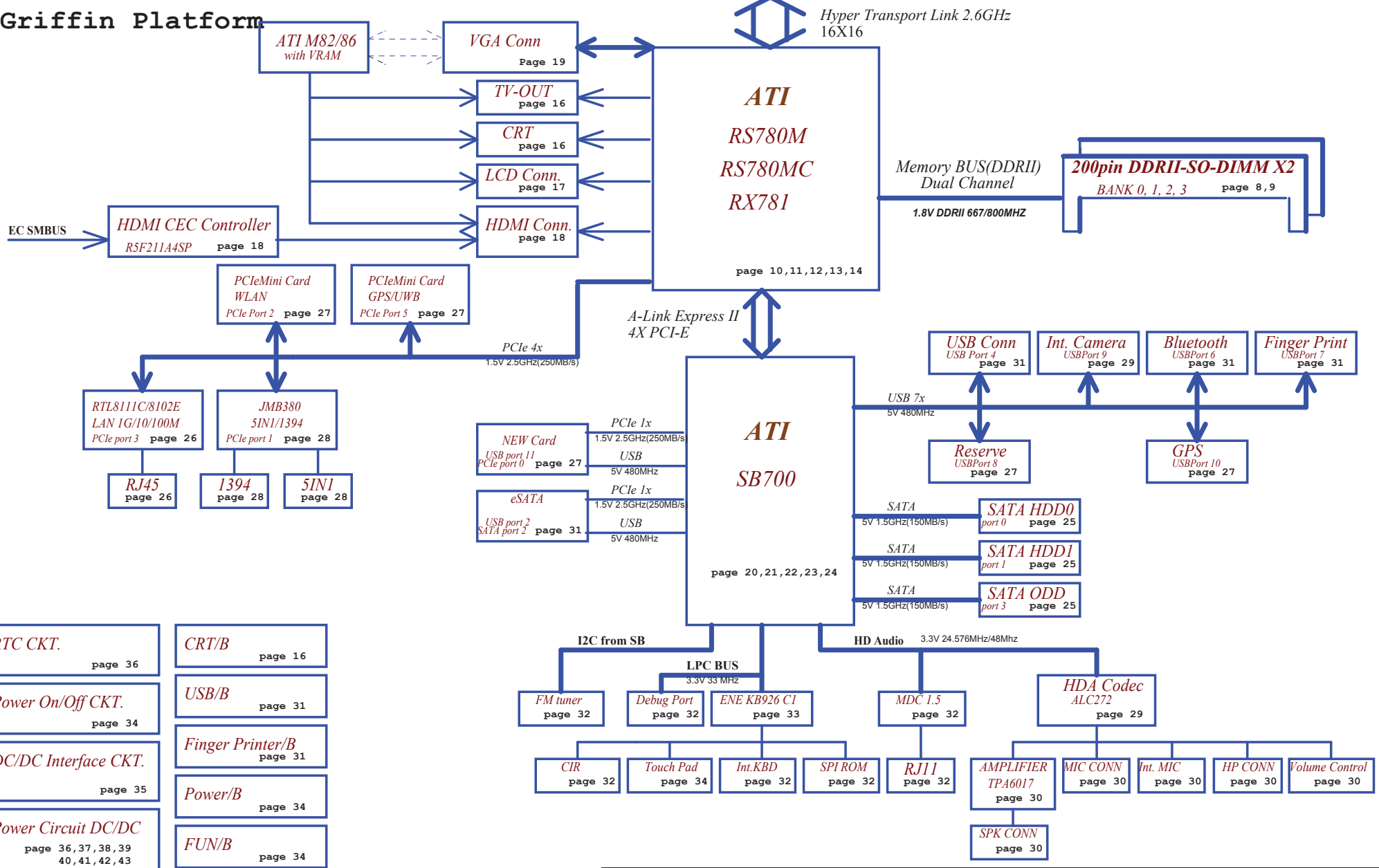
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Model Name : KTKAE

File Name : LA-4581P

## Griffin Platform

Fan Control page 4	<b>AMD SIG2 CPU</b> uFCPGA-638 Package page 4,5,6,7	Thermal Sensor ADM1032ARMZ page 6	Clock Generator SLG8SP626 page 15
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RTC CKT. page 36	CRT/B page 16
Power On/Off CKT. page 34	USB/B page 31
DC/DC Interface CKT. page 35	Finger Printer/B page 31
Power Circuit DC/DC page 36,37,38,39 40,41,42,43	Power/B page 34
	FUN/B page 34
	LED/B page 34

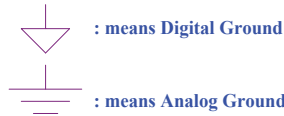
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				<b>Block Diagram</b>	
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**Voltage Rails**    ○ MEANS ON    ✗ MEANS OFF

power plane  State				+5VS +3VS +2.5VS +1.8VS +1.5VS +1.1VS +VGA_CORE +1.2V_HT +CPU_CORE_NB +CPU_CORE_0 +CPU_CORE_1
	+B +3VL +5VL +RTCVC	+5VALW +3VALW +1.2VALW +3V_LAN	+1.8V +0.9V +0.9V	
S0	○	○	○	○
S1	○	○	○	○
S3	○	○	○	✗
S5 S4/AC	○	○	✗	✗
S5 S4/ Battery only	○	✗	✗	✗
S5 S4/AC & Battery don't exist	✗	✗	✗	✗

**Symbol Note :**



@ : means just reserve , no build  
DEBUG@ : means just reserve for debug.

Ⓛ Layout Notes  
UMA@ : means for RS780M.

Item	CPU	NB	VGA	SB
GM@	S1G2	RS780M	NA	SB700
PM@+PM1@	S1G2	RX781	M82/M86	SB700
RV@+PM@	S1G2	RS780M	M82	SB700
GM@	S1G2	RS780MC	NA	SB700

**BTO Option Table**

Function	HDMI			TV-out
description	(Y)			(S)
explain	AMD (UMA)	ATI VGA/B	COMMON	
BTO	IHDMI@	HDMI@	H@	TV@

Function	2nd HDD	LAN		Mini card	RJ11/FM tuner		3G SIM slot
description	(2H)	(E)	(C)	(D2)	(R)	(M)	(G)
explain		10/100M	Giga	Two Crads	RJ11	FM	
BTO	HDD2@	8102E@	8111C@	WLAN@	GPS@	MDC@	3G@

Function	Felica	BLUE TOOTH	CIR	CAMERA & MIC		Finger printer
description	(J)	(B)	(I)	(X)		(F)
explain				CAMERA	MIC	
BTO	FLICA@	BT@	CIR@	CAM@	MIC@	FP@

**I2C / SMBUS ADDRESSING**

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
DDR SO-DIMM 1	A4	1 0 1 0 0 1 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

**EC SM Bus1 address**

Device	HEX	Address
Smart Battery	16H	0001 011X b
HDMI-CEC	34H	0011 010X b
EC KB926C1		

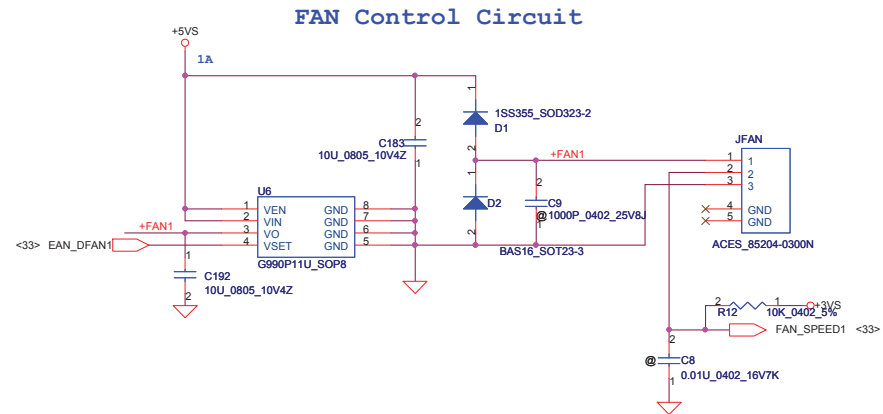
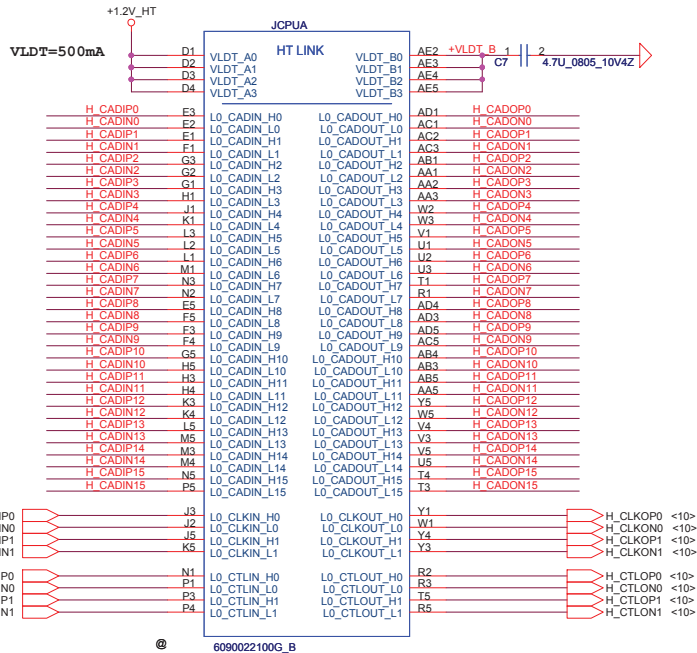
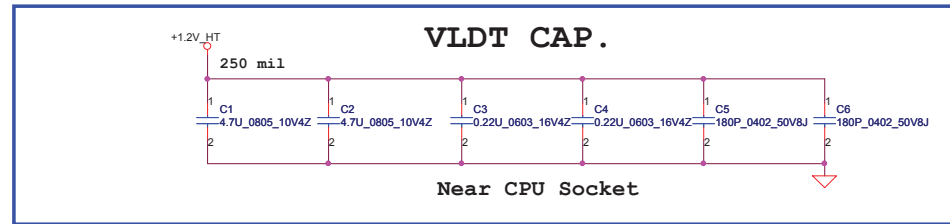
**EC SM Bus2 address**

Device	HEX	Address
AD11032-1 CPU	98H	1001 100X b
AD11032-2 VGA	9AH	1001 101X b
EC KB926C1		
Ext. VGA/B		
CS/B		

**SMBUS Control Table**

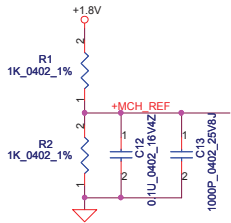
	SOURCE	INVERTER	BATT	CEC	THERMAL SENSOR CPU & ADM1032	SODIMM I / II	CLK CHIP	MINI CARD Slot 2	LCD	HDMI	G-Sensor
SMB_EC_CK1	KB926	✗	V	V	✗	✗	✗	✗	✗	✗	✗
SMB_EC_DA1	KB926	✗	✗	✗	V	✗	✗	✗	✗	✗	✗
SMB_EC_DA2	KB926	✗	✗	✗	V	✗	✗	✗	✗	✗	✗
I2C_CLK	RS780M	✗	✗	✗	✗	✗	✗	✗	V	✗	✗
I2C_DATA	RS780M	✗	✗	✗	✗	✗	✗	✗	✗	V	✗
DDC_CLK0	RS780M	✗	✗	✗	✗	✗	✗	✗	✗	V	✗
DDC_DATA0	RS780M	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗
DDC_CLK1	RS780M	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗
DDC_DATA1	RS780M	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗
SCL0	SB700	✗	✗	✗	✗	V	V	✗	✗	✗	V
SDA0	SB700	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗
SCL1	SB700	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗
SDA1	SB700	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗
SCL2	SB700	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗
SDA2	SB700	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗
SCL3	SB700	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗
SDA3	SB700	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗

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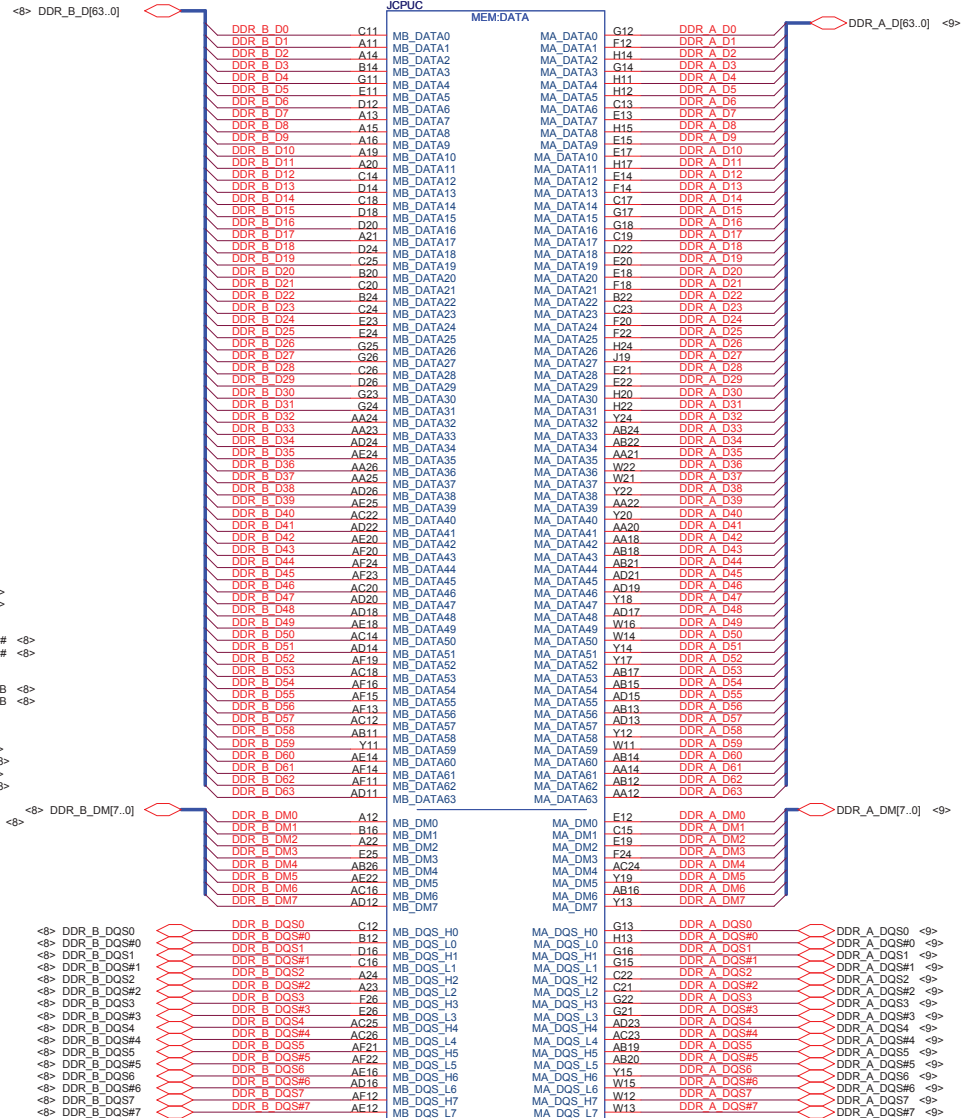
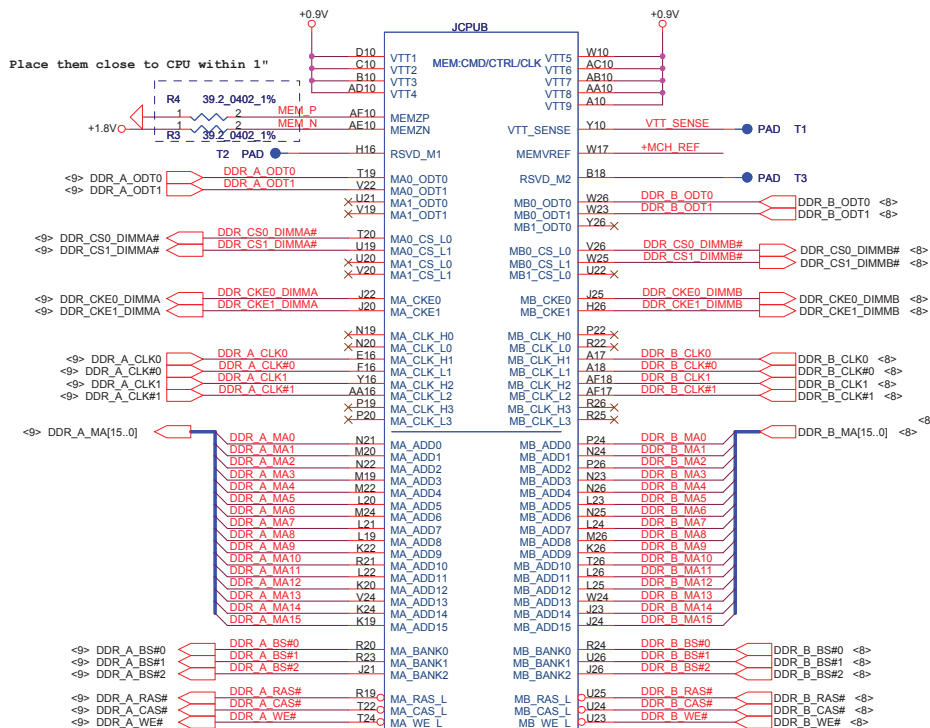
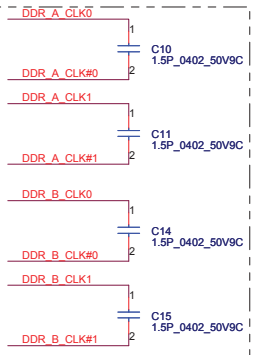


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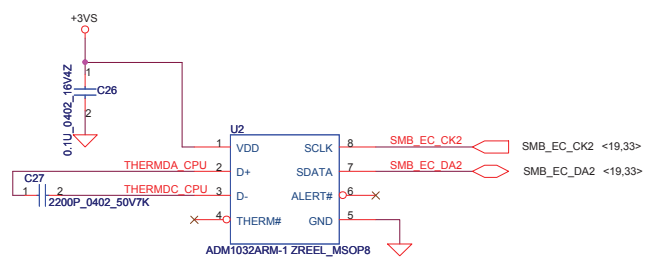
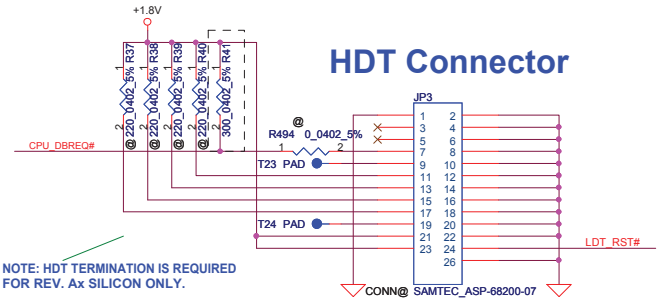
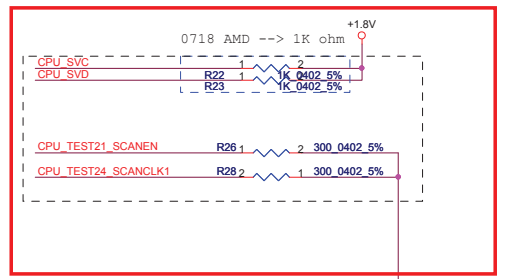
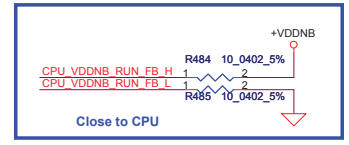
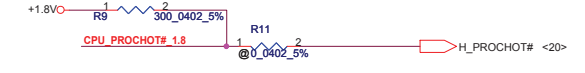
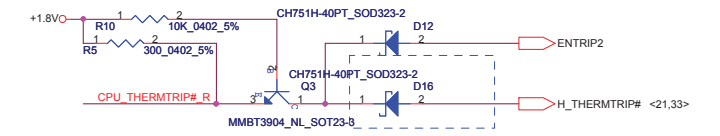
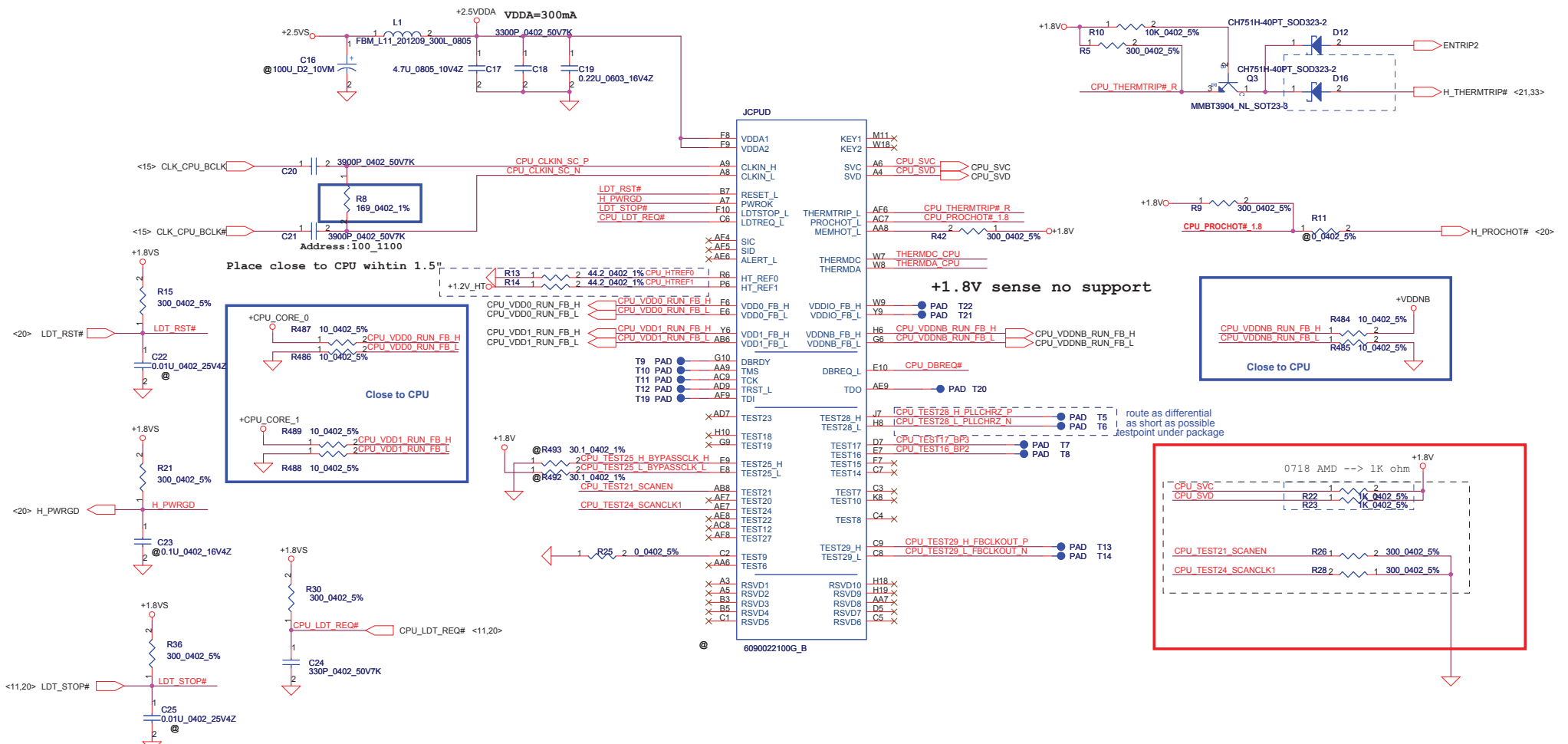
# Processor DDR2 Memory Interface



PLACE CLOSE TO PROCESSOR  
WITHIN 1.5 INCH



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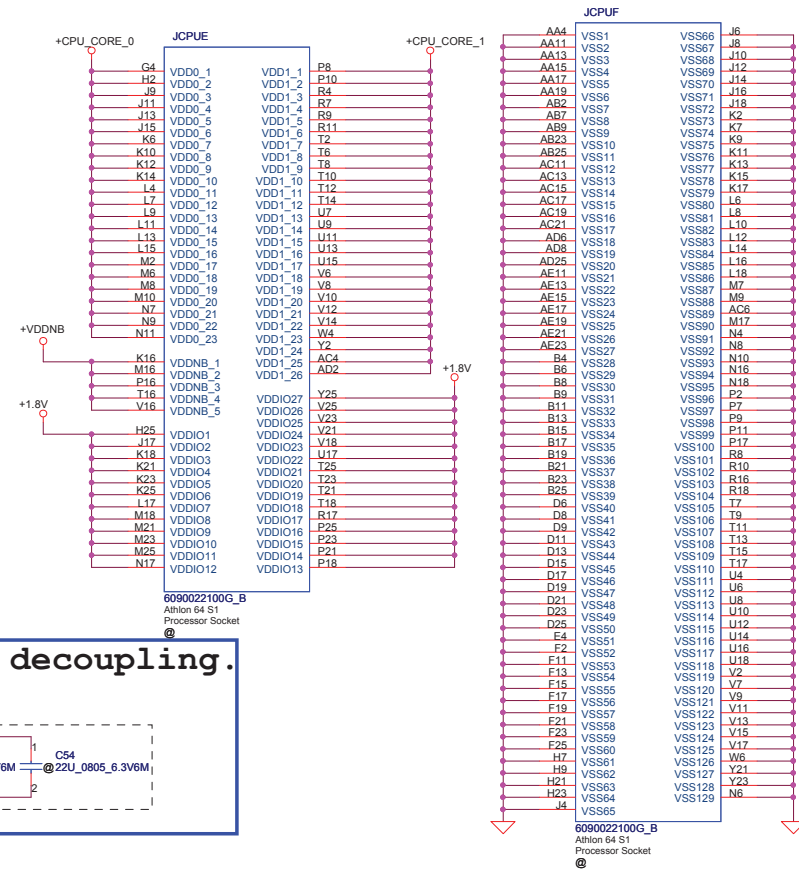
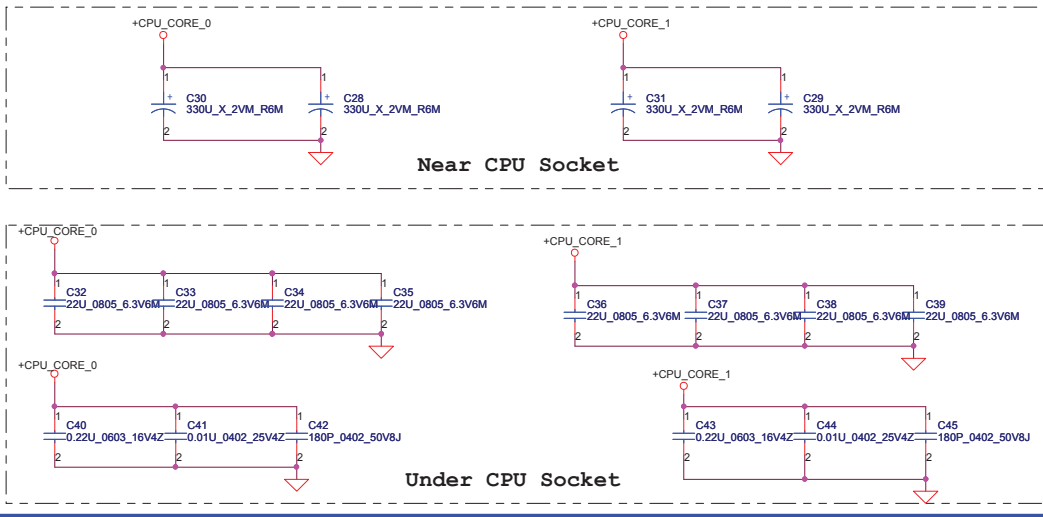


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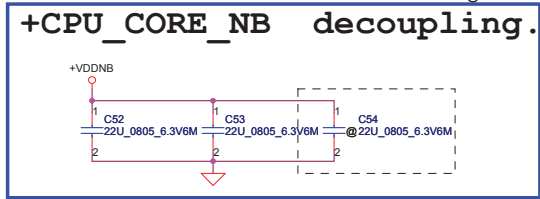
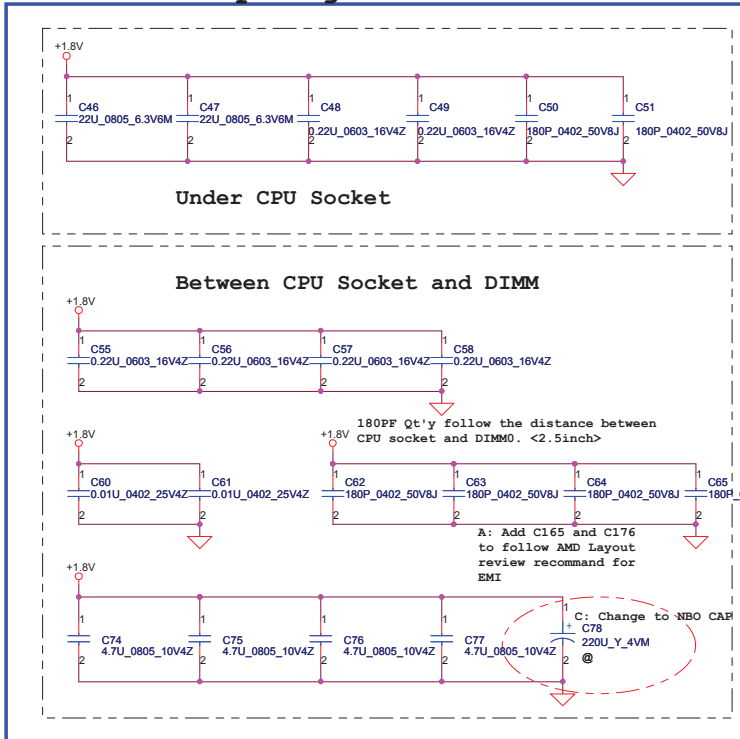
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<b>AMD CPU SIG2 CTRL</b>			
Size	Document Number		Rev
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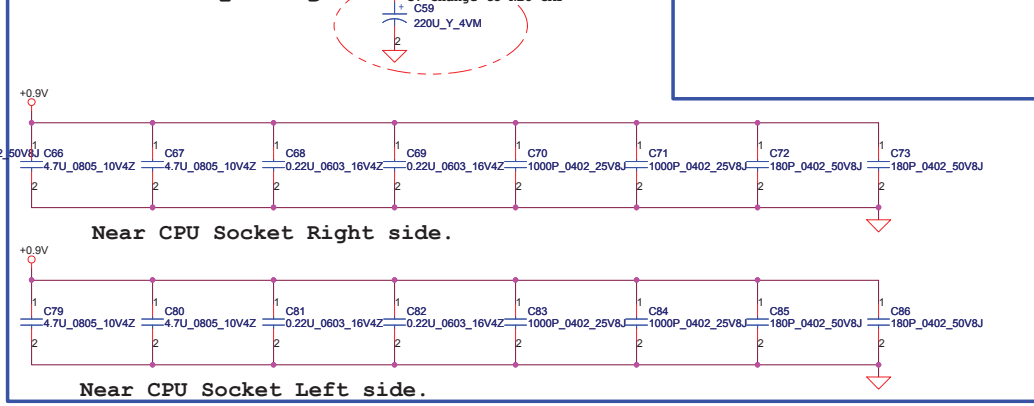
## VDD (+CPU\_CORE) decoupling.



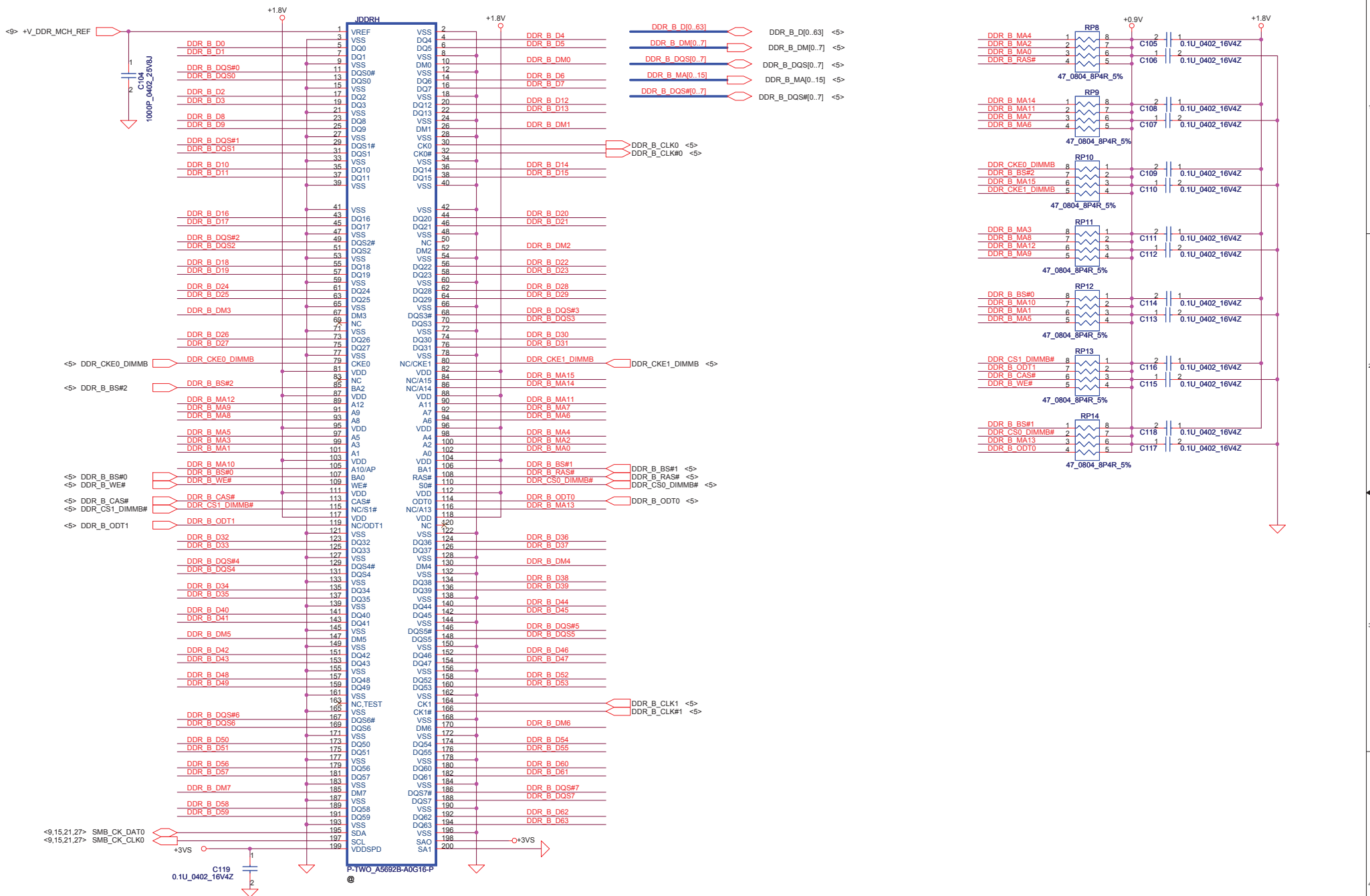
## VDDIO decoupling.



## VTT decoupling.



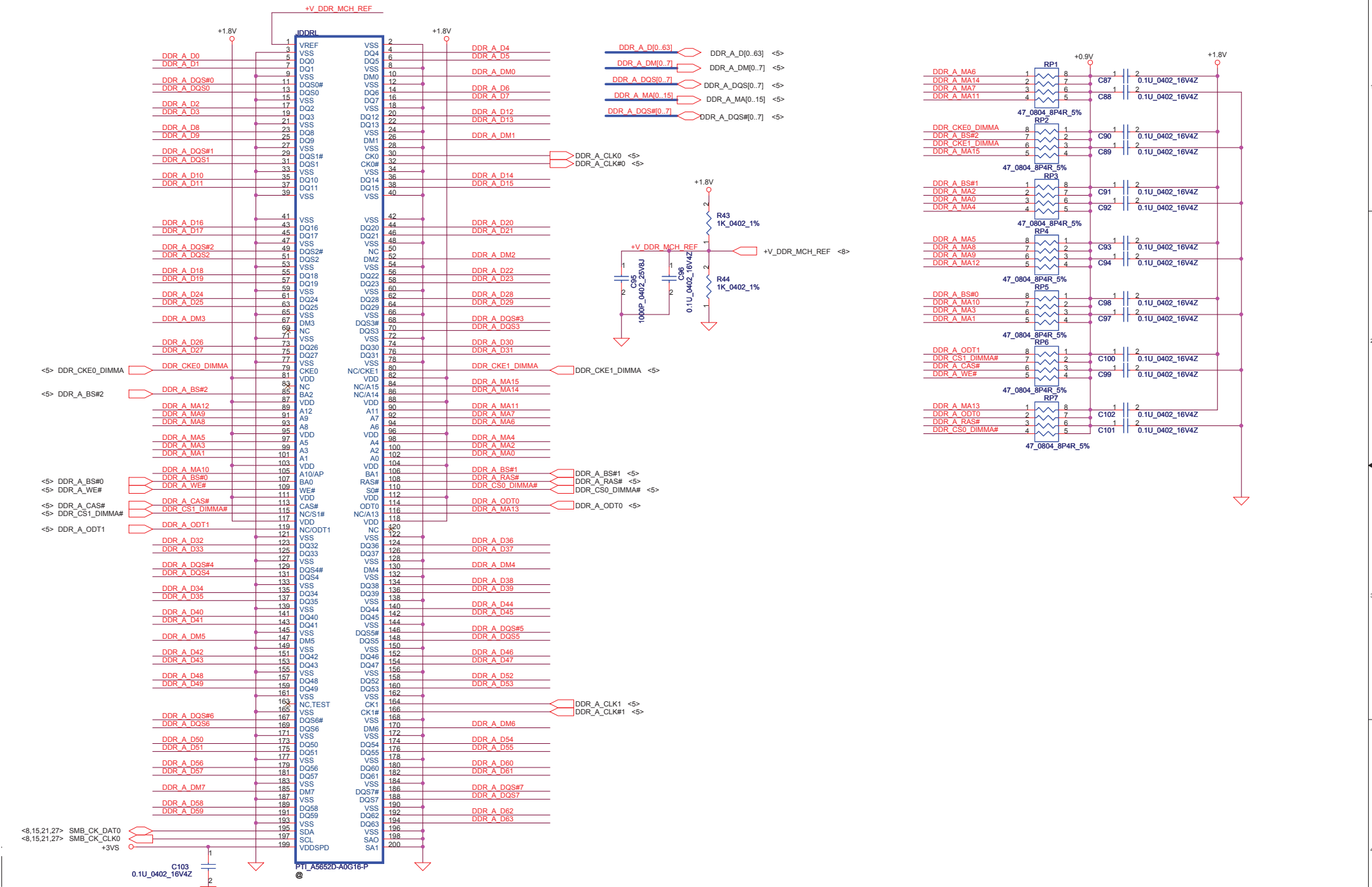
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DIMM0 STD H:9.2mm (Bot)

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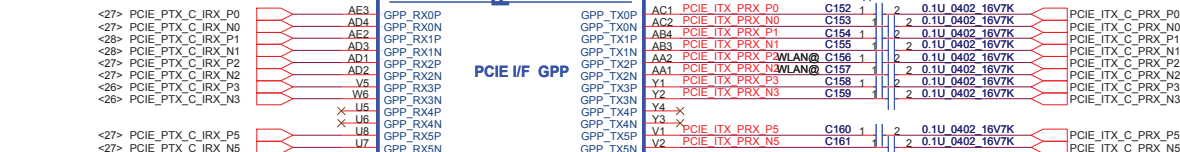
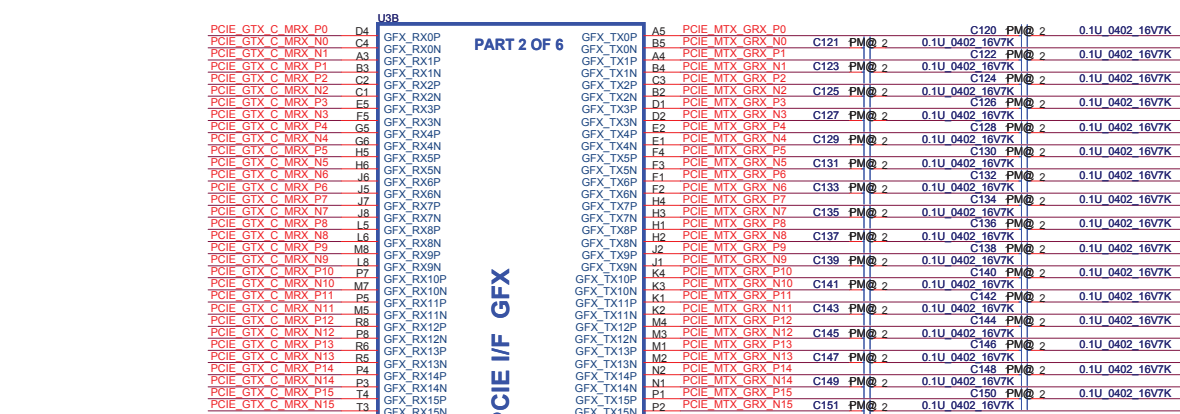
**DIMM0 STD H:5.2mm (Bot)**

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<b>DDR2 SO-DIMM 1</b>		
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GM: RS780M, PM: RX781

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 PCIE\_MTX\_C\_GRX\_P0..15 PCIE\_MTX\_C\_GRX\_N0..15



**RS780M Display Port Support (muxed on GFX)**

DP0	GFX_TX0, TX1, TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4, TX5, TX6 and TX7 AUX1 and HPD1

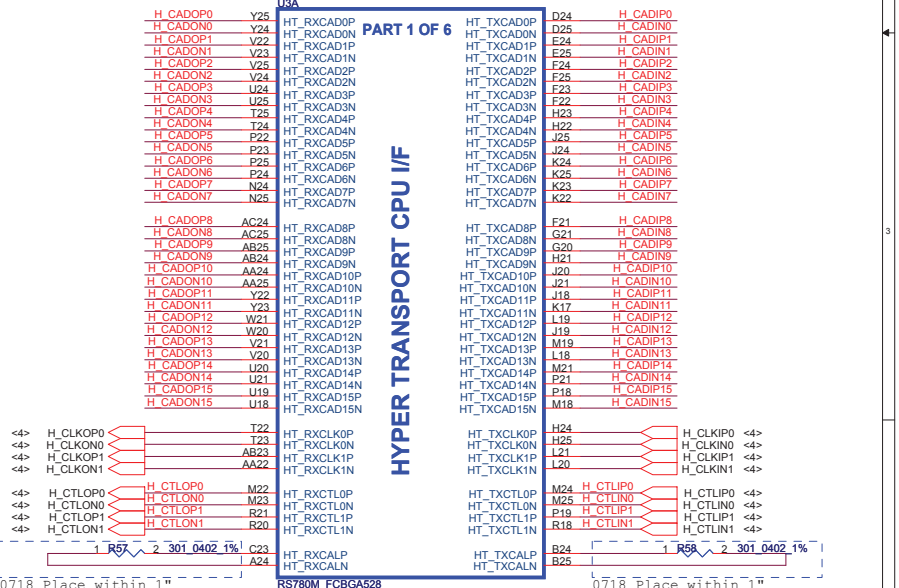
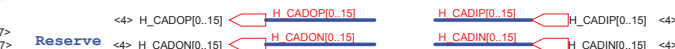
PCIE_MTX_GRX_P0	R741	I <sub>HDMI@2</sub>	0.0402 5%	HDMI_TXD0+ <18,19>
PCIE_MTX_GRX_N0	R751	I <sub>HDMI@2</sub>	0.0402 5%	HDMI_TXD0- <18,19>
PCIE_MTX_GRX_P1	R761	I <sub>HDMI@2</sub>	0.0402 5%	HDMI_TXD1+ <18,19>
PCIE_MTX_GRX_N1	R811	I <sub>HDMI@2</sub>	0.0402 5%	HDMI_TXD1- <18,19>
PCIE_MTX_GRX_P2	R821	I <sub>HDMI@2</sub>	0.0402 5%	HDMI_TXD0+ <18,19>
PCIE_MTX_GRX_N2	R831	I <sub>HDMI@2</sub>	0.0402 5%	HDMI_TXD0- <18,19>
PCIE_MTX_GRX_P3	R841	I <sub>HDMI@2</sub>	0.0402 5%	HDMI_CLK0+ <18,19>
PCIE_MTX_GRX_N3	R851	I <sub>HDMI@2</sub>	0.0402 5%	HDMI_CLK0- <18,19>

Polarity inversion

Polarity inversion

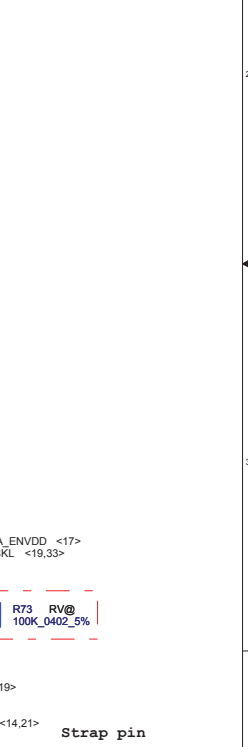
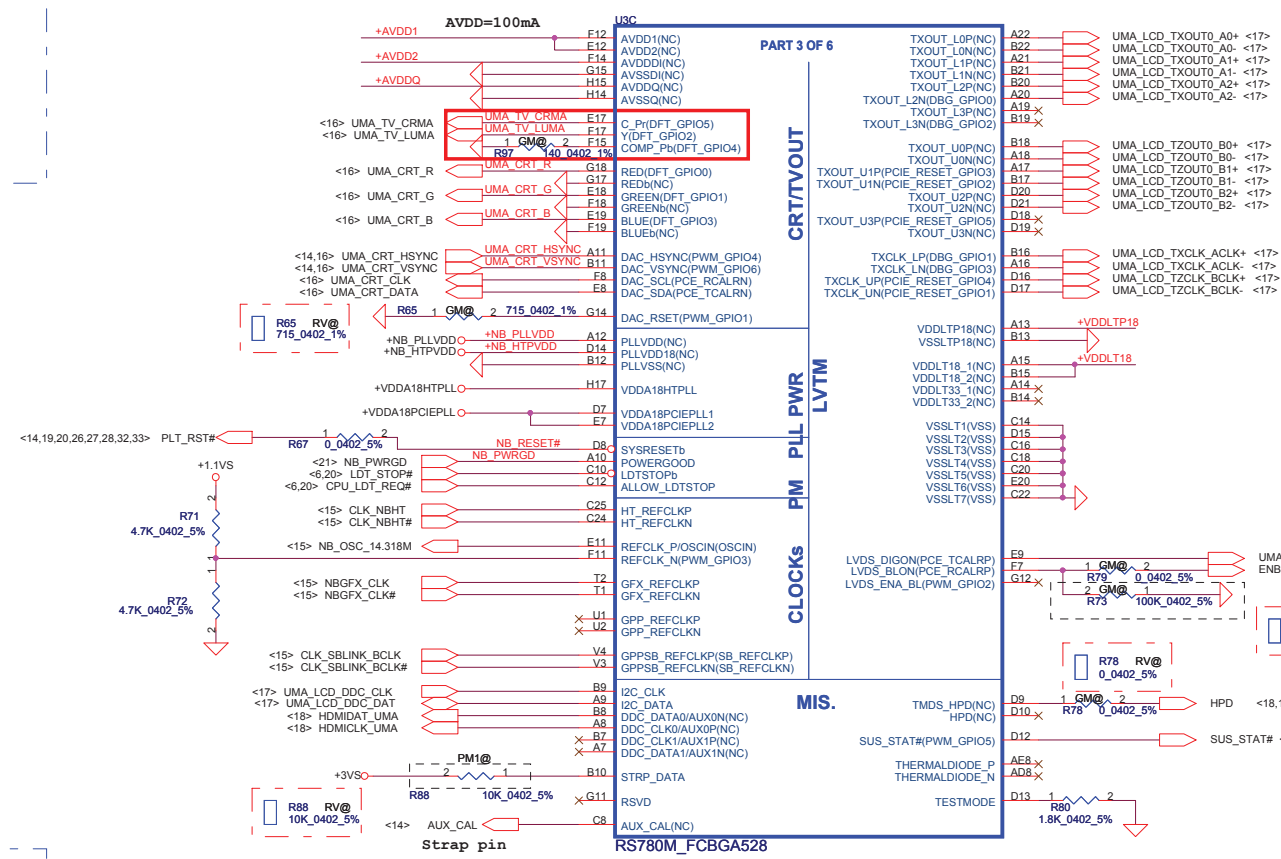
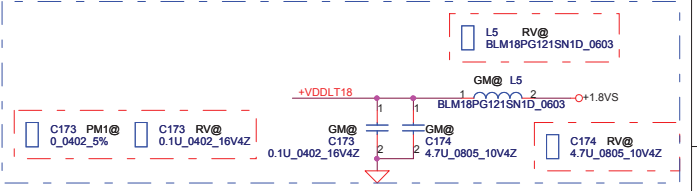
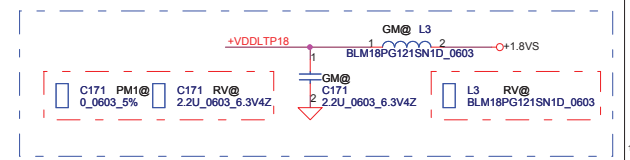
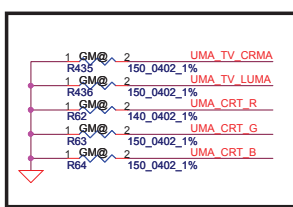
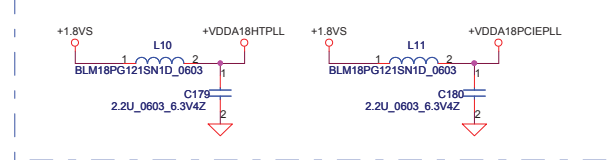
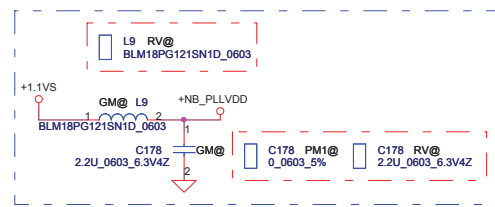
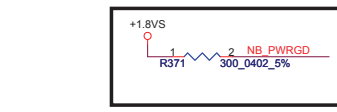
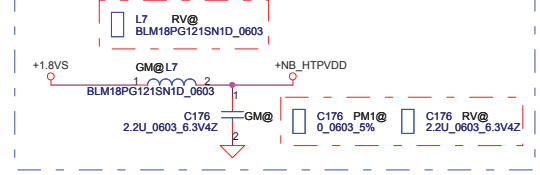
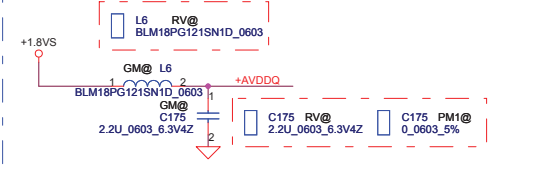
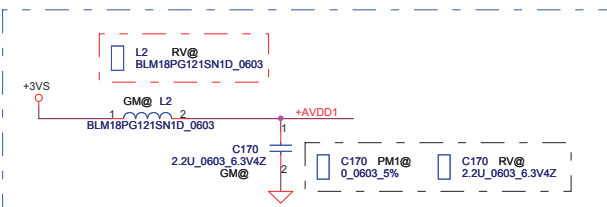
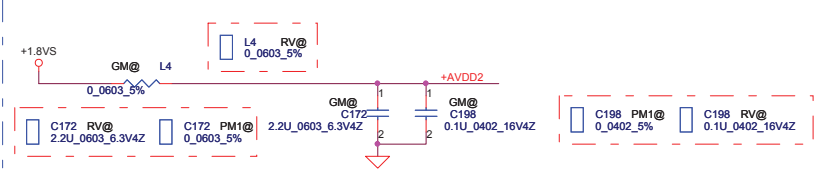
Polarity inversion

New Card  
 Card Reader  
 WLAN  
 LAN  
 Reserve



NEED CHECK R57 & R58 WITH AMD

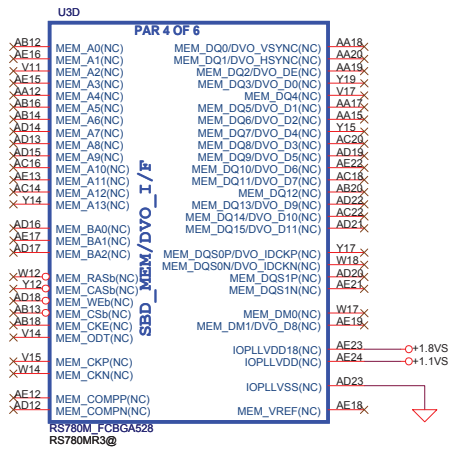
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Issued Date	2008/04/14	Deciphered Date	2009/04/14	Size	Document Number	Rev
				Customer	LA-4581P	1.0
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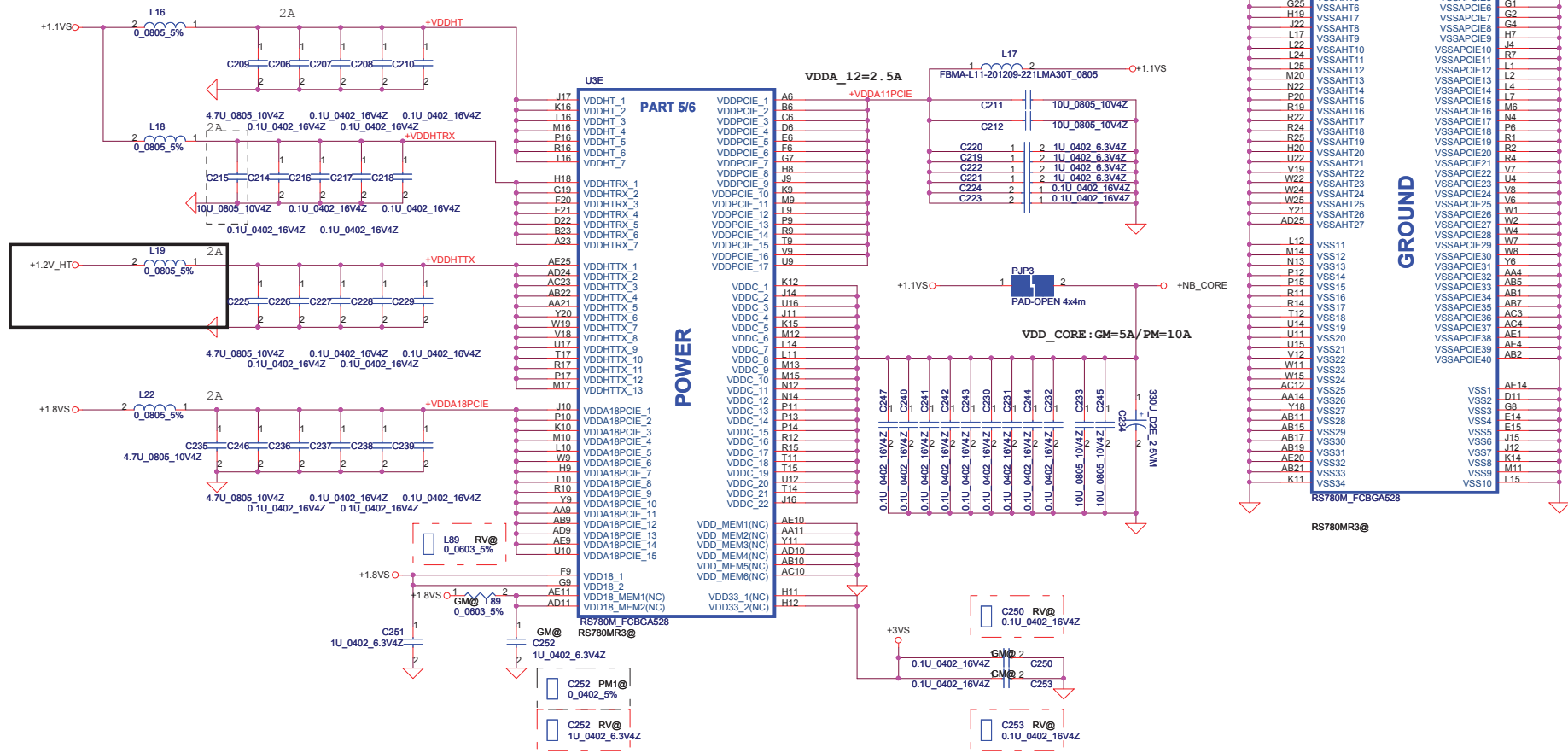
Security Classification	Compal Secret Data	
Issued Date	2008/04/14	Deciphered Date
		2009/04/14

Title		
Compal Electronics, Inc.		
RS780 VEDIO/CLK GEN		
Size	Document Number	Rev
Custom	LA-4581P	1.0
Date:	Friday, December 26, 2008	Sheet 11 of 45

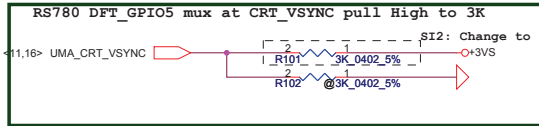
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Security Classification	Compal Secret Data		Title	<b>Compal Electronics, Inc.</b>	
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			Custom	<b>LA-4581P</b>	<b>1.0</b>
			Date:	Friday, December 26, 2008	Sheet 13 of 45



**DFT\_GPIO5:STRAP\_DEBUG\_BUS\_GPIO\_ENABLEb**

Enables the Test Debug Bus using GPIO.

- 1 : Enable (RX780, RS780)
- 0 : Disable (RX780, RS780)

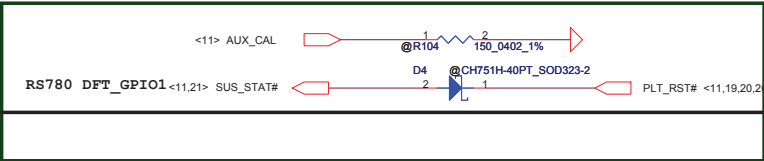
PIN: RS740-->RS780\_AUX\_CAL; RX780-->NB\_TV\_C; RS780--> VSYNC#

RS780 use register to control PCI-E configure

**DFT\_GPIO[4:2]: STRAP\_PCIE\_GPP\_CFG[2:0]**

These pin straps are used to configure PCI-E GPP mode.

- 000 : 00001
- 001 : 00010
- 010 : 01011
- 011 : 00100
- 100 : 01010
- 101 : 01100
- 111 : 01011

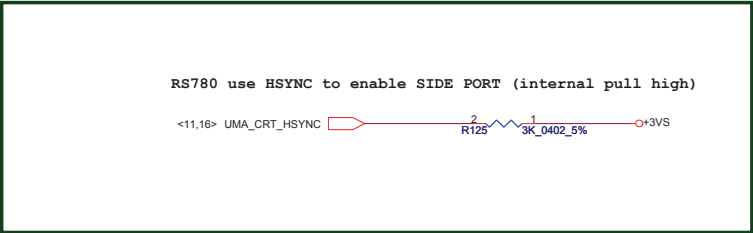


**DFT\_GPIO1: LOAD\_EEPROM\_STRAPS**

Selects Loading of STRAPS from EPROM

- 1 : Bypass the loading of EEPROM straps and use Hardware Default Values
- 0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

RS740/RX780: DFT\_GPIO1 RS780:SUS\_STAT



**DFT\_GPIO0: STRAP\_DEBUG\_BUS\_PCIE\_ENABLEb**

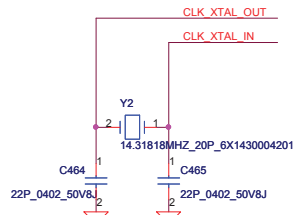
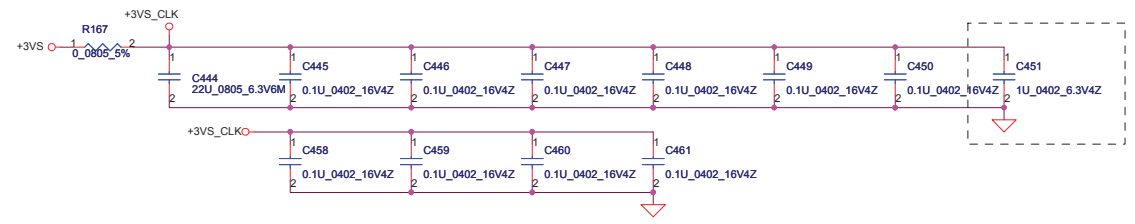
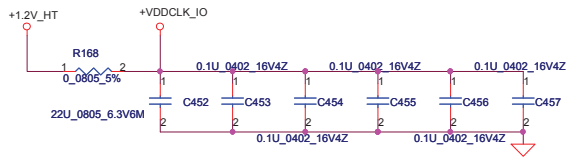
RX780: Enables the Test Debug Bus using PCIE bus

- 1 : Disable ( Can still be enabled using nbcfg register access )
- 0 : Enable

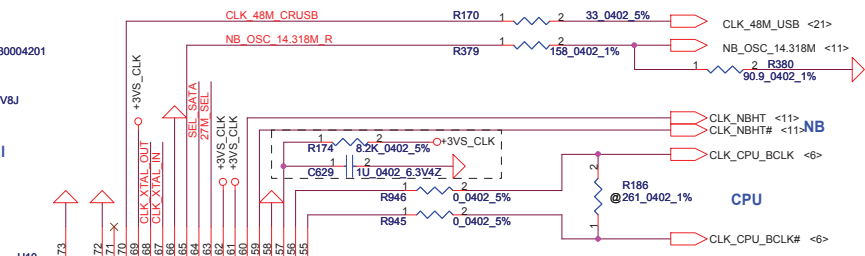
RS780: Enables Side port memory ( RS780 use HSYNC#)

- 1. Disable (RS780)
- 0 : Enable (RS780)

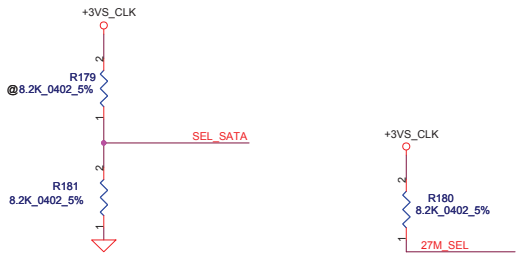
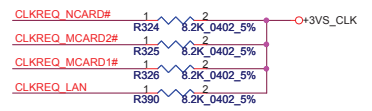
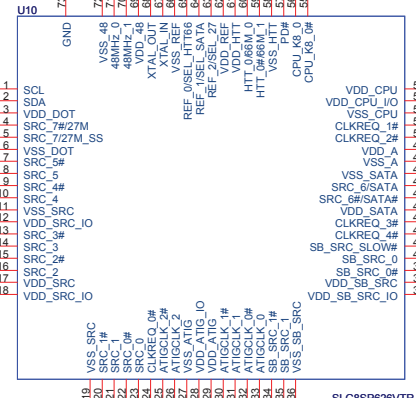
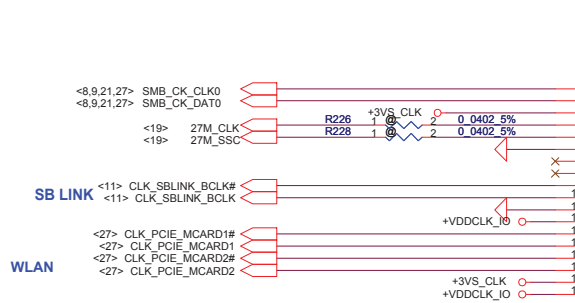
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				Document Number	1.0
				LA-4581P	
				Date:	Friday, December 26, 2008
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Routing the trace at least 10mil



	OSC_14M_NB
RS780	1.1V 158R/90.9R



SEL_SATA	1	configure as SATA output
	0 *	configure as normal SRC(SRC 6) output * default

27M_SEL	1 *	configure as 27M and 27M_SS output
	0	configure as SRC 7 output * default

NB CLOCK INPUT TABLE

NB CLOCKS	RX780	RS780
HT_REFCLKP	100M DIFF	100M DIFF
HT_REFCLKN	100M DIFF	100M DIFF
REFCLK_P	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF(IN/OUT)
GPP_REFCLK	100M DIFF	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF	100M DIFF

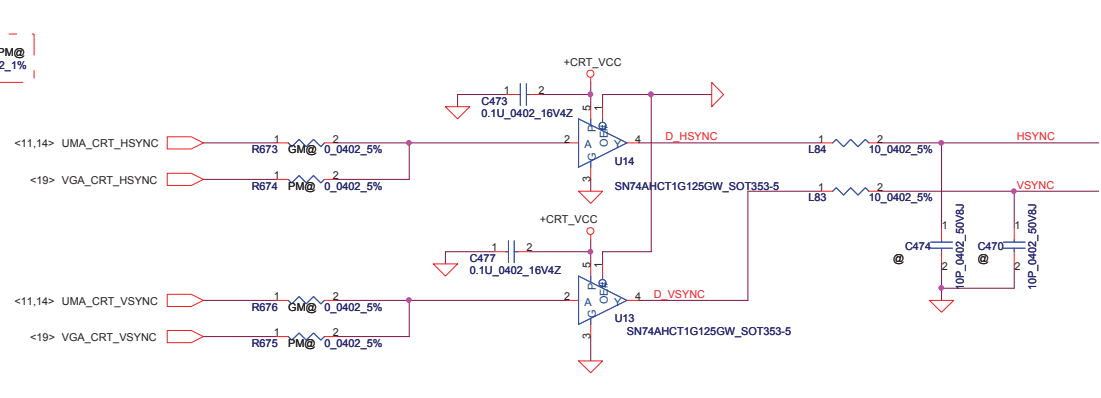
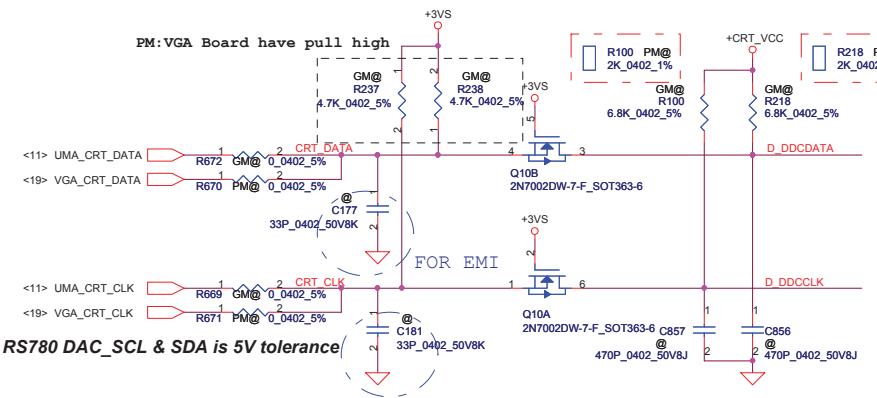
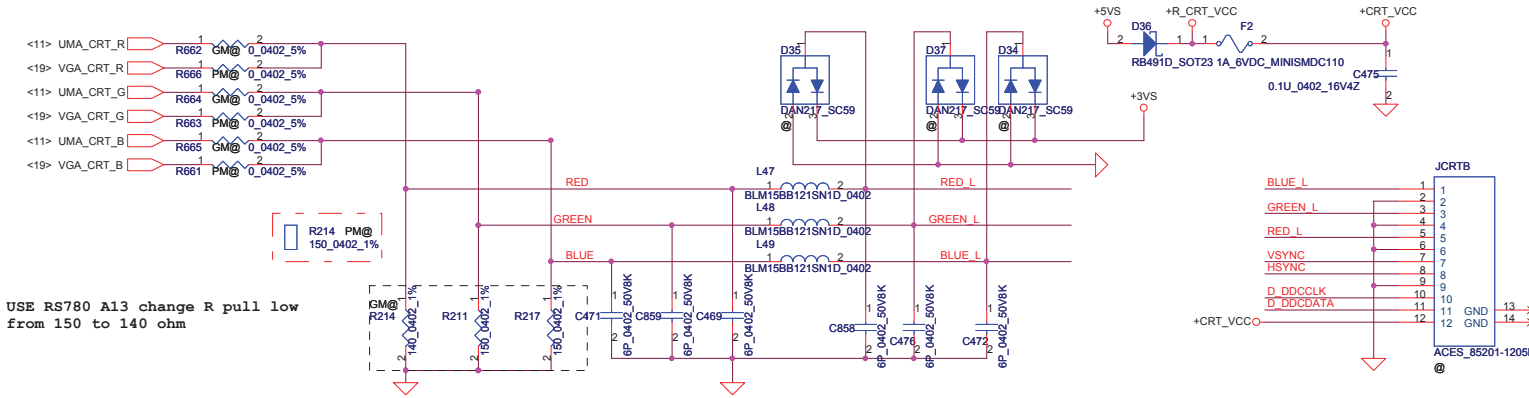
Use voltage divider resistor R379 & R380 to pull low

NB_OSC_14.318M	1	configure as single-ended 66MHz output
	0 *	configure as differential 100MHz output * default

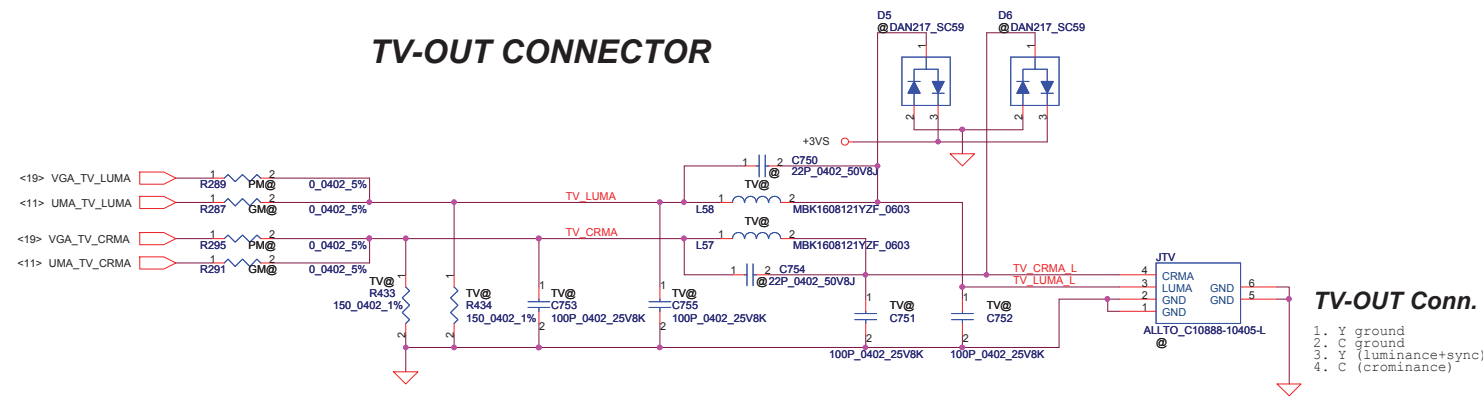
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Title			<b>Compal Electronics, Inc.</b>	
			<b>Clock Generator</b>	
Size	Document Number	Rev		
Custort	LA-4581P	1.0		
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# CRT CONNECTOR



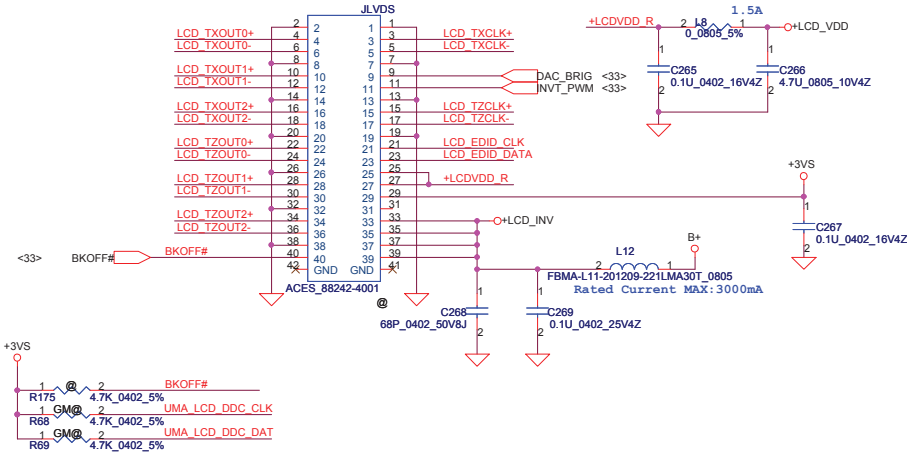
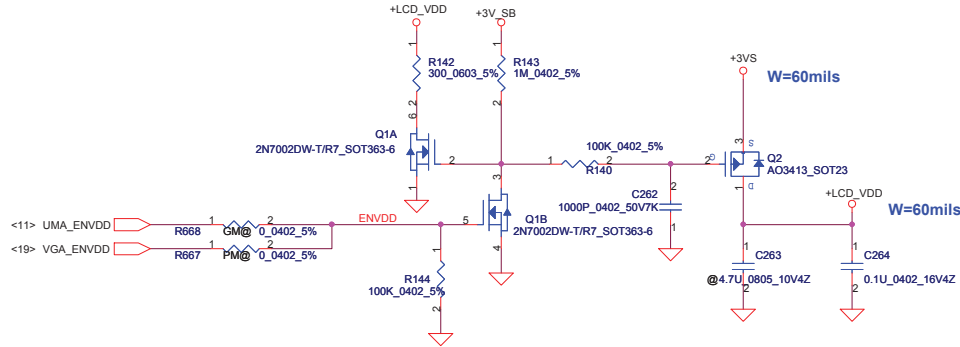
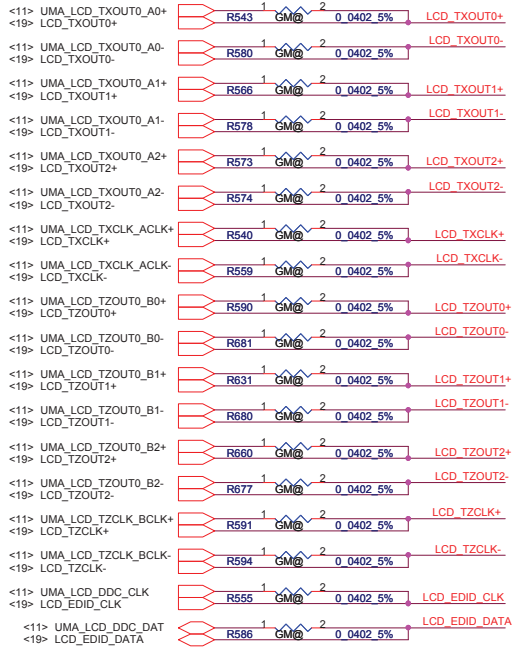
# TV-OUT CONNECTOR



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Size	Document Number	Rev		1.0	
Custom	LA-4581P				
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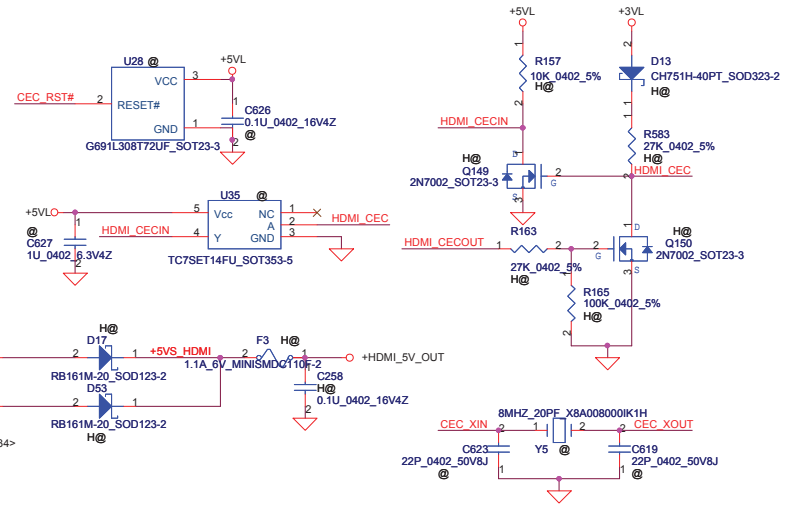
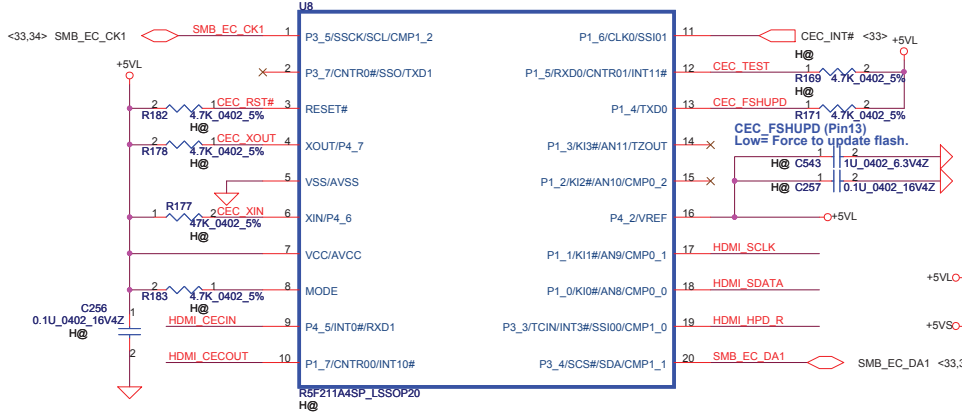


# LCD/PANEL BD. Conn.

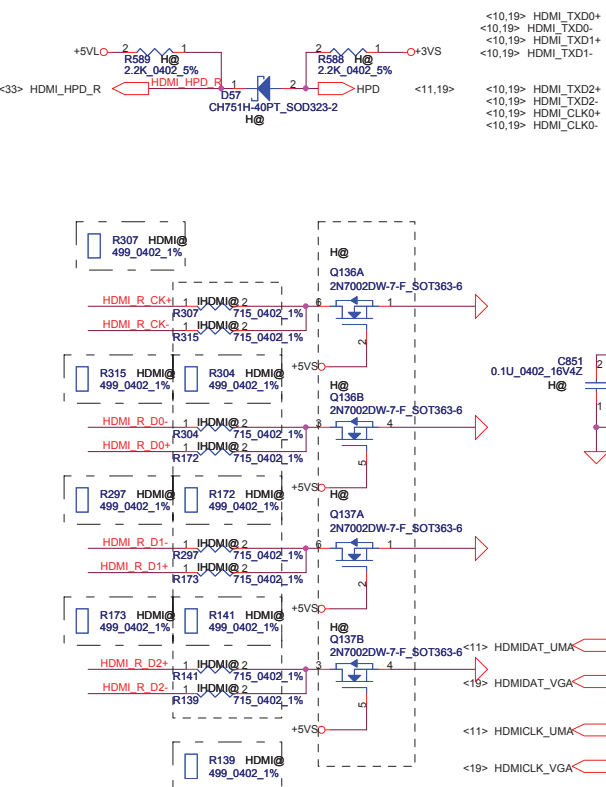
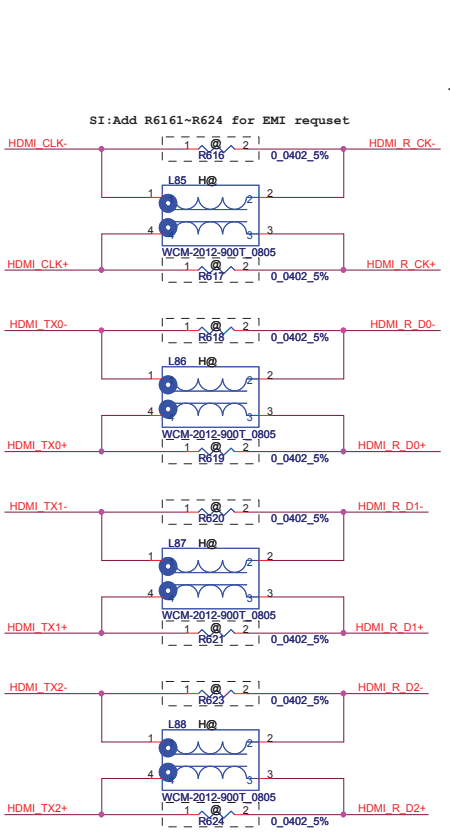
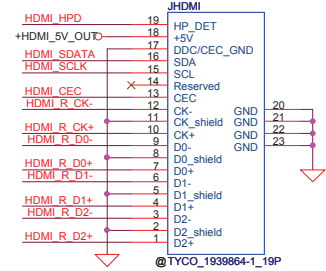


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				Date:	Friday, December 26, 2008
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# HDMI CEC Controller

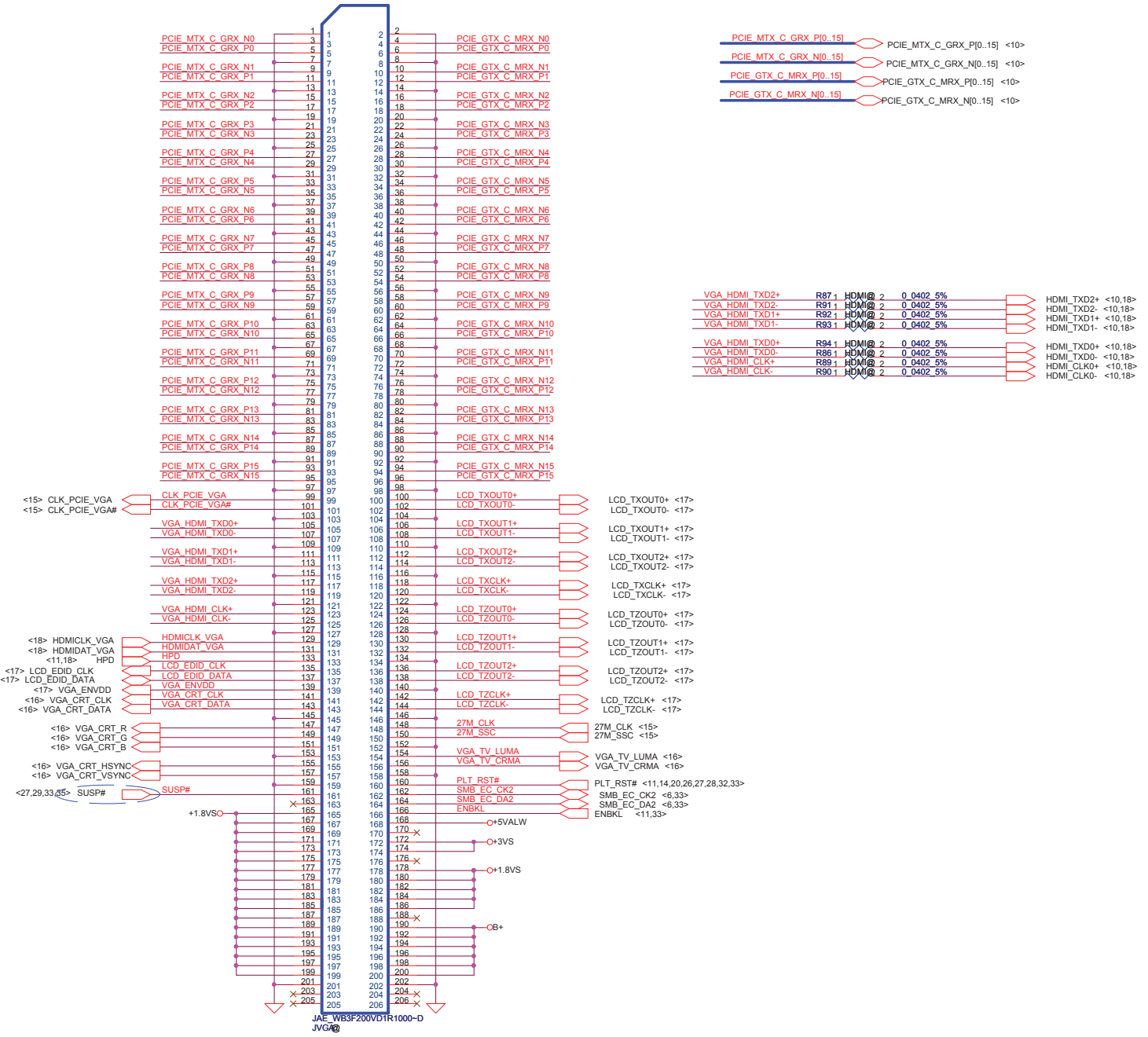


# HDMI Connector

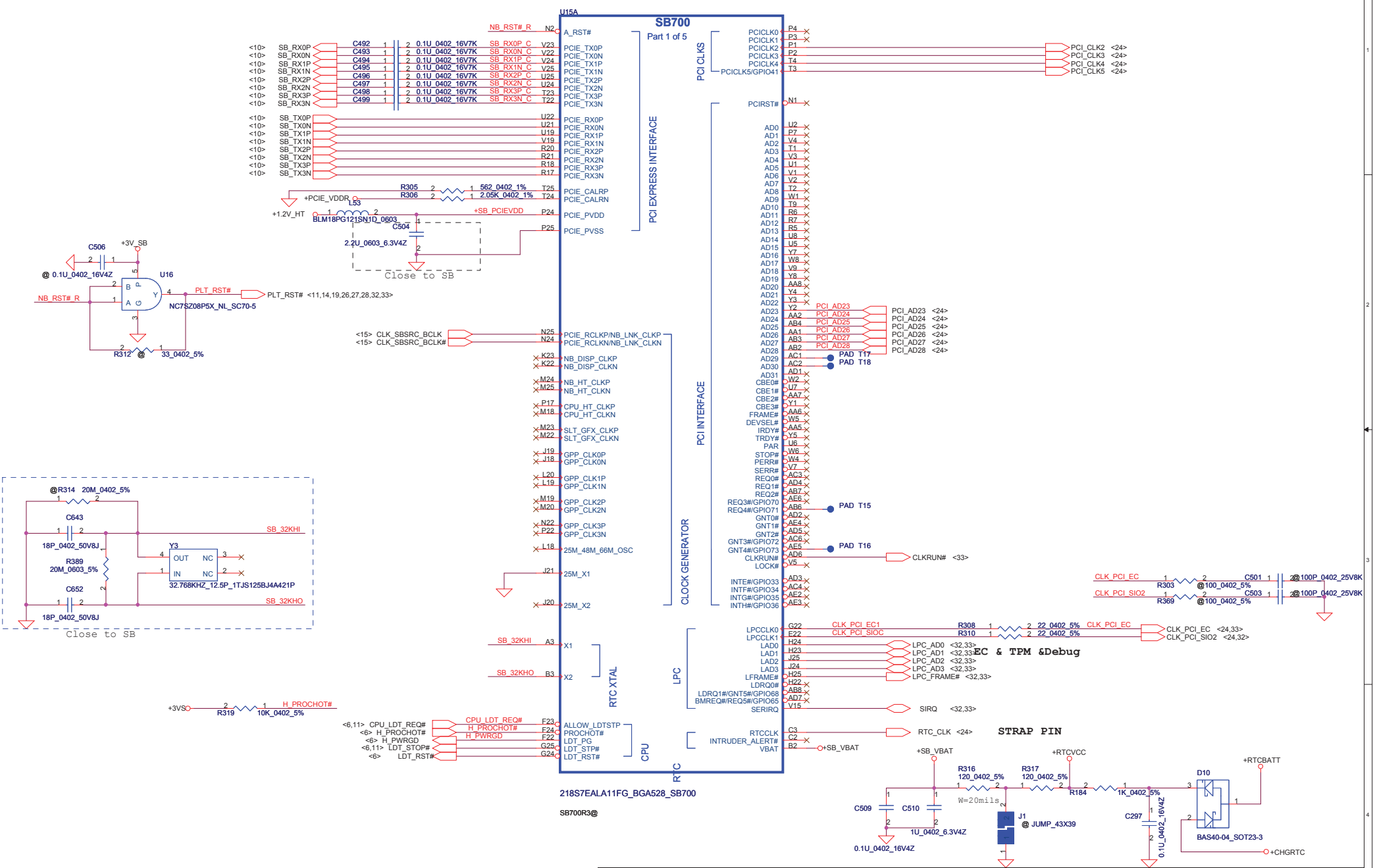


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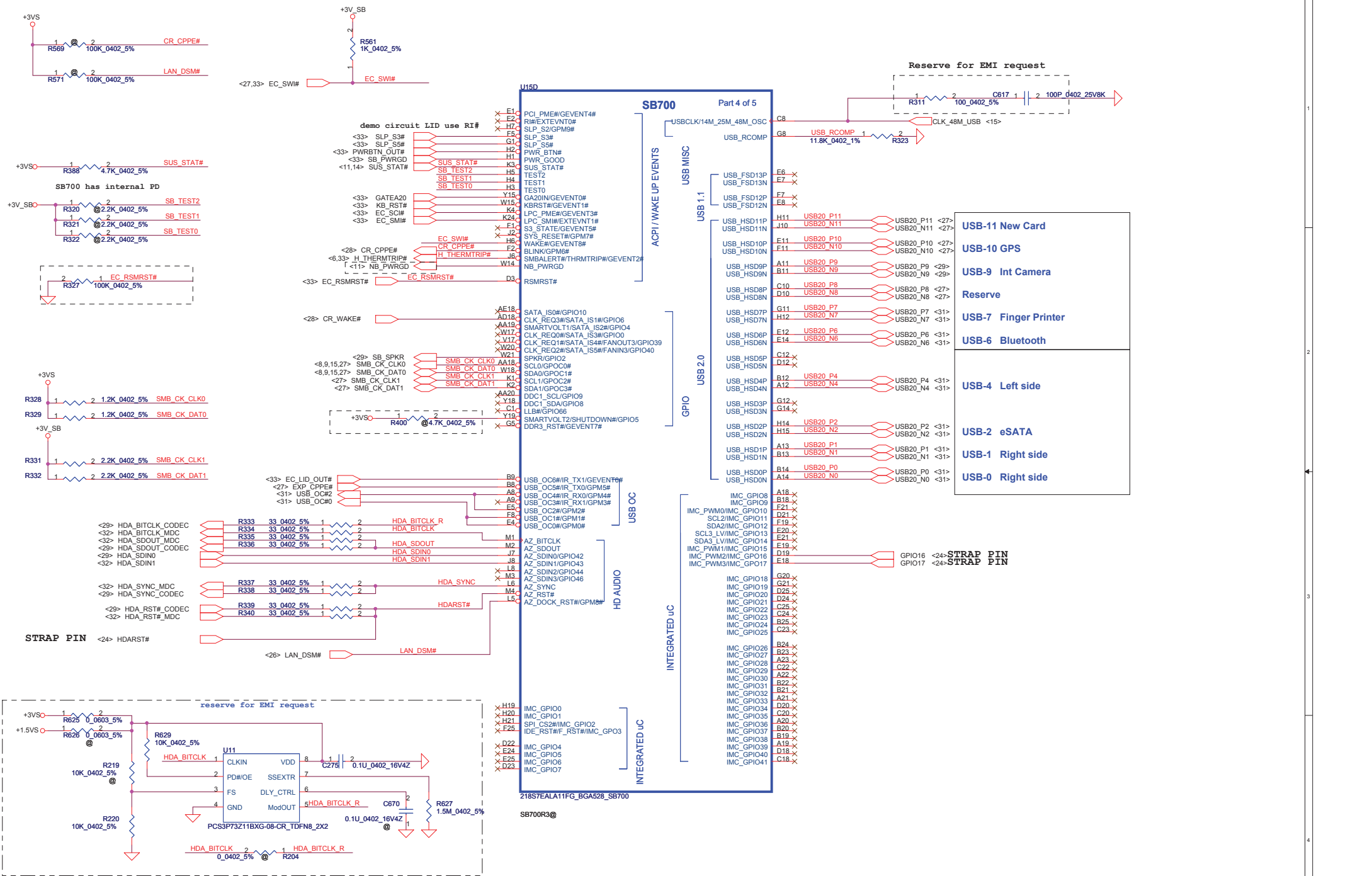
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HDMI/CEC		
Size	Document Number	Rev
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				Custom	LA-451P	1.0
				Date:	Friday, December 26, 2008	Sheet 19 of 45

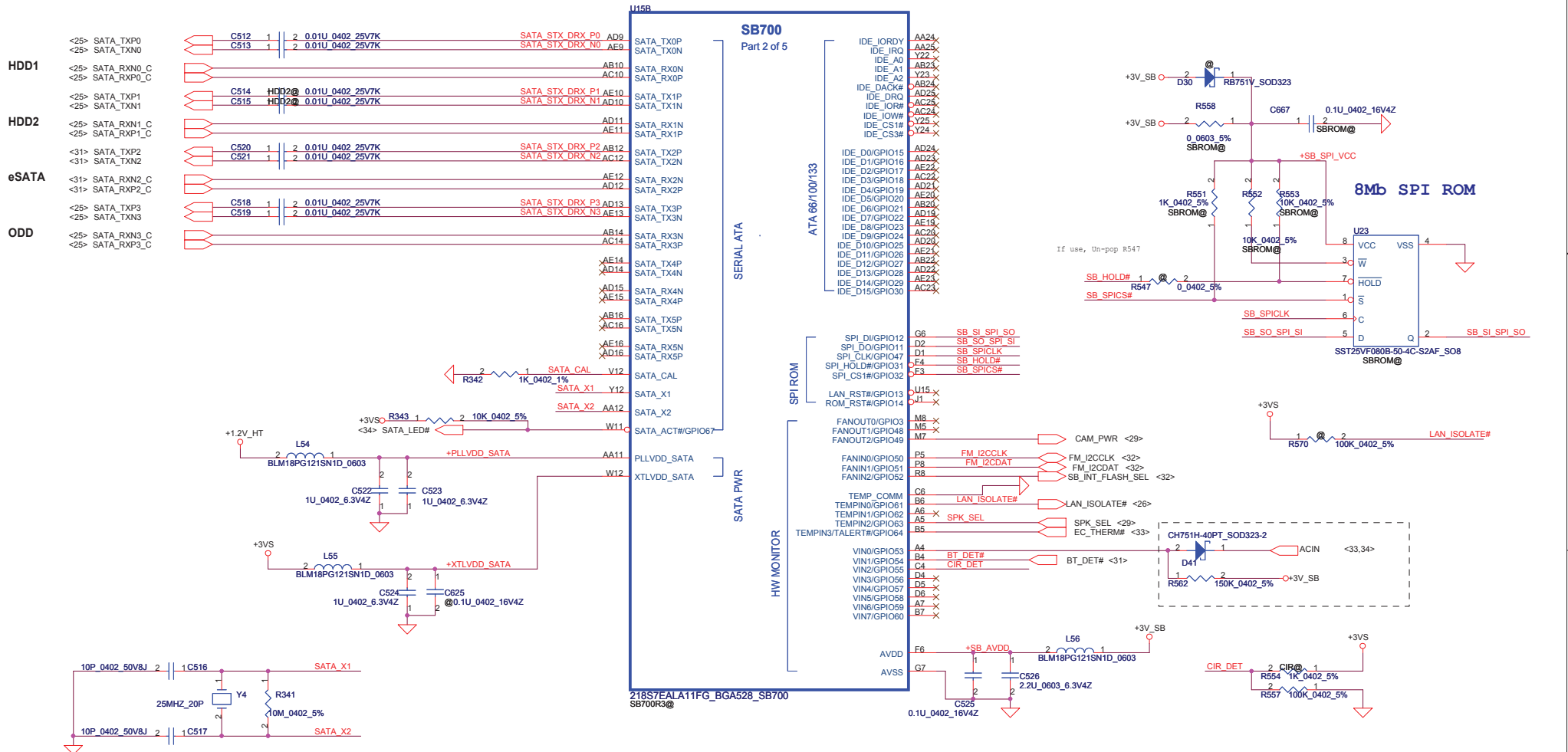


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			Sheet	20 of 45

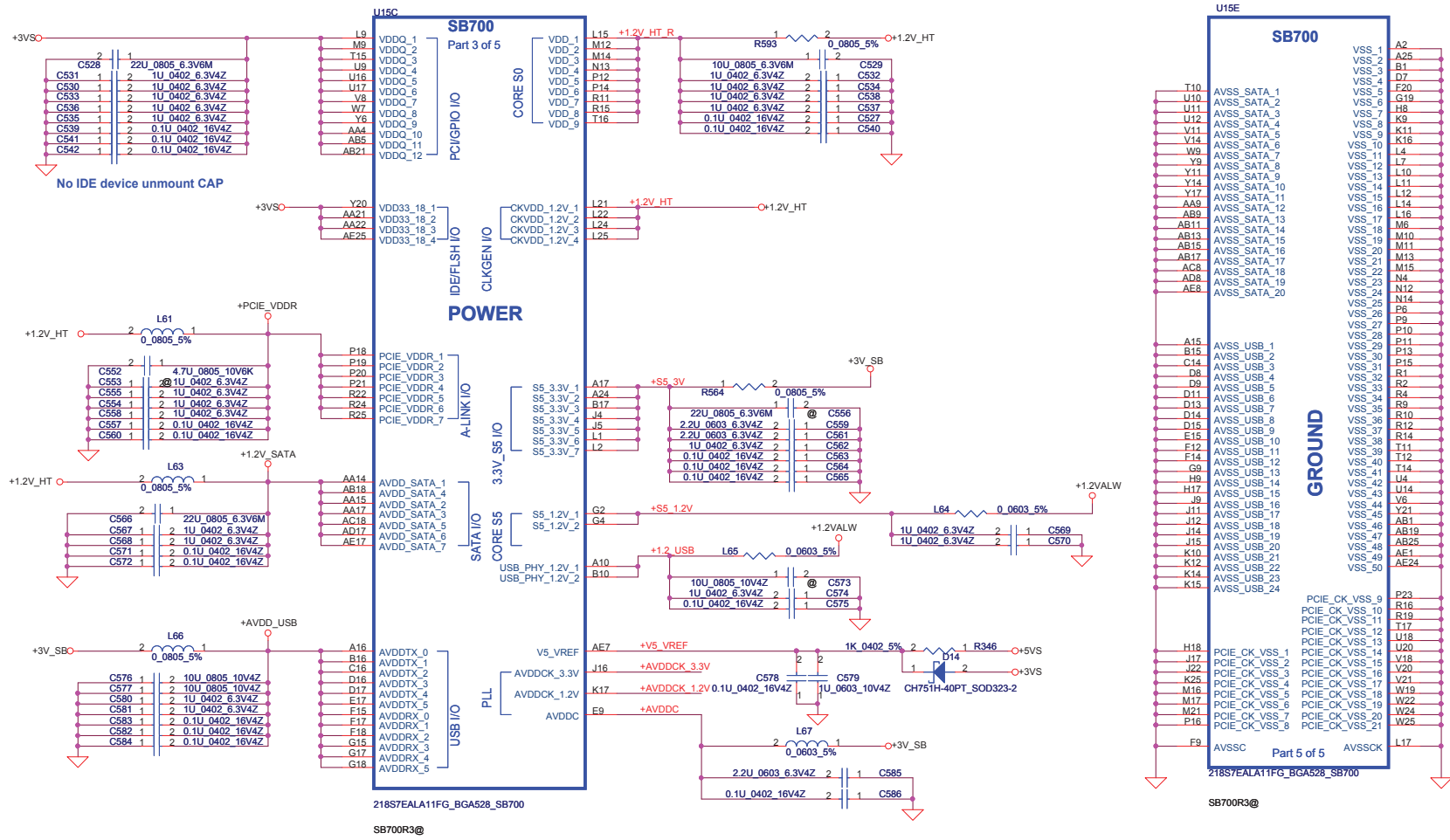


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Size	Document Number	Rev			
Custom	LA-4581P	1.0			
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Issued Date	2008/04/14	Deciphered Date	2009/04/14	SB700 SATA/IDE/SPI	
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				LA-4581P	Rev 1.0
				Date:	Friday, December 26, 2008
				Sheet	22 of 45



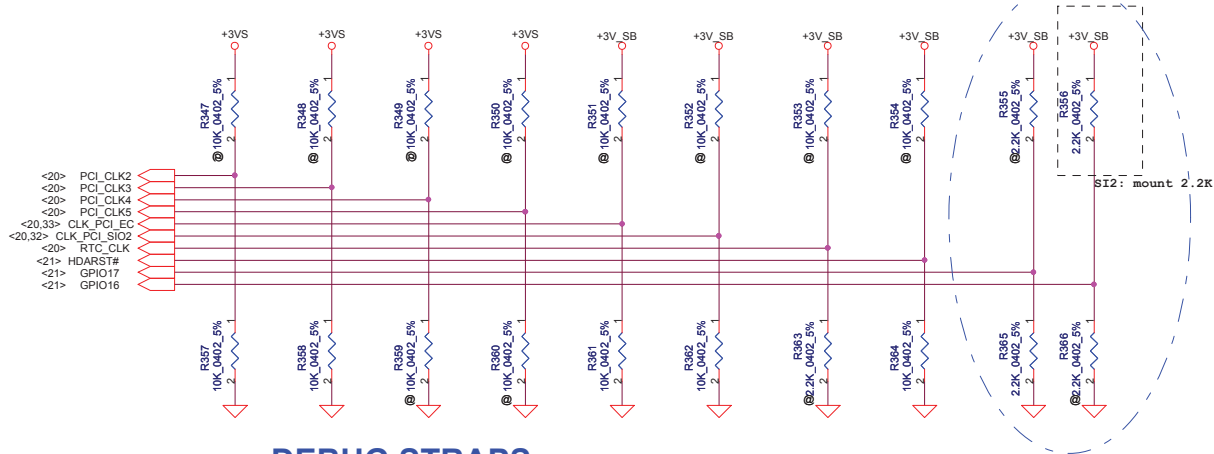
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Compal Electronics, Inc.			
Title			
<b>SB700 Power/GND</b>			
Size	Document Number		Rev
Custort	LA-4581P		1.0
Date:	Friday, December 26, 2008	Sheet	23 of 45

# REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC\_CLK

	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	AZ_RST_CD#	GP17	GP16
<b>PULL HIGH</b>	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC <b>DEFAULT</b>	EC ENABLED	Internal pull up H,H = Reserved H,L = SPI ROM	
<b>PULL LOW</b>	BOOTFAIL TIMER DISABLED <b>DEFAULT</b>	IGNORE DEBUG STRAPS <b>DEFAULT</b>			DISABLE PCI MEM BOOT <b>DEFAULT</b>	CLKGEN DISABLED <b>DEFAULT</b>	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED <b>DEFAULT</b>	L,H = LPC ROM (Default) L,L = FWH ROM	

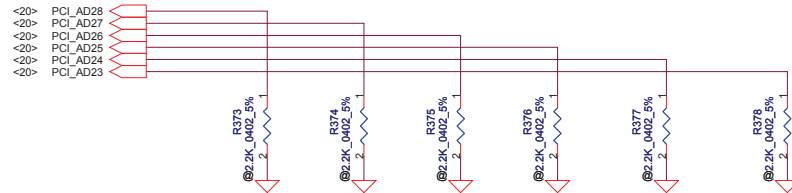


# DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI\_AD[28:23]

Need to confirm if SB SPI ROM will mount

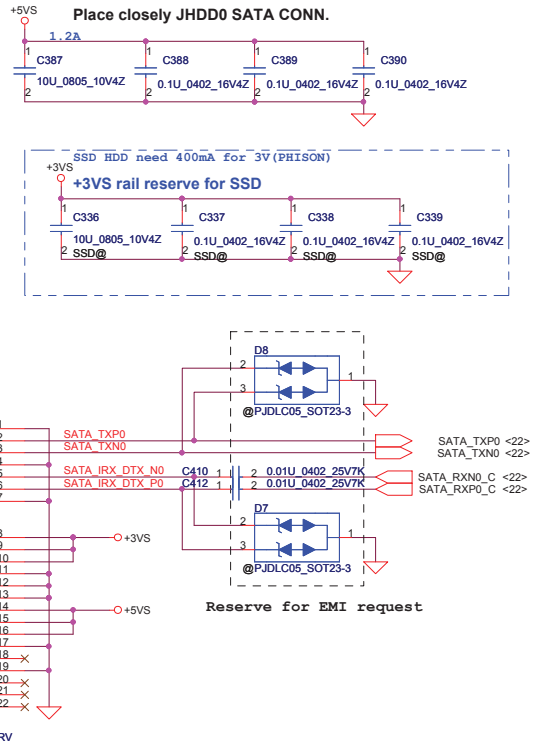
	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
<b>PULL HIGH</b>	USE LONG RESET <b>DEFAULT</b>	USE PCI PLL <b>DEFAULT</b>	USE ACPI BCLK <b>DEFAULT</b>	USE IDE PLL <b>DEFAULT</b>	USE DEFAULT PCIE STRAPS <b>DEFAULT</b>	RESERVED
<b>PULL LOW</b>	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	



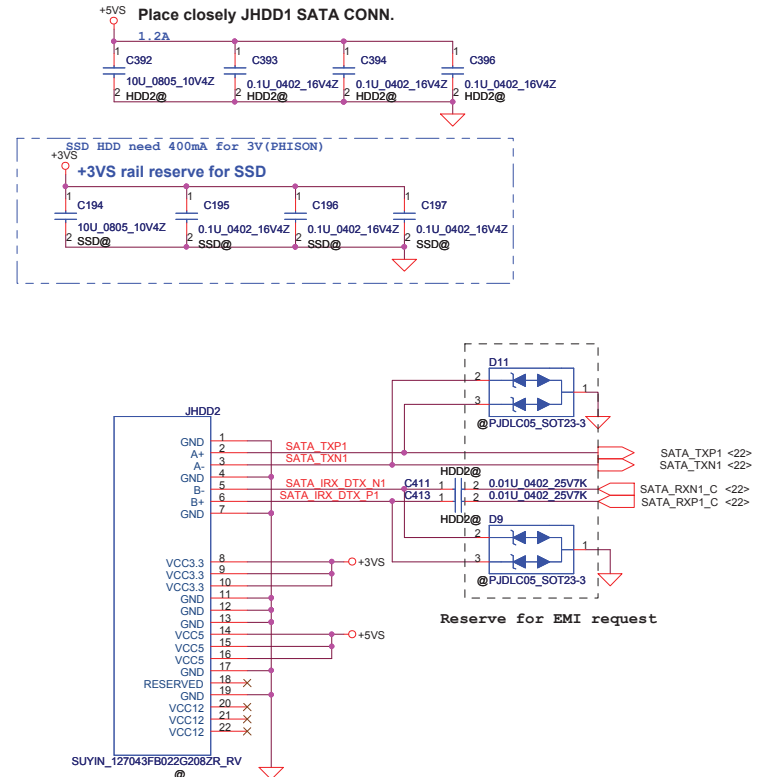
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				SB700 STRAPS		
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				Date:	Friday, December 26, 2008	Sheet 24 of 45



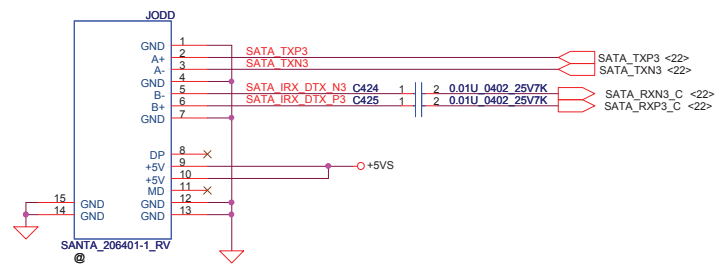
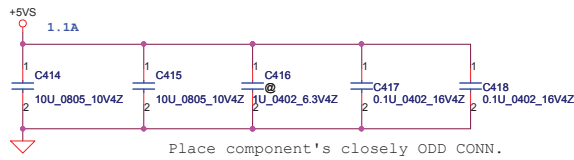
### SATA HDD1 Conn.



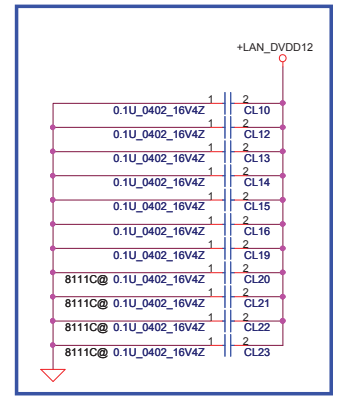
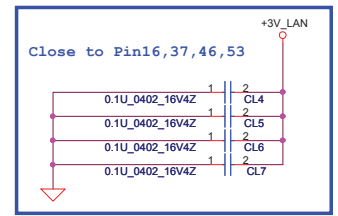
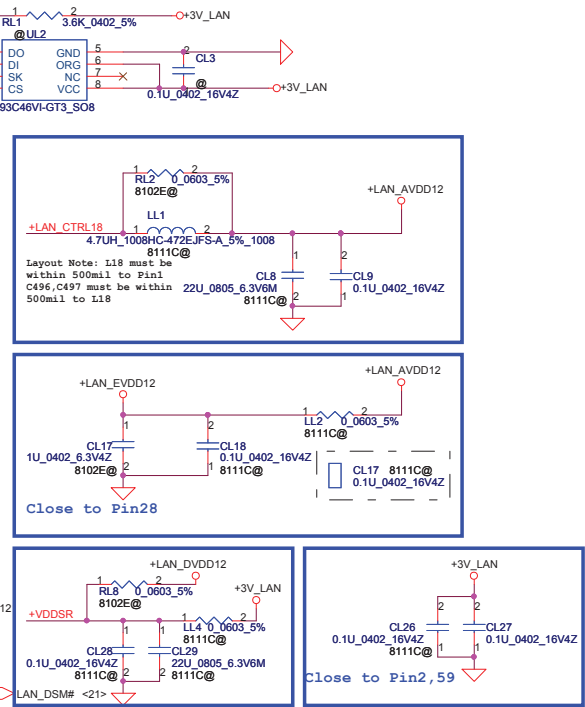
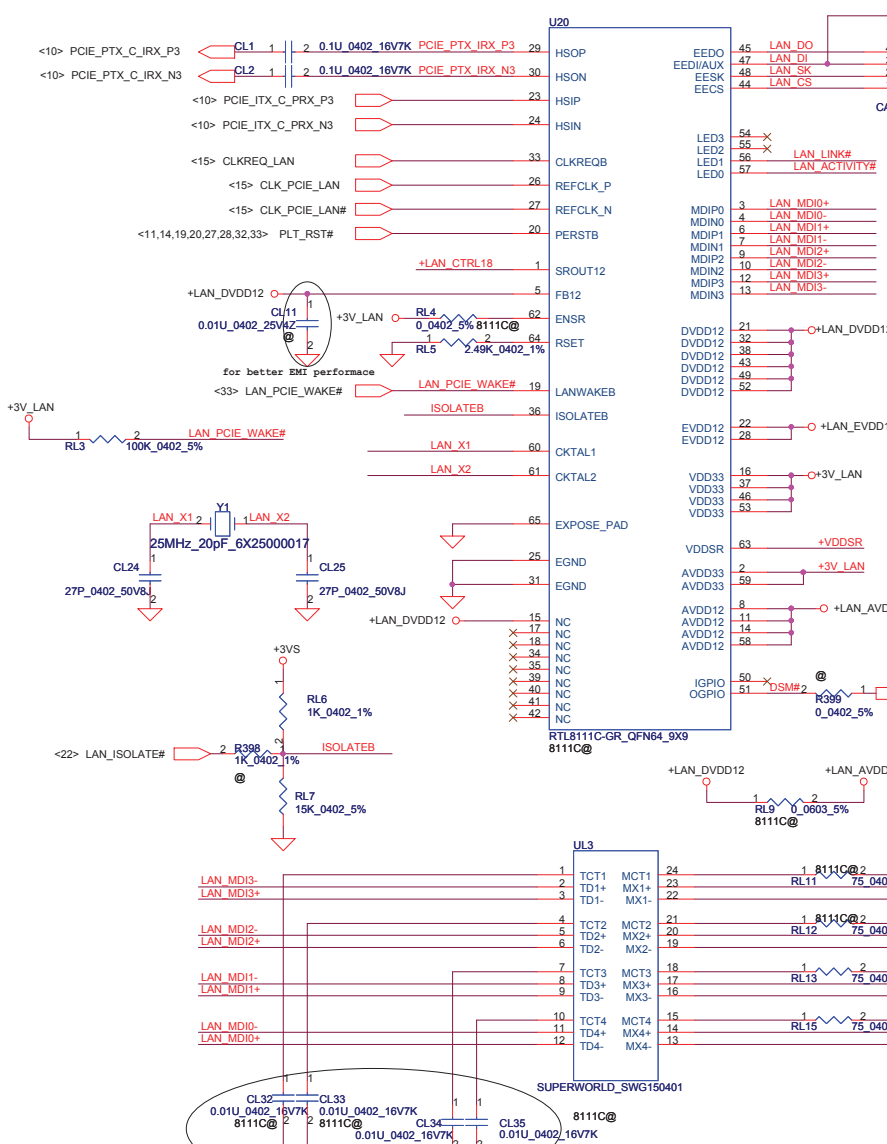
### SATA HDD2 Conn.



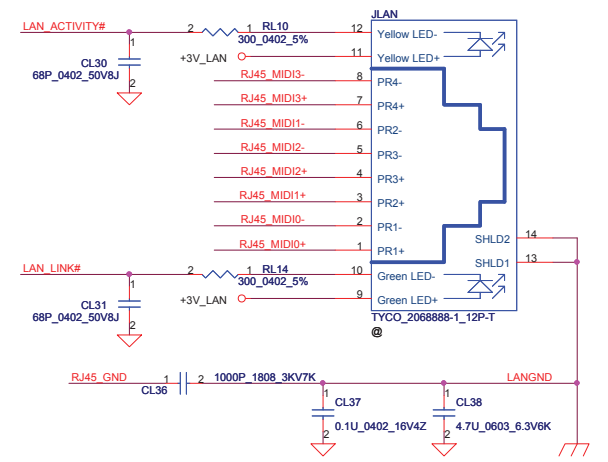
### SATA ODD Conn



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Size	Document Number	Date		Rev	1.0
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**LAN Conn.**



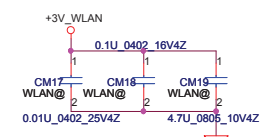
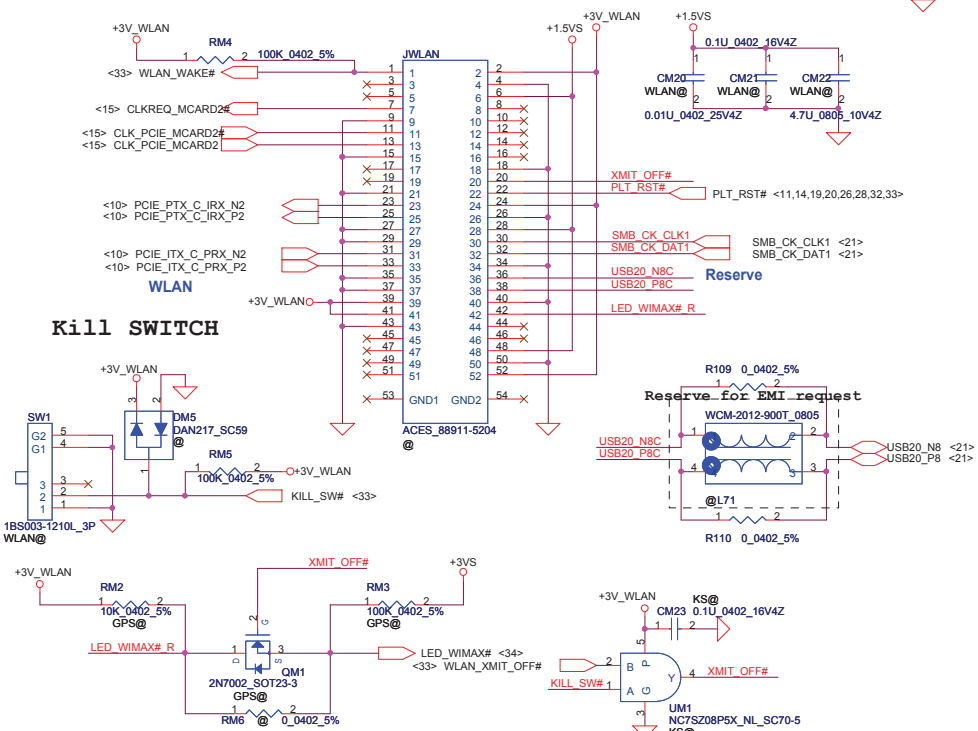
Place these components close to LAN chip

pin assignments table for difference

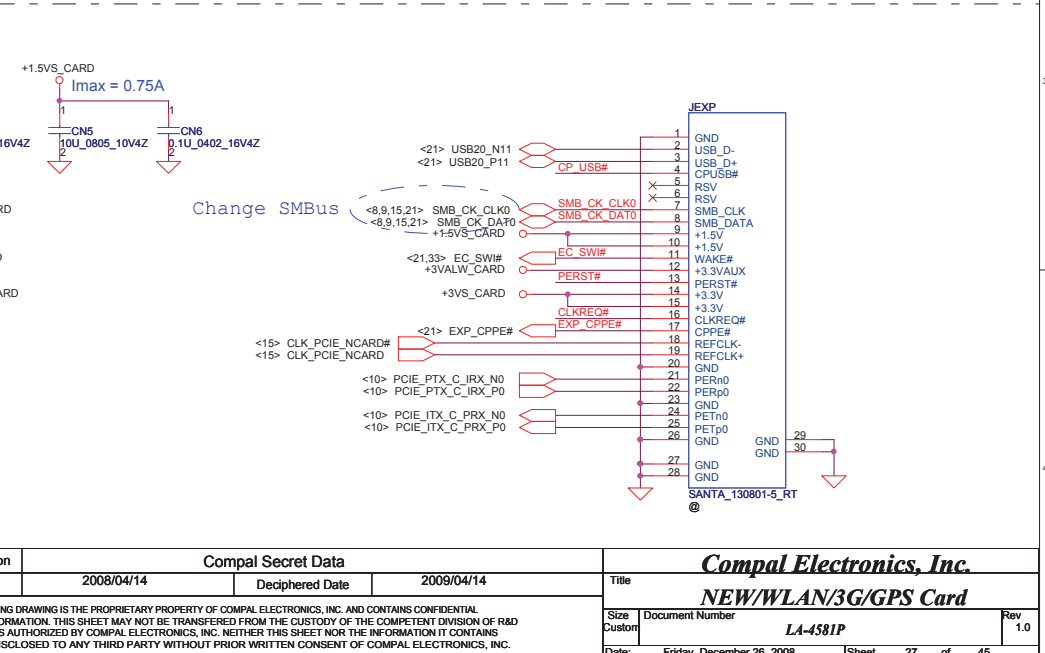
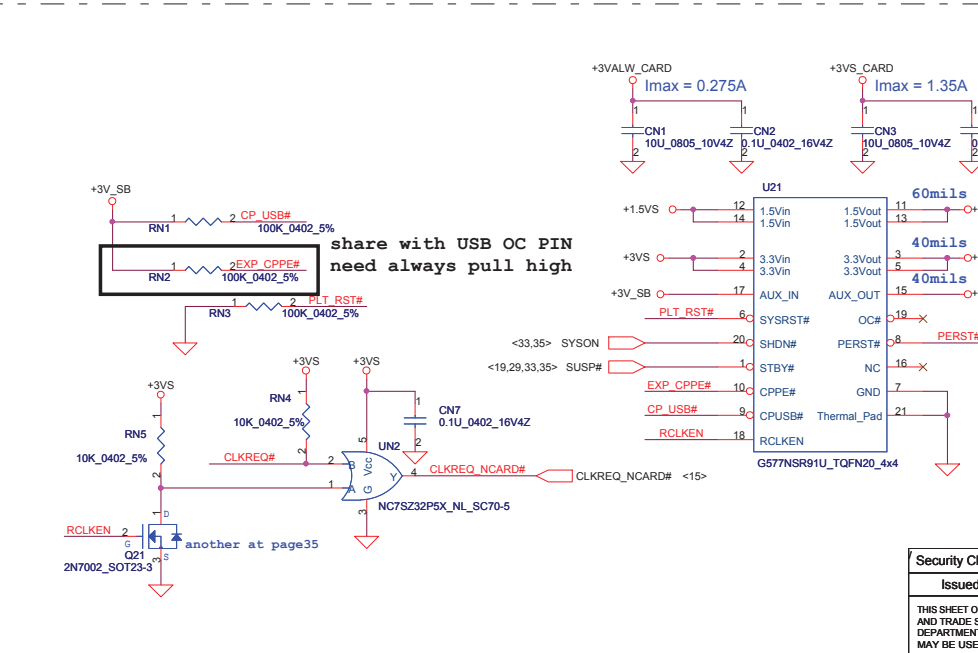
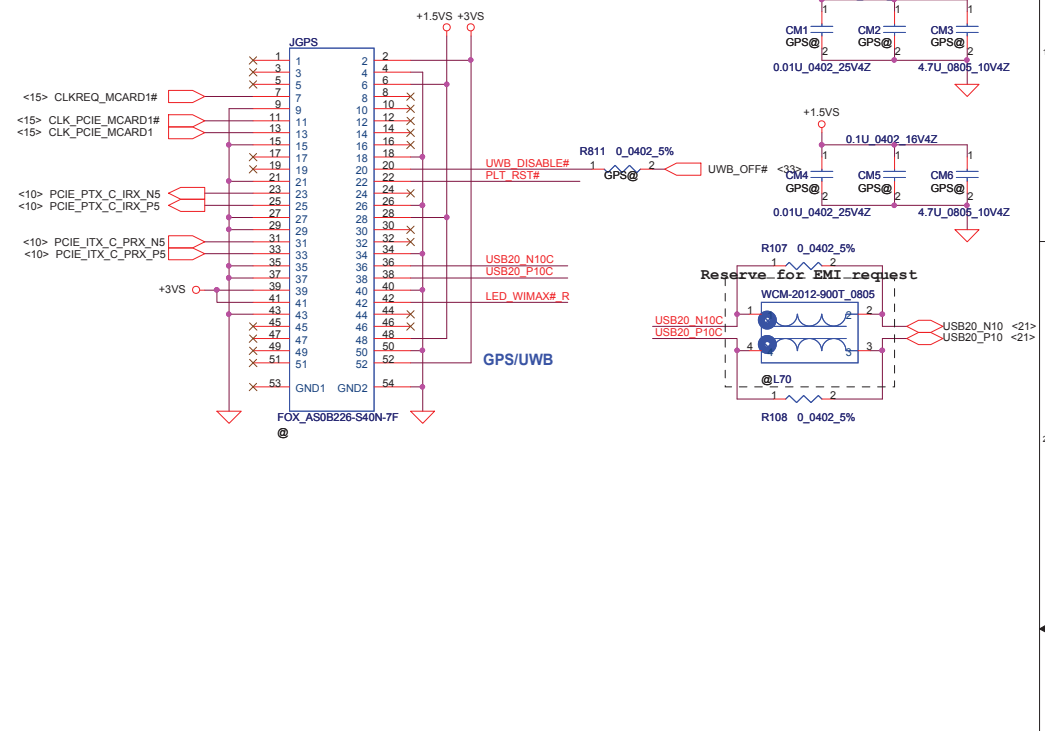
Pin	8111C	8102E
1	SR0UT12	VCTRL12A
5	FB12	NC
8	AVDD12	NC
9	MDI2E	NC
10	MDIN2	NC
11	AVDD12	NC
12	MDI2E	NC
13	MDIN3	NC
14	AVDD12	NC
15	NC	DVDD12
22	EVDD12	NC
32	DVDD12	NC
52	DVDD12	NC
58	AVDD33	DVDD12
59	AVDD33	NC
62	ENSR	NC
63	VDDSR	VCTRL12D

Security Classification	Compal Secret Data			Title	
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				Custom	1.0
				Document Number	
				LA-4581P	
				Date:	Friday, December 26, 2008
				Sheet	26 of 45

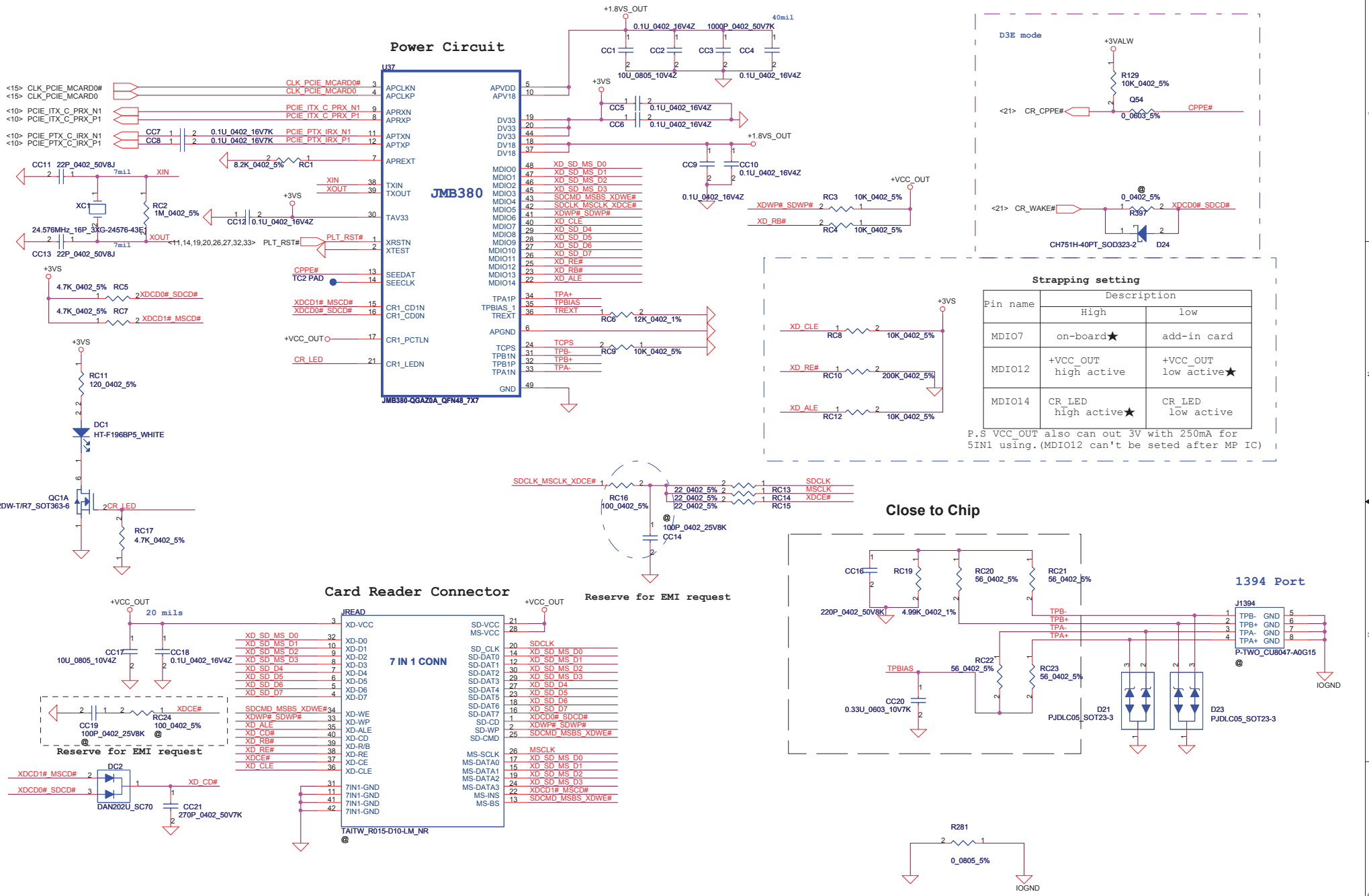
# PCIe Mini Card for WLAN



# PCIe Mini Card GPS/UWB

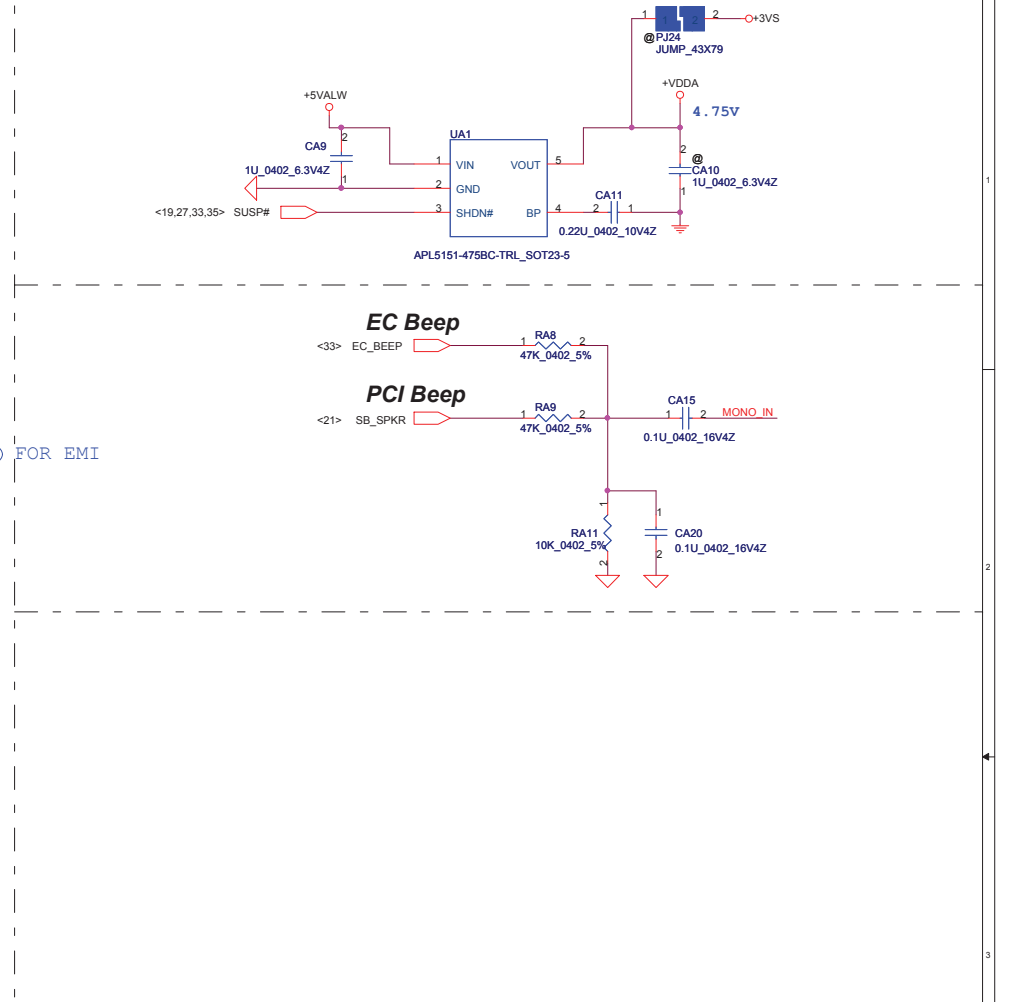
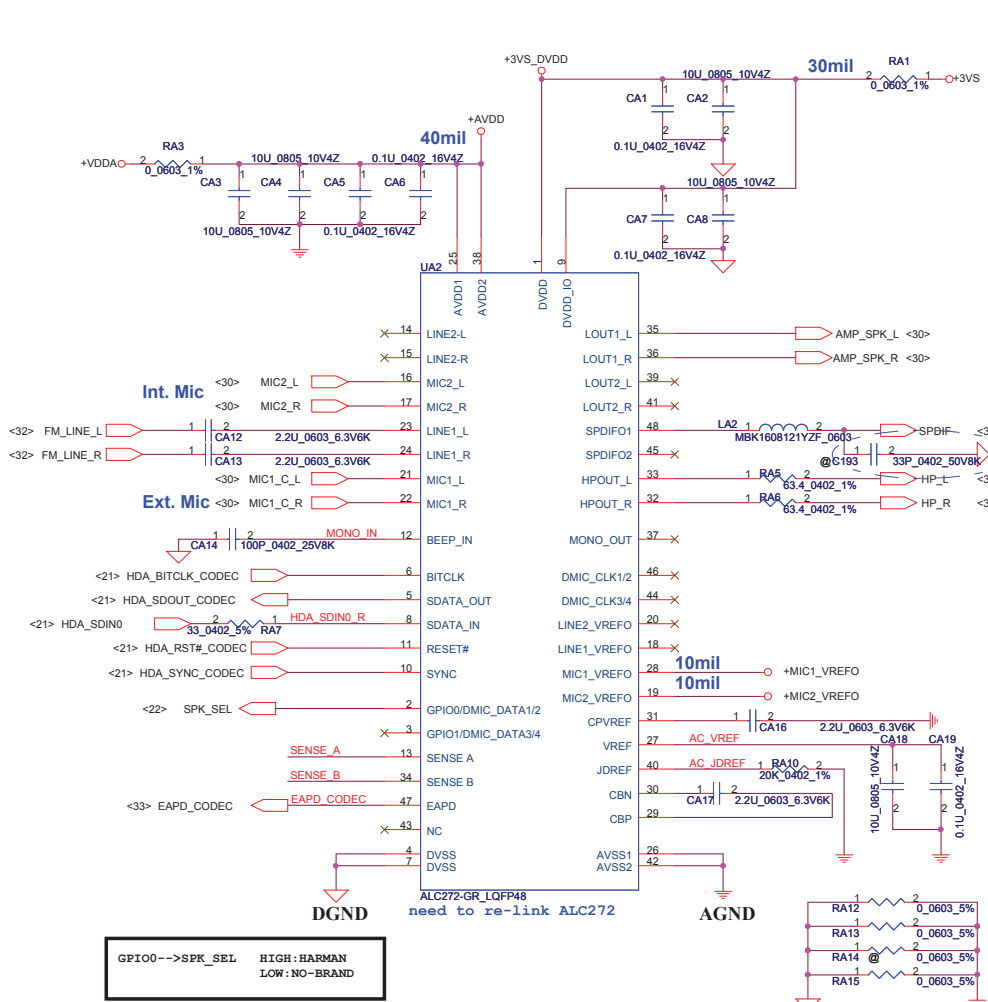


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Issued Date	2008/04/14	Deciphered Date	2009/04/14	NEW/WLAN/3G/GPS Card	
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				Customer	LA-4581P
				Date	Friday, December 26, 2008
				Sheet	27 of 45
				Rev	1.0

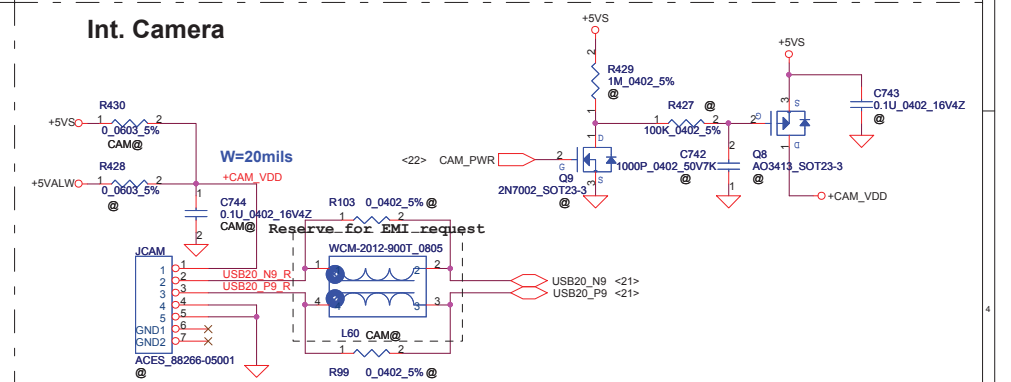
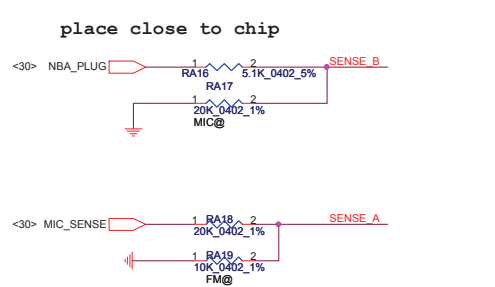


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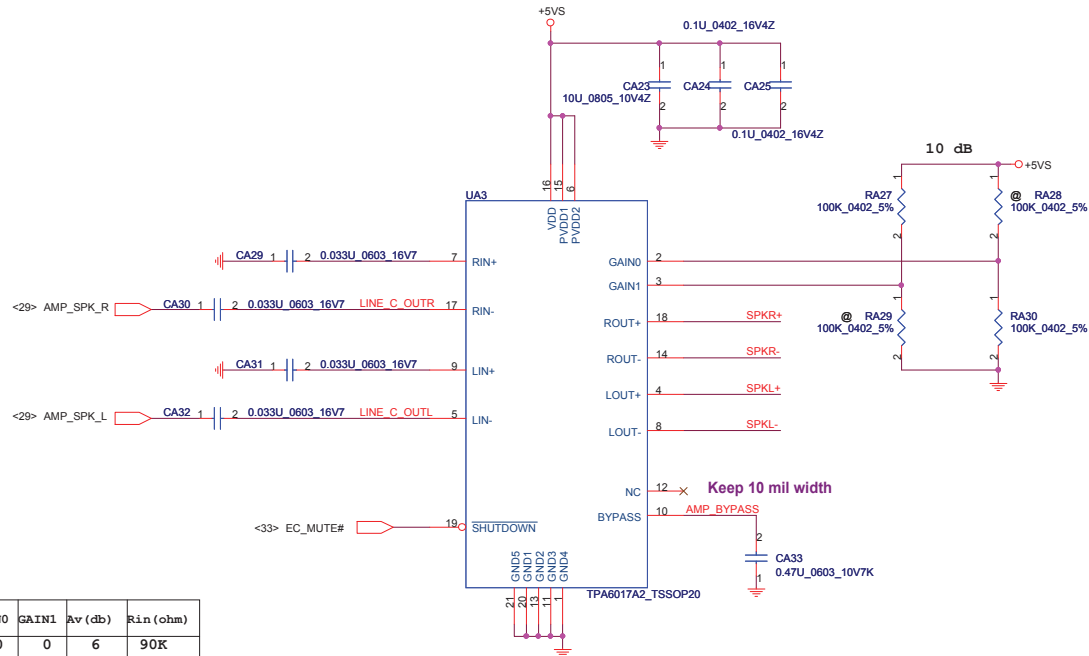
Title			
<b>Compal Electronics, Inc.</b>			
<b>JMB380 card reader/1394</b>			
Size	Document Number		Rev
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Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-A (PIN 39, 41)	Ext. MIC
	20K	PORT-B (PIN 21, 22)	
	10K	PORT-C (PIN 23, 24)	
SENSE B	5.1K	PORT-D (PIN 35, 36)	SPK out
	39.2K	PORT-E (PIN 14, 15)	Int. MIC
	20K	PORT-F (PIN 16, 17)	
	10K	PORT-H (PIN 37)	
5.1K	PORT-I (PIN 32, 33)	Headphone out	

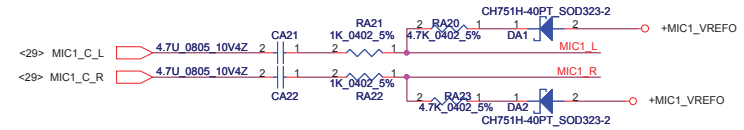


# TPA6017 Medium Range Amplifier

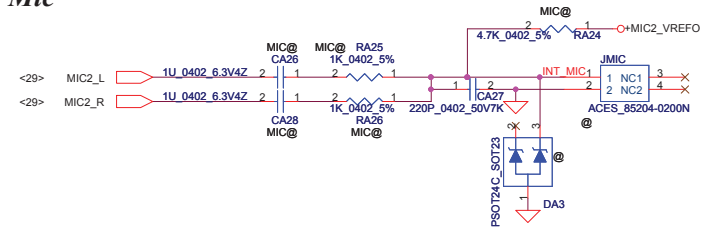


GAIN0	GAIN1	Av (db)	Rin (ohm)
0	0	6	90K
0	1	10	70K
1	0	15.6	45K
1	1	21.6	25K

## Ext. Mic



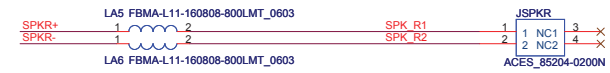
## Int. Mic



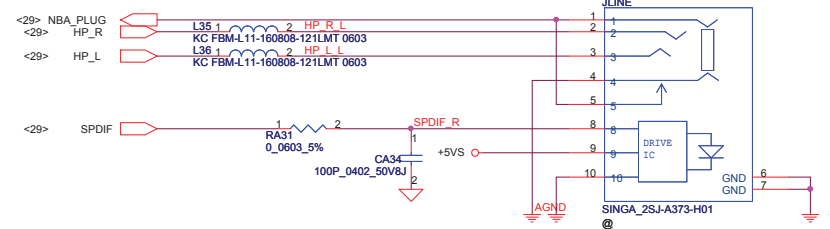
## Left Connector



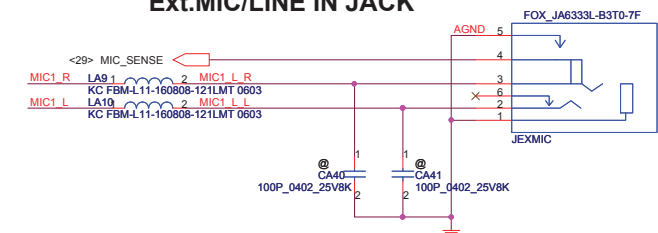
## Right Connector



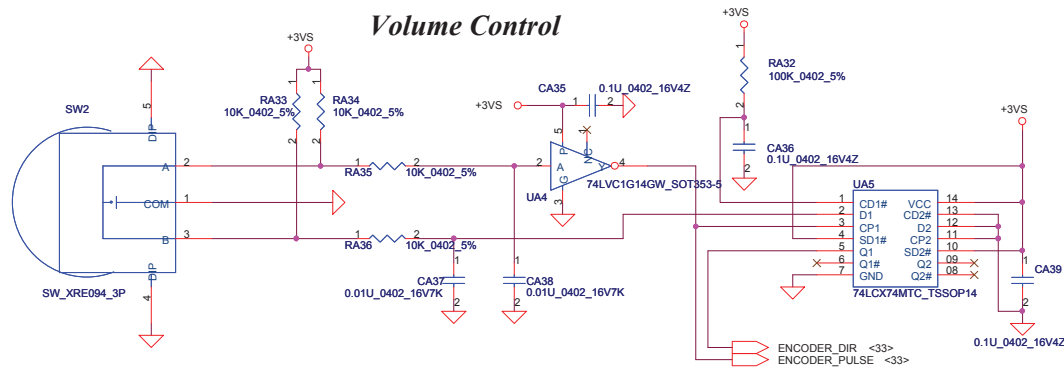
## HeadPhone/LINE Out JACK



## Ext.MIC/LINE IN JACK

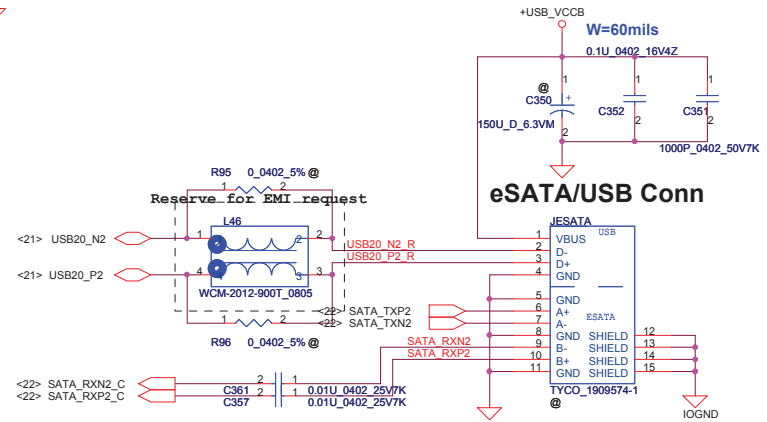
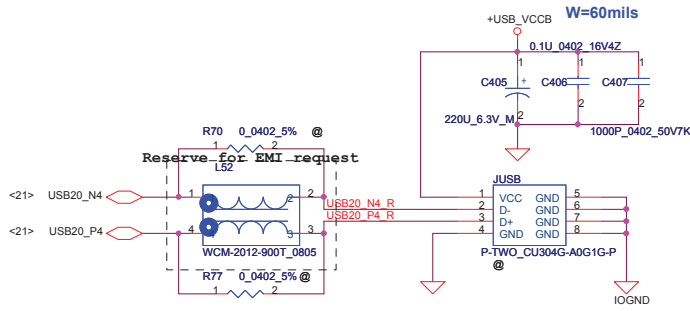
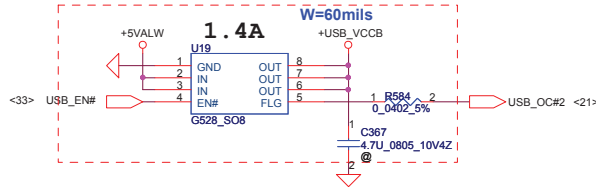


## Volume Control

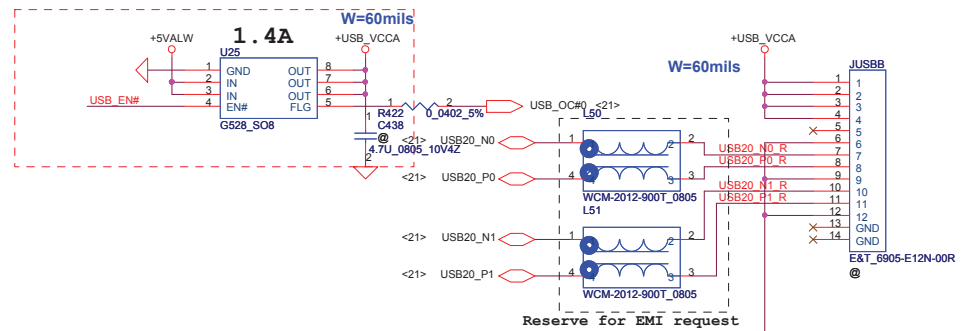


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				Custom	1.0
				Document Number	LA-4581P
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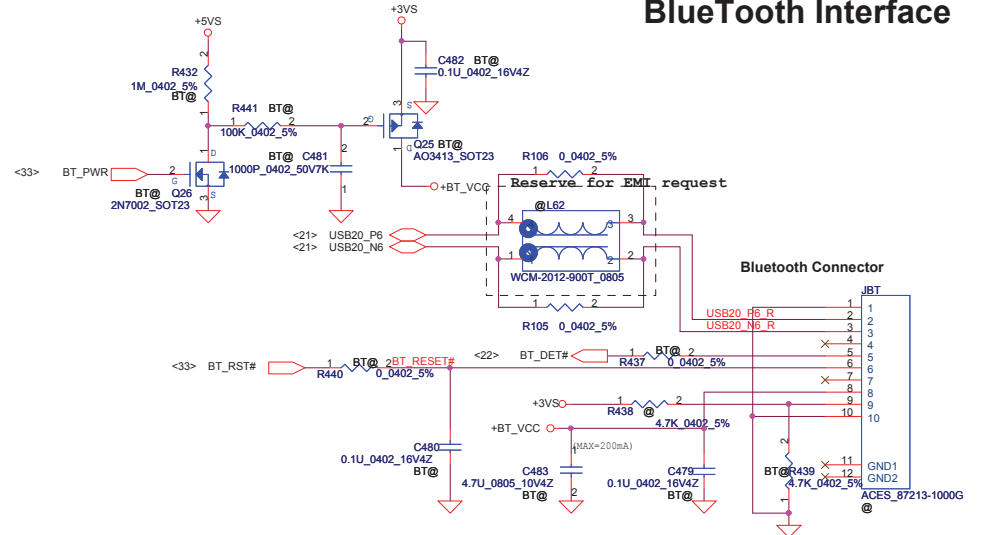
### eSATA/USB



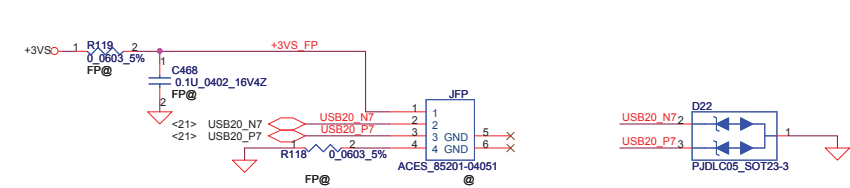
### USB Board



### BlueTooth Interface

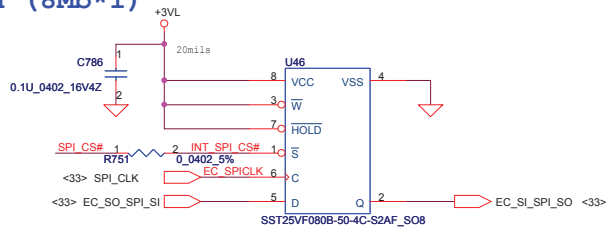


### Finger printer

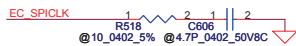


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				USB/BT/FingerPrint	
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				Date:	Friday, December 26, 2008
				Sheet	31 of 45

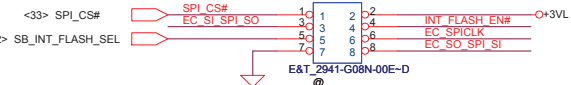
### SPI Flash (8Mb\*1)



### External Flash ROM

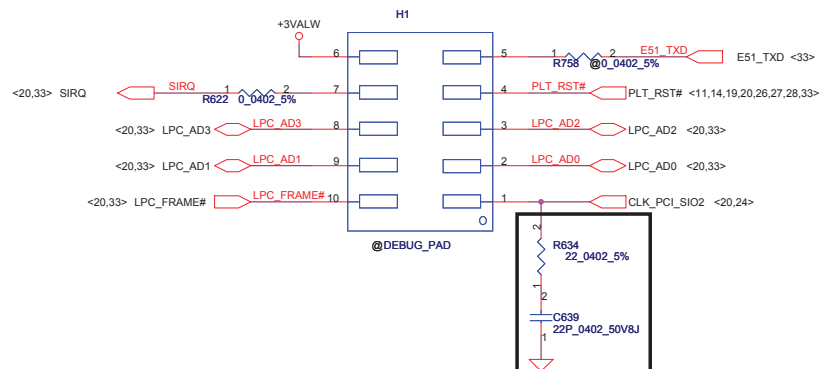


### External Flash ROM

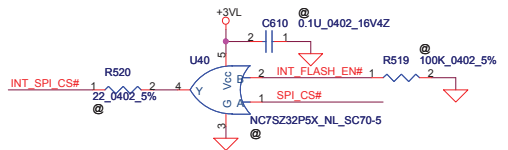


### LPC Debug Port

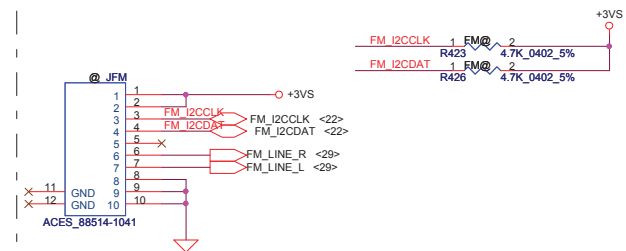
Please place the PAD under DDR DIMM.



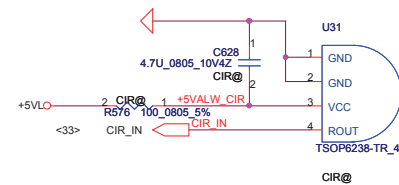
If these TEST@ components are mounded, please delete R387



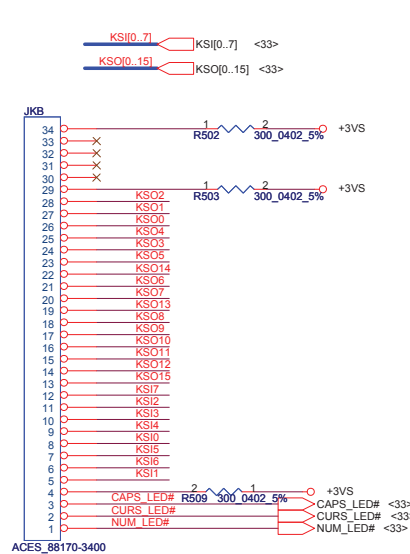
### FM tuner



### CIR



### KEYBOARD CONN.

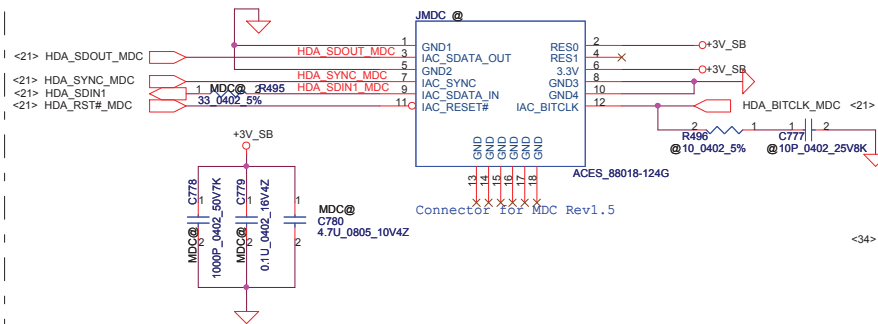


For EMI

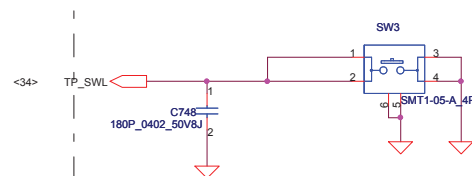
KSO2	C725	100P_0402_25V8K
KSO1	C717	100P_0402_25V8K
KSO0	C721	100P_0402_25V8K
KSO4	C609	100P_0402_25V8K
KSO3	C724	100P_0402_25V8K
KSO5	C728	100P_0402_25V8K
KSO14	C730	100P_0402_25V8K
KSO6	C715	100P_0402_25V8K
KSO7	C732	100P_0402_25V8K
KSO13	C733	100P_0402_25V8K
KSO8	C740	100P_0402_25V8K
KSO9	C737	100P_0402_25V8K
KSO10	C718	100P_0402_25V8K
KSO11	C738	100P_0402_25V8K
KSO12	C716	100P_0402_25V8K
KSO15	C736	100P_0402_25V8K
KSI7	C716	100P_0402_25V8K
KSI2	C741	100P_0402_25V8K
KSI3	C726	100P_0402_25V8K
KSI4	C723	100P_0402_25V8K
KSI4	C723	100P_0402_25V8K
KSI5	C731	100P_0402_25V8K
KSI6	C739	100P_0402_25V8K
KSI6	C735	100P_0402_25V8K
KSI1	C734	100P_0402_25V8K
CAPS_LED#	C722	100P_0402_25V8K
CURS_LED#	C727	100P_0402_25V8K
CURS_LED#	C714	100P_0402_25V8K
NUM_LED#	C714	100P_0402_25V8K

### MDC 1.5 Conn.

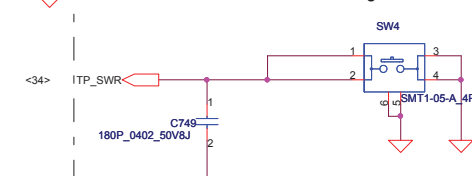
Change type 4/25



### Left switch

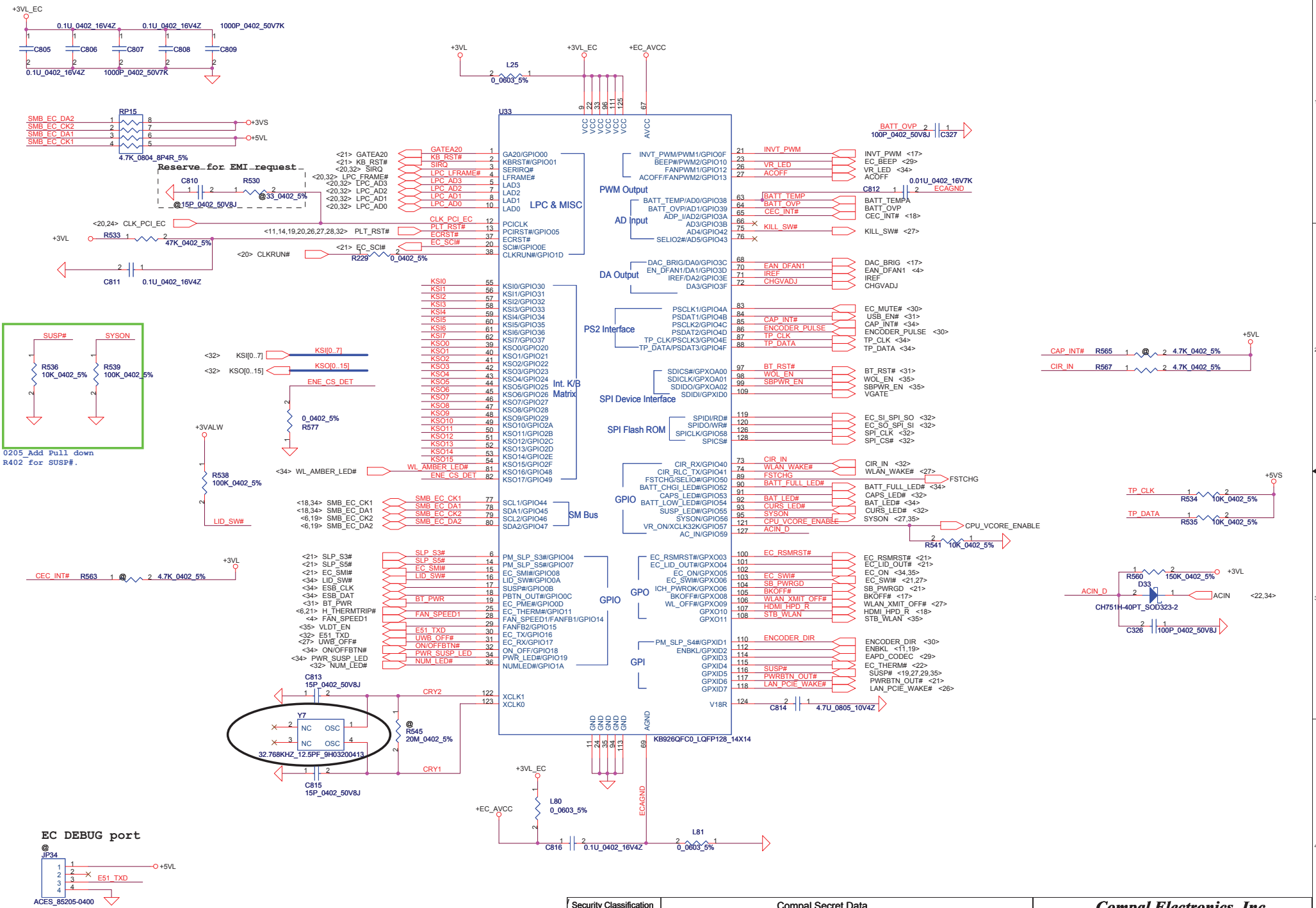


### Right Switch



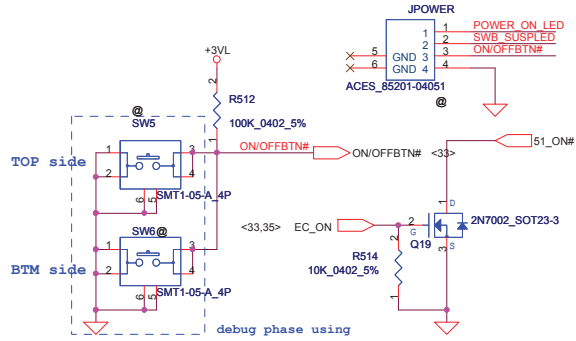
Security Classification	Compal Secret Data			Title <b>Compal Electronics, Inc.</b> <b>SPI/LPC/PS2/MDC/FM/CIR</b>	
Issued Date	2008/04/14	Deciphered Date	2009/04/14		
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				Rev <b>1.0</b>	
				Date: Friday, December 26, 2008	Sheet 32 of 45



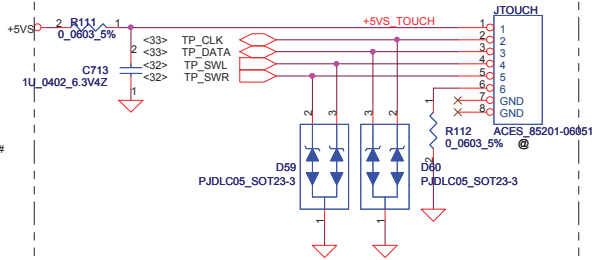


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Issued Date	2008/04/14	Deciphered Date	2009/04/14	ENE KB926C	
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Customer	Document Number	Friday, December 26, 2008	LA-4581P	33	1.0
Date:	Friday, December 26, 2008	Sheet	33	of	45

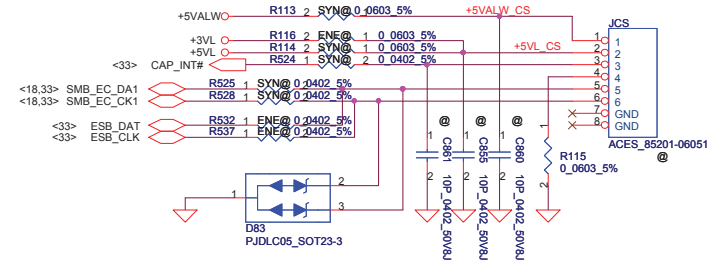
### Power Button/ PWR/B



### Touch/B Connector



### FUN/B Connector



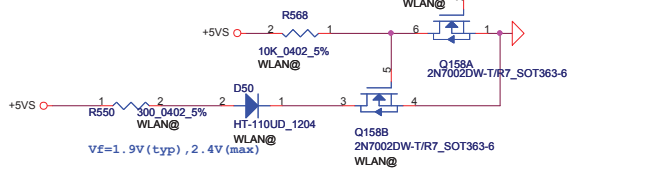
### DC-IN LED



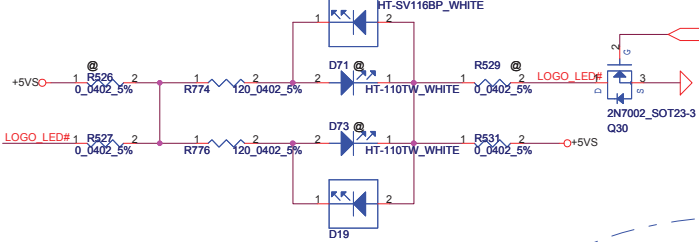
### POWER LED



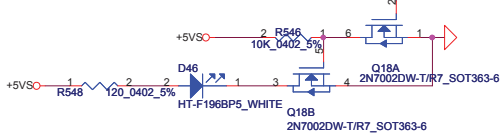
### WL&BT LED



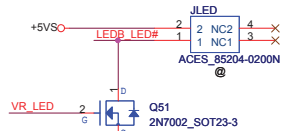
### Logo LED



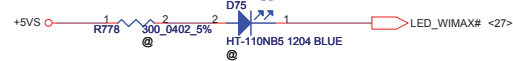
### HDD LED



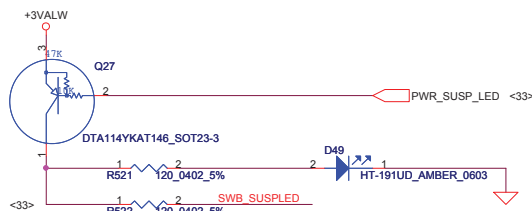
### LED/B Connector



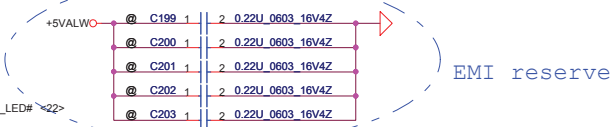
### GPS LED



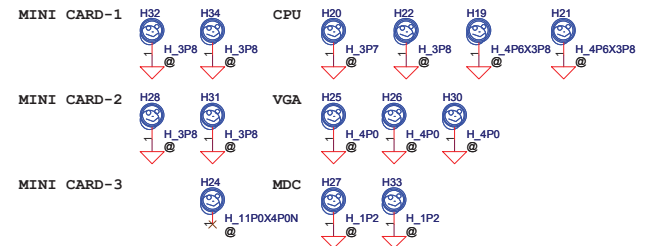
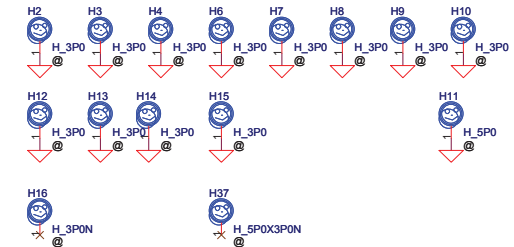
### SUSPEND LED



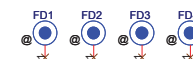
### BATT CHARGE/FULL LED



### Screw Hole



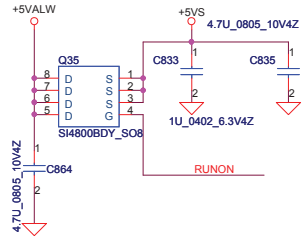
### PCB Fedcal Mark PAD



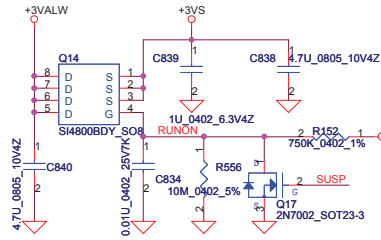
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Title <b>LED/LID/PB/FB/SCREW HOLE</b>		
Size	Document Number	Rev
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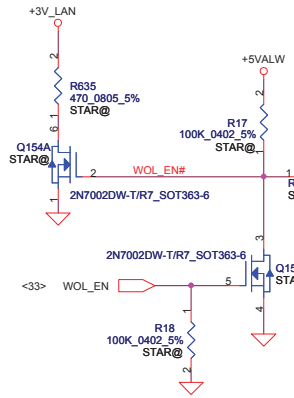
**+5VALW TO +5VS**



**+3VALW TO +3VS**

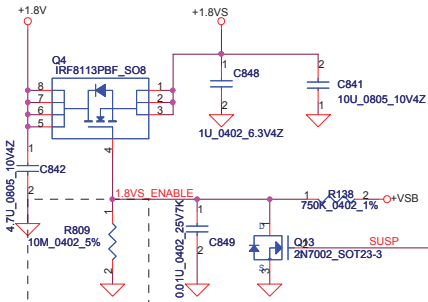


**+3VALW TO +3V\_LAN**

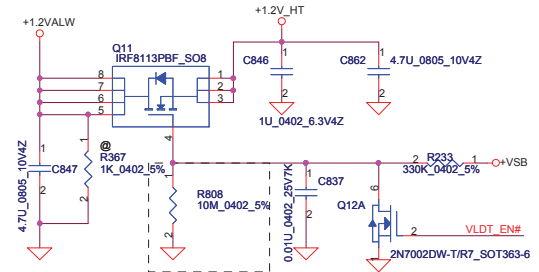


$V_{gs} = -4.5V, I_d = 3A, R_{ds} < 97m\Omega$

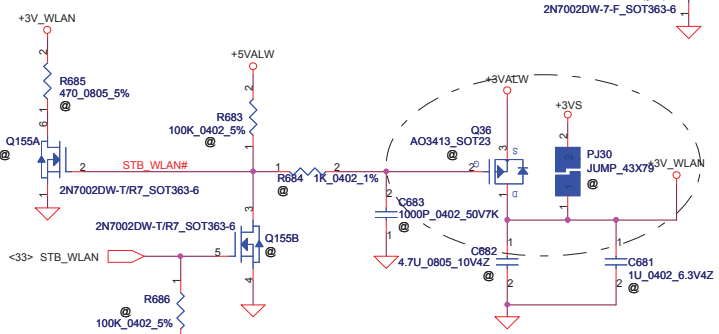
**+1.8V TO +1.8VS**



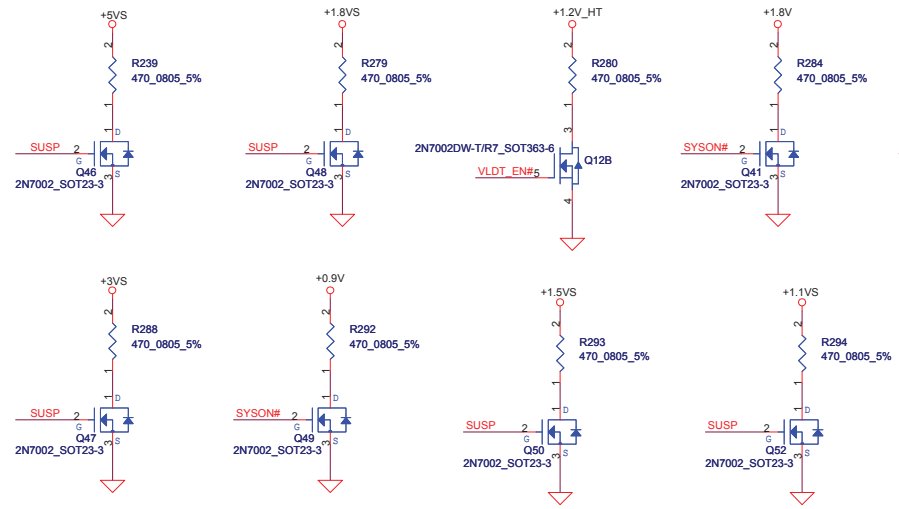
**+1.2VALW TO +1.2V\_HT**



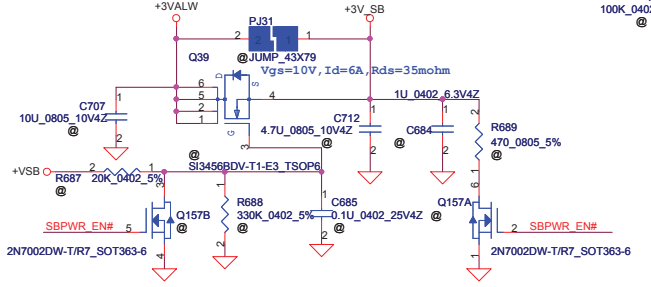
**+3VALW TO +3V\_WLAN**



**Discharge circuit**

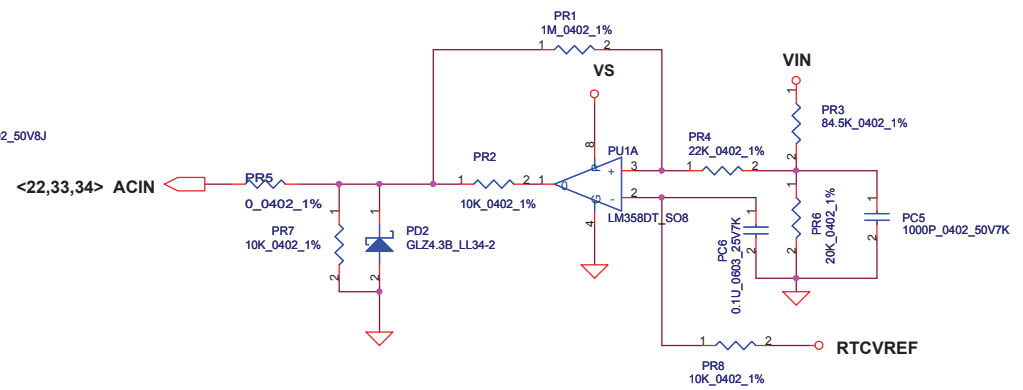
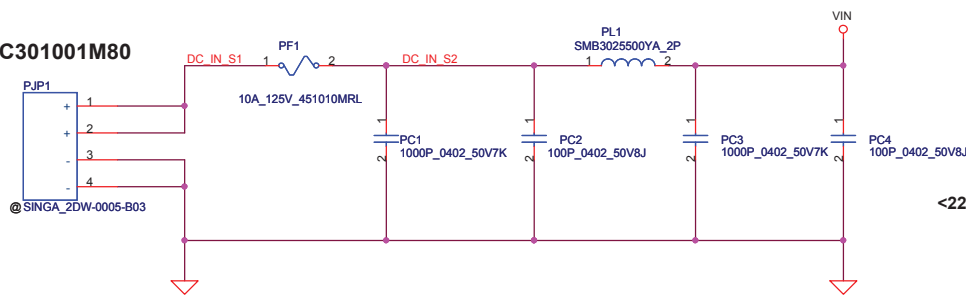


**+3VALW TO +3V\_SB**

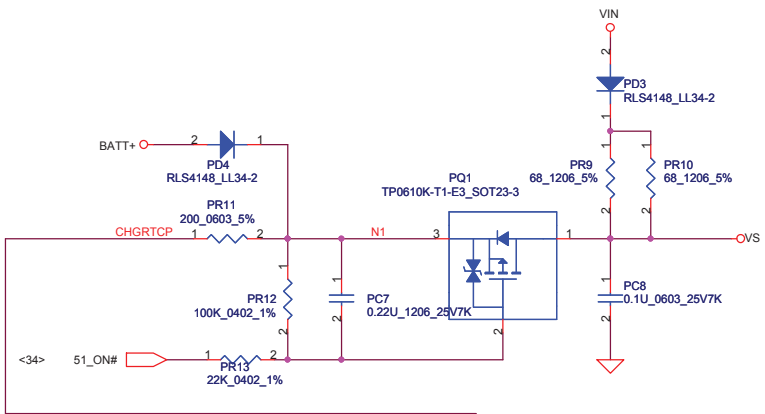


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Issued Date	2008/04/14	Deciphered Date	2009/04/14	DC/DC Circuits	
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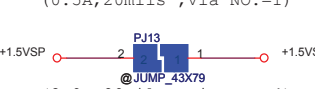
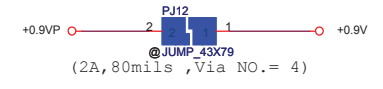
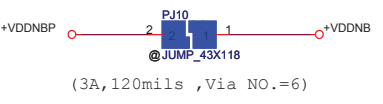
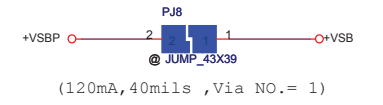
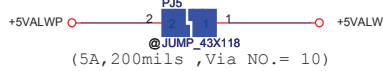
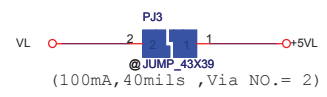
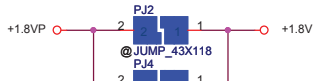
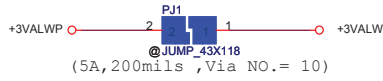
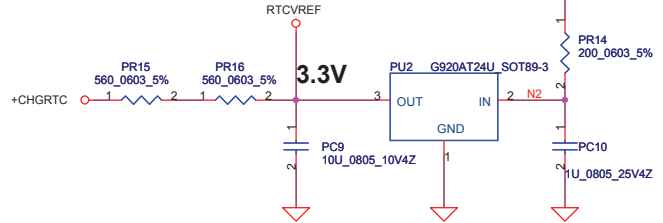
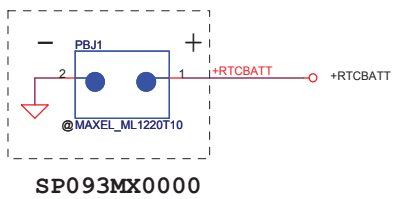
**DC301001M80**



Vin Detector			
High	18.384	17.901	17.430
Low	17.728	17.257	16.976

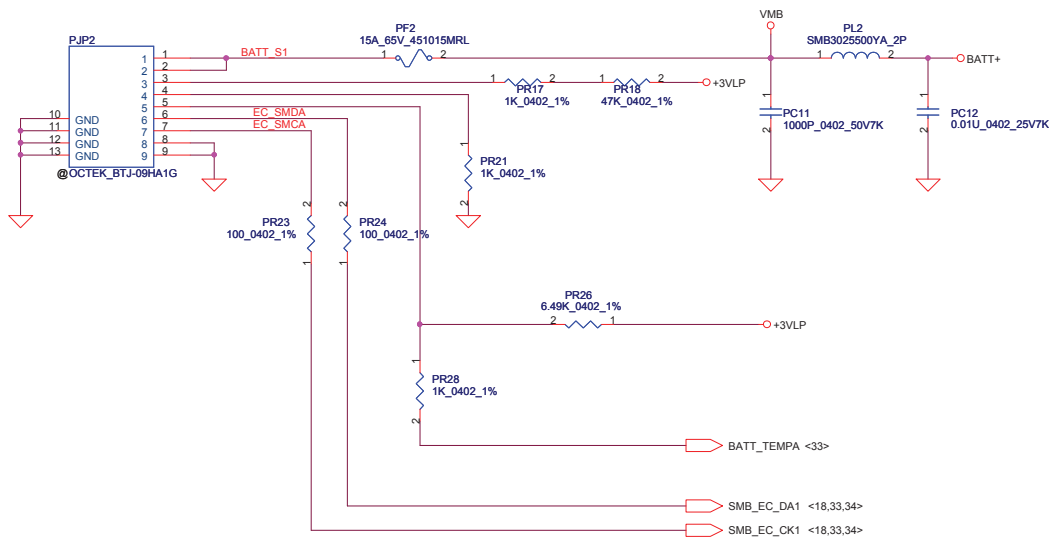


**RTC Battery**

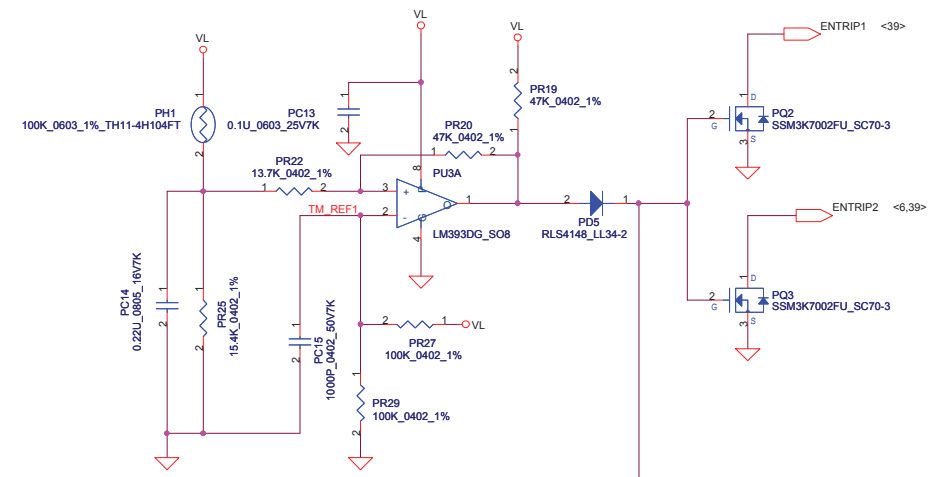


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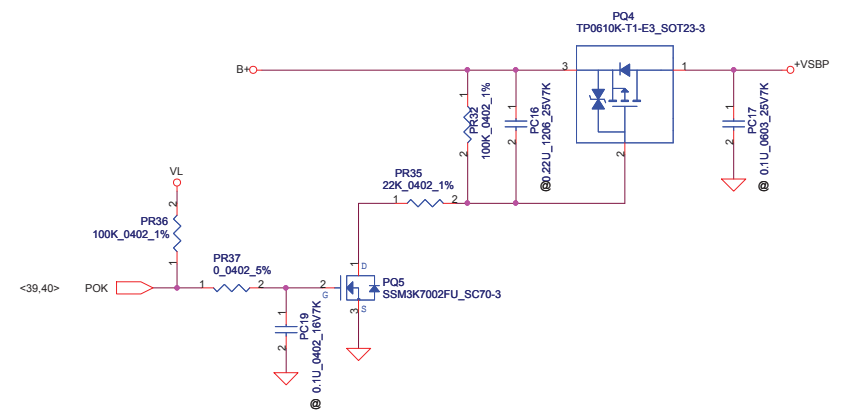
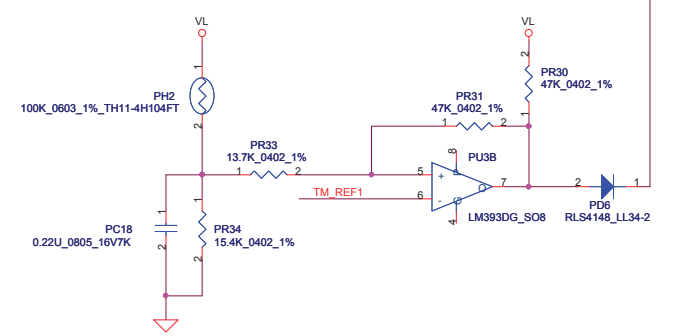
Compal Electronics, Inc.			
Title <b>DCIN/DECTOR</b>			
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**PH1 under CPU bottom side :**  
 CPU thermal protection at 92 degree C  
 Recovery at 56 degree C

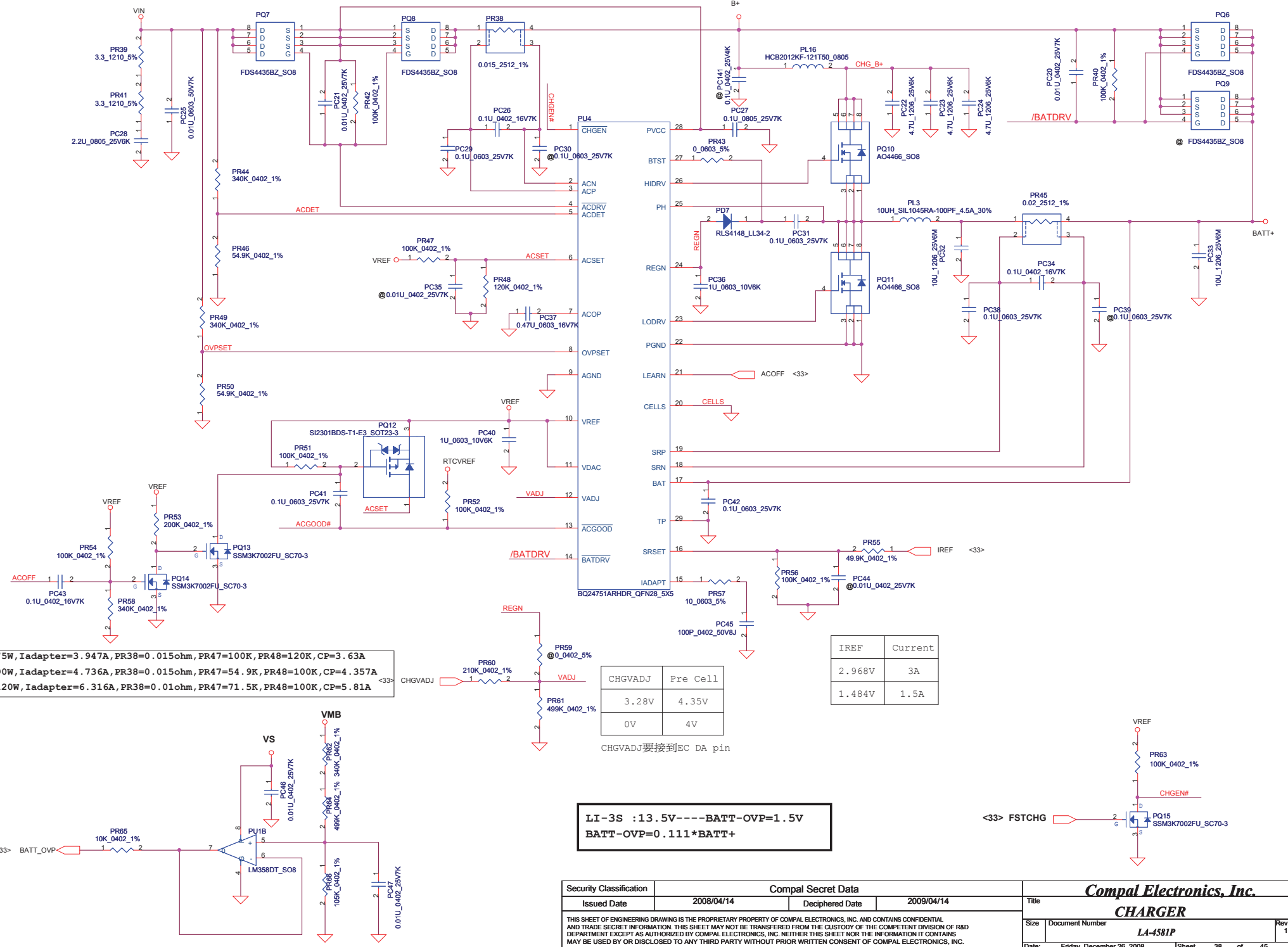


**PH2 near main Battery CONN :**  
 BAT. thermal protection at 92 degree C  
 Recovery at 56 degree C



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**Compal Electronics, Inc.**  
**BATTERY CONN / OTP**  
 LA-4581P  
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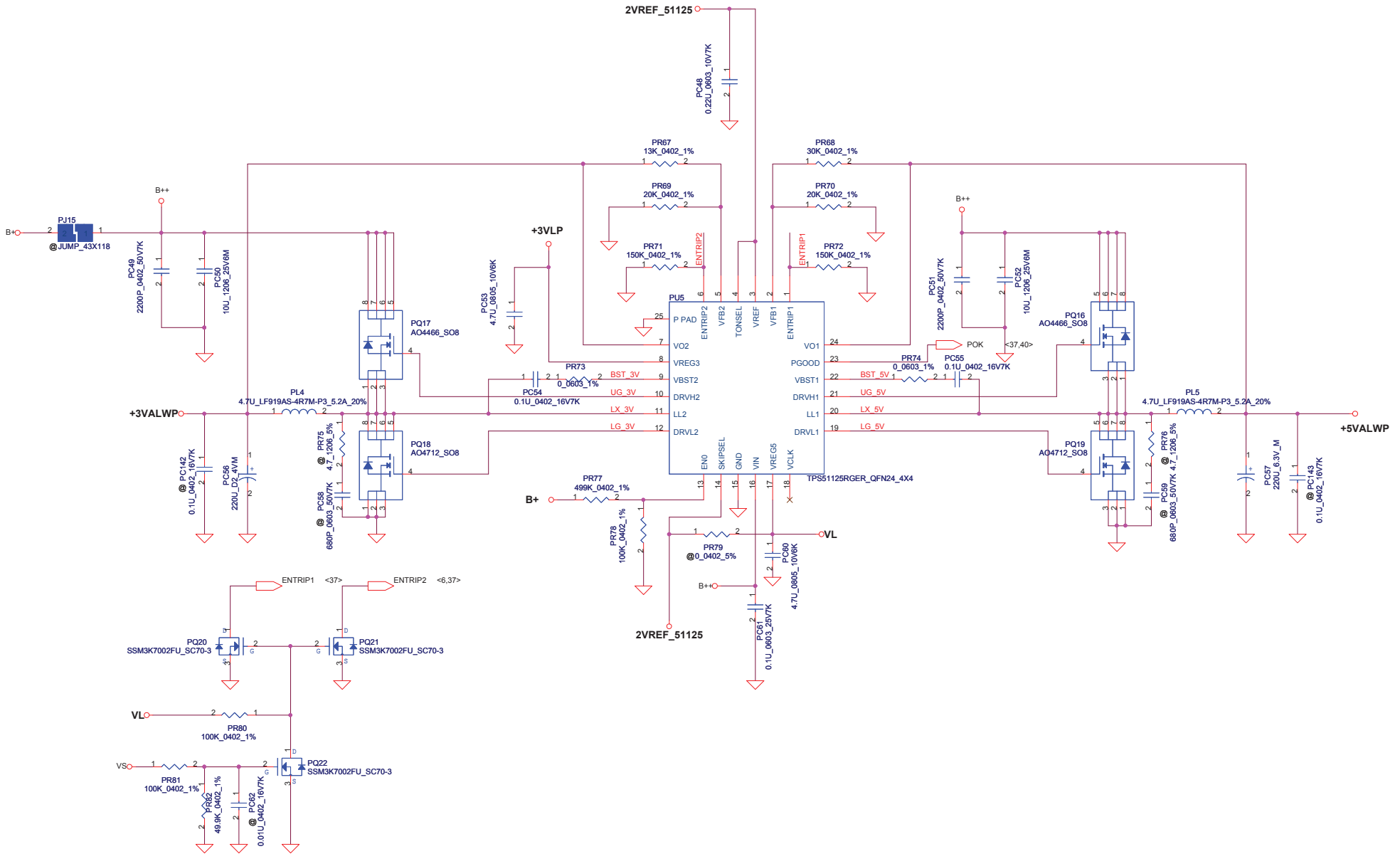


75W, Iadapter=3.947A, PR38=0.015ohm, PR47=100K, PR48=120K, CP=3.63A  
 90W, Iadapter=4.736A, PR38=0.015ohm, PR47=54.9K, PR48=100K, CP=4.357A  
 120W, Iadapter=6.316A, PR38=0.01ohm, PR47=71.5K, PR48=100K, CP=5.81A

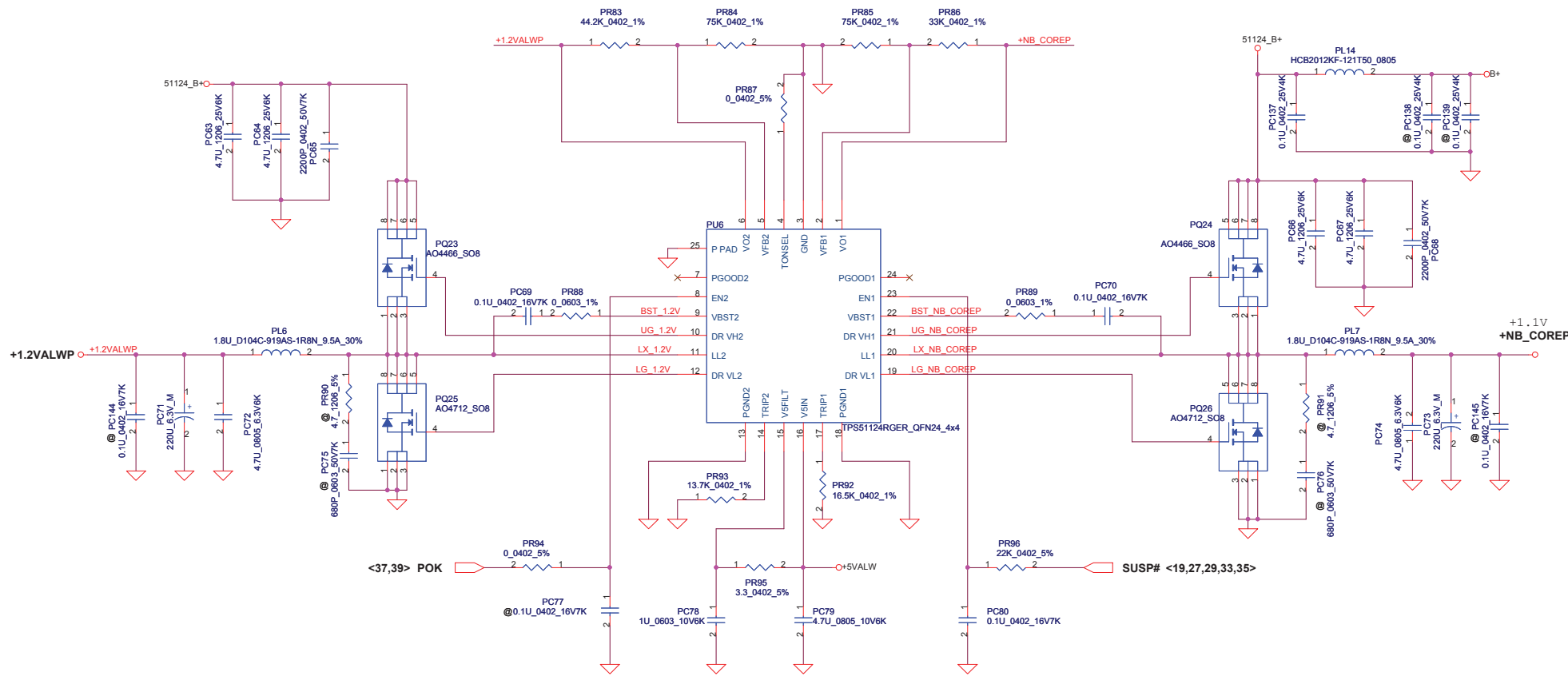
CHGVADJ	Pre Cell
3.28V	4.35V
0V	4V

IREF	Current
2.968V	3A
1.484V	1.5A

**LI-3S : 13.5V---BATT-OVP=1.5V  
 BATT-OVP=0.111\*BATT+**



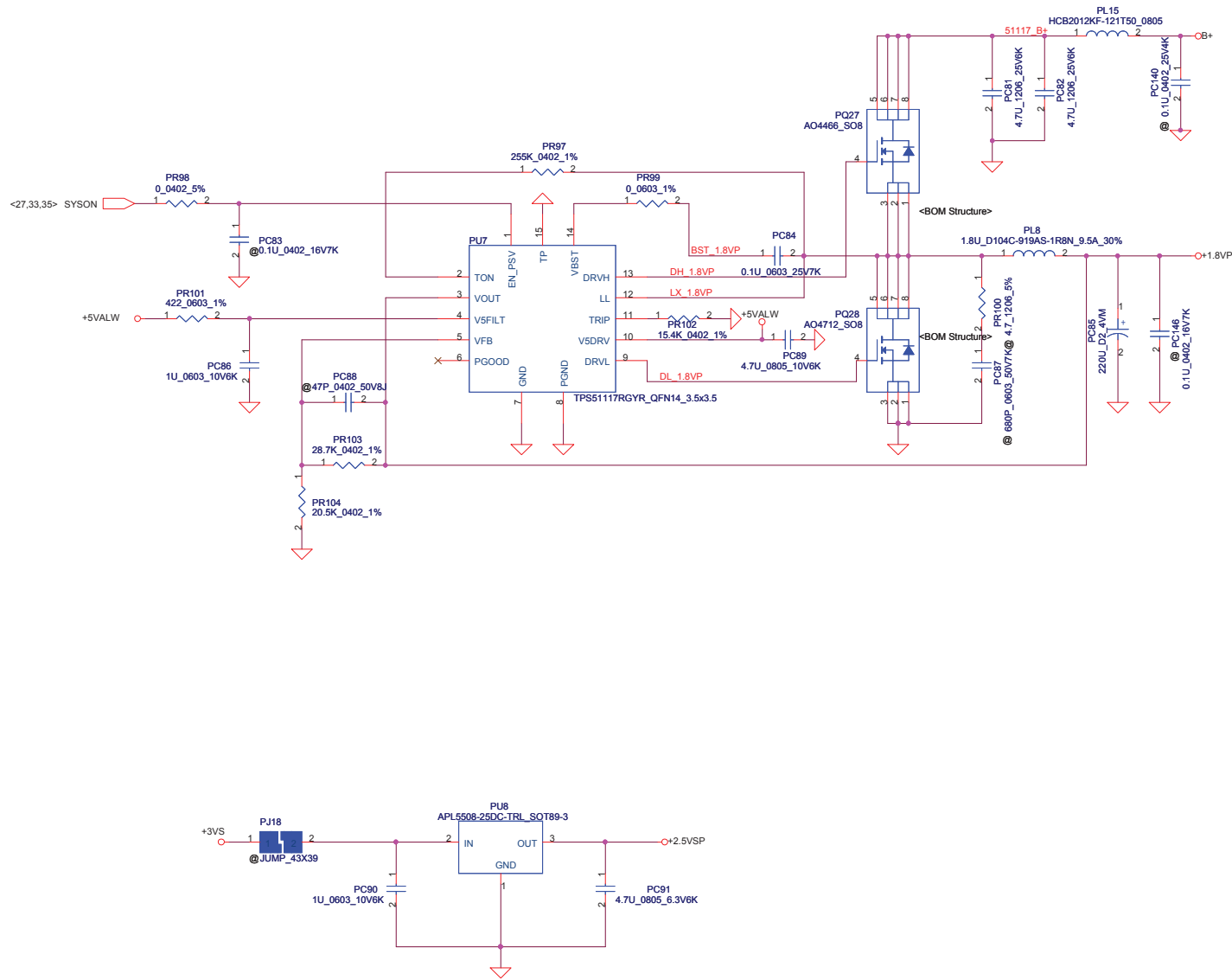
Security Classification	Compal Secret Data		Title	
Issued Date	2008/04/14	Deciphered Date	2009/04/14	3VALW/5VALW
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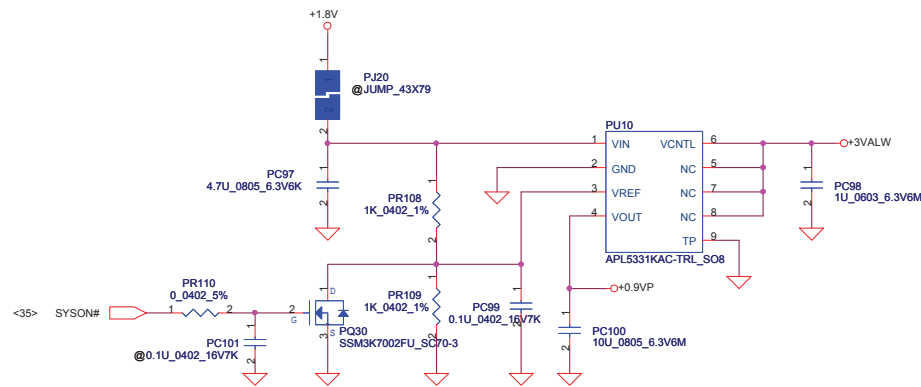
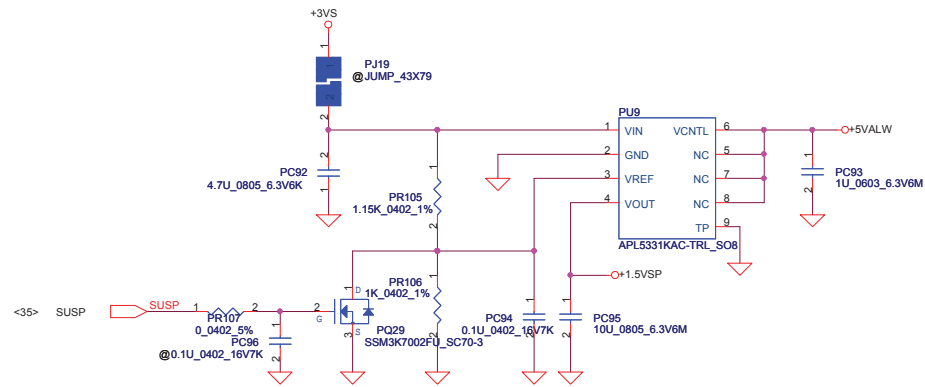
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<b>Compal Electronics, Inc.</b> <b>NB_COREP/1.2VALWP</b>			
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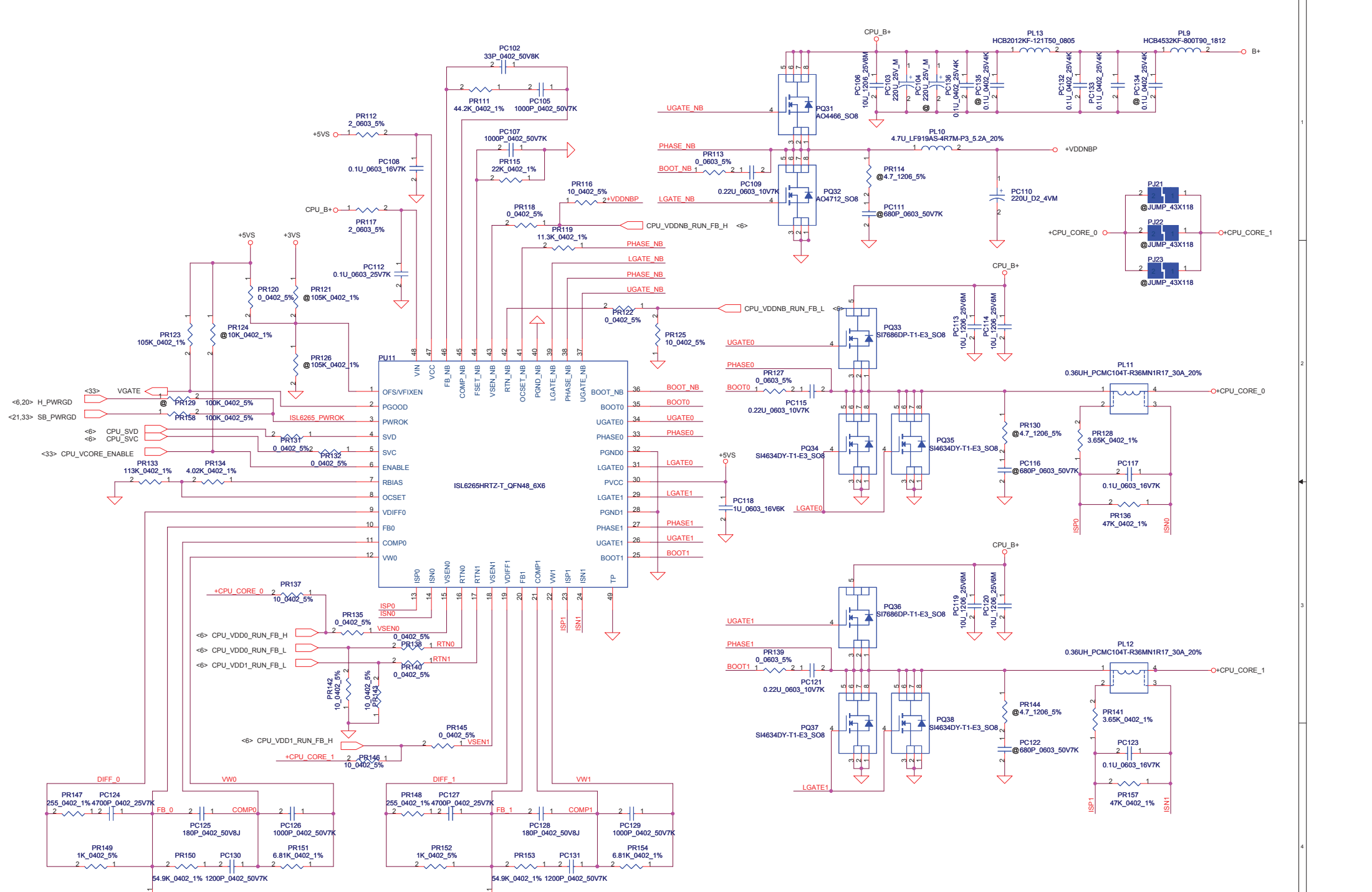


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Title			<b>Compal Electronics, Inc.</b>
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				Custom	1.0
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# Version Change List (P. I. R. List) for Power Circuit

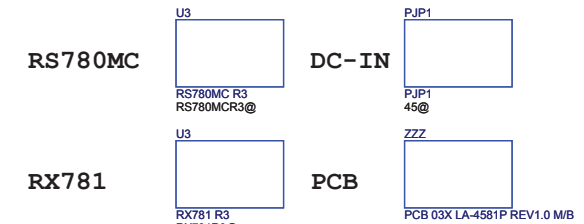
Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
43		Add PR158 remove PR129	2008/06/23	HW	Code 88	change EC to CPU control signal,PWROK	
41		Change UMA PR102 to 15.4K	2008/06/23	POWER	OCP to low	Change trip resistor.	
42		Change PU10 SUSP to SYSON#	2008/06/23	HW		Change control signal	
39		Add PC142,PC143	2008/07/23	SED	GPS	Reduce GPS noise	
40		Add PC144,PC145	2008/07/23	SED	GPS	Reduce GPS noise	
41		Add PC146,Change PC85	2008/07/23	SED,ME	GPS	Reduce GPS noise	

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# HW4 Product Improvement Record (P.I.R.)

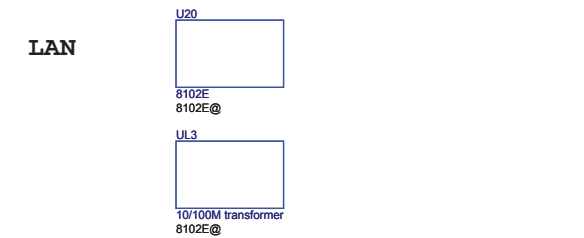
Revision Change: 0.1 to 0.2

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	6/20	27	Exchange UIM_RESET and UIM_CLK connect to J3GSIM	Correct schematic
2	6/20	21	Change FM_I2CCLK and FM_I2CDAT to GPIO50, GPIO51	For NXP request
3	6/20	25	Remove JHDD1	Remove Dip HDD
4	6/20	34	Change Q27.3 to pull up with +3VALW and R521, R522 to 120ohm	Solve suspend led issue
5	6/22	27	Change CM15, CM16 to 10P and un-mount RM1 and CM14	For customer request
6	6/23	32	Change ROM from 1M to 2M	For BIOS request
7	6/23	30	Change CA30, CA32 from 0.47u to 0.033u	Set high pass frequency to 68Hz
8	6/24	16, 29	Reserve C177, C181, C193	For EMI request



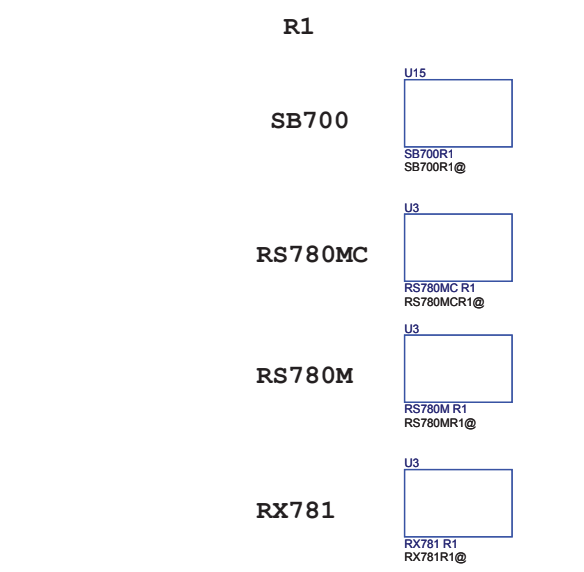
Revision Change: 0.2 to 0.3

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	7/14	29	Remove Felica function schematic	KTKAE don't support
2	7/14	18	Change U39.5 from +HDMI_5V_OUT to +5VL	For customer request and follow Toshiba deisgn guide with CEC
3	7/18	21	Change internal camera USB port from port 5 to port 9	For USB sleep and charge function
4	7/21	27	Change New card SMBus from 1 to 0	For Express card logo
5	7/22	32	Change MDC power from +3VS to +3V_SB	Support wake on MDC
6	7/22	28	Add ESD diode near 1394 connector	For EMI request
7	7/23	22	Add SPI ROM schematic on SB	For AMD+ENE issue
8	7/24	34	Co-layout LOGO LED	Change logo led to high illumination
9	7/24	32	Change BIOS ROM from 2M to 1M	For SW request
10	7/24	28	Add D3E mode schematic	For Energy star
11	7/24	26	Add LAN saving mode schematic	For Energy star
10	8/8	21	Change R328, R329 to 1.2K	For new card recognize issue
11	8/8	22	Add R557	Correct CIR schematic
12	8/8	16	Change R433, R435 from 137 to 150ohm	For TV out
13	8/8	21	Correct HDA SSC schematic	For EMI request
14	8/8		Add EMI test schematic	For EMI request



Revision Change: 0.3 to 1.0

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	8/06	6	CPU thermtrip connection	For customer request
2	8/11	29	Change Camera power from +5VALW to +5VS	For Energy star
3	8/12	32	Delete TEST@	For MP
4	8/12	35	Change all +3VALW to +3V_WLAN components from STAR@ to @	No need
5	8/12	22	Add R557	Correct CIR schematic
6	8/13	28	Correct JMB380 schematic	For Energy star
7	8/24	26	Delete R398	No need LAN saving mode function
8	8/24	35	Short PJ31, Delete Q15, R24, R20, Q39, Q157, R687, R688, R689, C707, C685, C684, C712	For SB leakage issue
9	8/24	18	Add L85, L86, L87, L88, Delete R616~R621, R623, R624	For EMI request
10	8/28	33	Change R536 from 100k to 10k	For LED twinkle when insert AC issue
11	9/10	26	Remove R399	No DSM function
12	9/24	6	Add C24	Add ESD solution



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